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ALESSANDRA LEONHARDT

Compact Modelling and Parameter Extraction of Nanoscale FinFETs

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Advisor: Prof. Dr. Sergio Bampi
Coadvisor: Prof. Dr. Luiz Fernando Ferreira

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UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
Reitor: Prof. Carlos Alexandre Netto
Vice-Reitor: Prof. Rui Vicente Oppermann
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Bibliotecária-chefe do Instituto de Informática: Beatriz Regina Bastos Haro

"Life is like riding a bicycle. To keep your balance, you must keep moving."

— ALBERT EINSTEIN

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ALESSANDRA LEONHARDT AND SERGIO BAMPI, Analytical Compact Models for Long Channel Double Gate MOSFETs : A Review. **XXIX South Symposium on Microelectronics - SIM**, 2014.

ALESSANDRA LEONHARDT, LUIZ FERNANDO FERREIRA AND SERGIO BAMPI, Effective Device Electrical Parameter Extraction on sub-22nm FinFETs. **IEEE International Symposium on Circuits and Systems - ISCAS**, 2015. (Submitted to publication)

ALESSANDRA LEONHARDT, LUIZ FERNANDO FERREIRA AND SERGIO BAMPI, Nanoscale FinFET Global Parameter Extraction for the BSIM-CMG Model. **VI Latin American Symposium on Circuits & Systems - LASCAS**, 2015. (Accepted)

ABSTRACT

This graduation work presents a study of FinFETs, compact models and their parameter extraction procedures, and also the results of parameter extractions of measured FinFET devices for different compact models, as well as other electrical parameters extracted from the transistors.

The first part of this report will explain in detail the existing challenges to further scale the dimensions of the MOSFET device, such as short channel and parasitic effects, as well as large statistical device variations, that have become proeminent and assume a higher influence in the device behaviour. The FinFET architecture promises a better electrical behaviour in sub-22nm lengths, and will be discussed in detail. A large set of FinFET devices has been manufactured in the IMEC Institute, Belgium, and characterised in the PhD thesis of (FERREIRA, 2012) and is used throughout this work. The FinFET devices range from 10µm to 45nm of mask length, with fin thickness of 10nm, 15nm and 20nm.

A compact model uses assumptions and simplifications to predict the electrical output characteristics of a device, while being computationally efficient. In this work, the EKV Double-Gate model, the BSIM-CMG and the PSP-DGFET will be studied, along with their parameter extraction procedures. Changes are proposed to the BSIM-CMG global parameter extraction in order to ensure that the parameters are consistent with the whole set of devices.

The results obtained for the implemented parameter extractions are presented and discussed. Electrical parameters, such as series resistance and effective length have been extracted using different methodologies available in the literature. The extracted series resistance ranges from 500Ω to 300Ω, and the channel length reduction varies between 14nm and 16nm. The EKV Double-Gate model and parameter extraction has been implemented in MATLAB and the results show weaknesses in the model. The BSIM-CMG parameter extraction procedure was implemented in IC-CAP and shows an accurate fitting over a wide range of channel lengths using a single set of parameters, with error mean absolute around 20% in all operation regimes. Subjective analysis are also used to compare and demonstrate issues that the models and extraction procedures present.

Keywords: FinFETs. Compact Models. Parameter Extraction. MOSFET. BSIM-CMG. EKV-DG. Effective Channel Length.

1 INTRODUCTION

The MOSFET technology has been driving the semiconductor industry to its current power for the last five decades. The dimensions of the transistors have been shrinking consistently from channel lengths of several micrometers to the current technology of tenths of nanometers. Several challenges are faced, however, in order to push forward this reduction in length, such as threshold voltage roll off, drain induced barrier lowering (DIBL), gate leakage, subthreshold slope degradation, gate induced drain leakage (GIDL), and also higher statistical variability. The FinFET architecture promises a better electrical behaviour in dimensions of few nanometers, and is regarded as the best alternative to further scale the transistor without a fundamental change in substrate material or fabrication flow. A large set of silicon on insulator FinFET devices has been manufactured by the IMEC Institute, Belgium, and characterised in the PhD thesis of (FERREIRA, 2012) and is used throughout this work. The measured FinFET devices range from 10µm to 45nm of mask length, with fin thickness of 10nm, 15nm and 20nm. In order to integrate the FinFET technology in modern circuit design, an accurate electrical modelling is essential, since compact device models are important tools for circuit designers.

The parameter extraction was performed in two different ways, although related: first, using extraction methodologies to assess electrical parameters such as series resistance, effective channel length, threshold voltage and subthreshold slope. These extractions were made using the methodologies presented in (SUCIU; JOHNSTON, 1980; CAMPBELL et al., 2011; TORRES-TORRES; MURPHY-ARTEAGA, 2002; WONG et al., 1987). The second part of the parameter extraction was performed for different compact models, adopting the proposed methodologies, in order to obtain a set of parameters to correctly simulate the FinFETs, using a certain device model.

A compact model uses assumptions and simplifications to predict the electrical output characteristics of a device, while being computationally efficient. In this work, the EKV Double-Gate model, the BSIM-CMG and the PSP-DGFET will be studied, along with their parameter extraction procedures. The EVK model for double-gate semiconductor devices (SALLESE et al., 2005; PRÉGALDINY et al., 2006; TANG et al., 2009; CHEVILLON et al., 2009; YESAYAN et al., 2011) is an academic and simple charge based model, with its long channel core model available in VHDL in (PRÉGALDINY et al., 2006). The BSIM-CMG was formulated in (DUNGA et al., 2007; DUNGA, 2008; DUNGA et al., 2008) and afterwards expanded in (LU et al., 2010; LU, 2011; CHAUHAN et al., 2011). It is an already solidified analytical model for multi gate devices, already implemented in commercial simulators such as the Cadence SPECTRE Circuit Simulator (CADENCE DESIGN SYSTEMS, 2013), used for the model simulations in this report. Finally, the PSP compact model for FinFETs (SMIT et al., 2006; SMIT et al., 2007; DESSAI et al., 2009) derived from the PSP surface potential model. It has no accessible implementation, however.

In order to correctly describe a given technology, a compact model needs a set of physi-

cal and fitting parameters, which is obtained from measured data using a parameter extraction procedure. A parameter extraction can be either global, to extract a single set of parameters to model a wide range of devices, or local, that accurately model transistors with small variations in channel length and width. The parameter extraction procedures of the studied models are explained and detailed in this report. The parameter extraction for the EKV Double-Gate model is adjusted to improve the model fitting. Changes are proposed to the BSIM-CMG global parameter extraction in order to ensure that the parameters are consistent with the whole set of devices.

Finally, the results obtained for the implemented parameter extractions are presented and discussed. Electrical parameters, such as series resistance and effective length have been extracted using different methodologies available in the literature. The EKV Double-Gate model and parameter extraction has been implemented in MATLAB and the results examined. The SPECTRE implementation of the BSIM-CMG was used and the parameter extraction procedure implemented in the Keysight IC-CAP Device Modeling Software. The quality of the extraction and modelling is assessed using the mean absolute percentage error (MAP Error) methodology. Subjective analysis are also used to compare and demonstrate issues that the models and extraction procedures present.

This work is organized as follows: in chapter 2 the MOSFET technology is reviewed, and the FinFET architecture detailed, along with comparisons. Chapter 3 explains in detail the models studied, with their equations, assumptions and issues. The effective device parameter extraction is addressed in chapter 4. The extraction procedures for the studied models are detailed, comprehensibly. In this chapter, the changes proposed in this work for the extraction procedures are presented, alongside their motivation. In chapter 5, the results of the mentioned parameter extractions are shown and discussed. Finally, chapter 6 summarizes the conclusions this work has reached, and points future lines of research that appeared as a direct or indirect result.

2 SCALING OF FETS BELOW 100-NM

2.1 CMOS Scaling Challenges

The CMOS transistor can be considered the greatest invention of the 20th century and has revolutionized the field of electronic devices and systems. For the last five decades the transistor has become steadily smaller and the integrated circuit density has increased, which in turn has made it cheaper, more powerful and more efficient. Scaling has doubled the device density in integrated circuits with each generation, as described by Moore's observation (MOORE, 1965).

The length scaling in MOS transistors allows for improvements in both electrical performance and packing density, where a reduction by a factor α provides a scaling in area equivalent to α^2 (SZE, 1998). Transistor scaling generally followed simple rules: either to maintain the electric field constant or to allow it to increase, but to conserve the shape of the potential profile in the scaled device (LIU; CHANG, 2009). The saturation of the carrier velocities and non scaling of the subtheshold slope and the OFF current forced for more generalized scaling rules (FRANK et al., 2001). Fundamental physical limits, however, have imposed challenges to the scaling trend of MOSFETs (KIM, 2010; ZEITZOFF, 2004).

The parameter non-scaling mentioned above present another difficulty, which slows the voltage reduction trend from one technology node to the next, since the ON/OFF current ration has to be high enough to allow for efficient circuits. Voltage reduction is not attractive for high performance circuits, where the switching time of the CMOS is fundamental. However, if the drain bias remains roughly constant while the other dimensions are scaled, however, the direct and transverse electric fields rise such as to degrade the effective carrier mobility (CHAUDHRY, 2013). A fine balance has to be achieved, thus, where the applied voltages are not low enough in order to still have a adequate ratio of ON/OFF current, but not high enough to cause mobility scattering and hot electron emissions.

The physical dimensions are limited by quantum mechanical tunnelling currents that pass through the various barriers in the transistor when they are sufficiently thin, deteriorating the electrical behaviour of the MOSFET. Tunnelling current through the gate insulator is one of the most restraining limits to scaling. The most commonly used gate insulator, SiO_2, presents high gate current leakage with thickness of approximately 2nm. If the oxide is kept at this thickness, while the rest of the device scales, the gate capacitance becomes insufficient to properly control the channel region as it shrinks and the source and drain get closer. This in turn increases the effect of DIBL, as the drain bias has increased control over the channel. The solution for the oxide tunnelling issue was to use insulators with higher dielectric constant, which provide the same gate capacitance while increasing the physical insulator thickness. Significant leakage current reductions could be achieved, yet sacrificing interface quality between the dielectric and the body or gate of the device. The surface scattering arising from the use of high-k dielectrics can be then reduced by the use of a mid-gap metal gate such as TiN (CHAU et al., 2004). This

combination of metal gate and high-k dielectric improves the mobility in the channel, compared to using only the dielectric and a conventional poly-Si gate. The association of metal gates and high-k dielectrics are nowadays integrated in several mainstream semiconductor foundries, being an important reason for the scaling of planar CMOS to the current geometries.

To minimize short channel effects in bulk MOSFETs, very high doping concentrations are necessary, in order to reduce the gate-controlled depletion width in the channel. This high doping profile, however, has an effect in raising the value of the threshold voltage V_{th}, which can be avoided by employing retrograde channel doping (TAUR et al., 1997). The technique of nonuniform doping is difficult to accurately control and very sensible to statistical variability, specially in very small channel lengths. Device-to-device variations arising from the statistical variability of the doping process – known as Random Dopant Fluctuation – cause reliability issues for the integrated circuit (TANG; DE; MEINDL, 1997; ASENOV, 1998; ASENOV, 2007). A very high doping concentration in the MOSFET channel also result in degraded carrier mobilities due to Coulombic scattering, and phonon scattering due to high effective transverse field (LIU; CHANG, 2009).

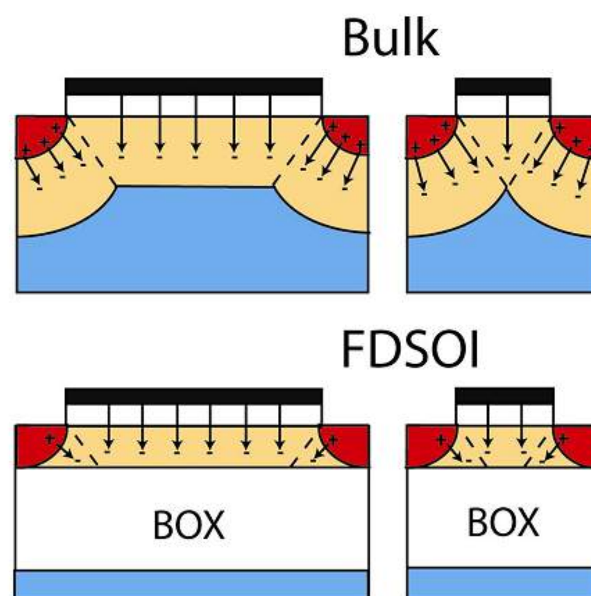


Figure 2.1: Charge distribution in long and short channel bulk and SOI MOSFETs (THOMAS, 2011).

The need for precisely controlled vertical channel and source/drain doping profiles to suppress SCE can be avoided by physically limiting the thickness of the semiconductor body. The thin body structure decreases the drain/source coupling with the channel and thus improves electrostatic control of the gate over the channel. Silicon-on-insulator wafers are commonly used for this purpose, with body thickness of 10nm or less. A high precision in the physical silicon thickness is necessary, however, in order to achieve controlled electrical characteristics.

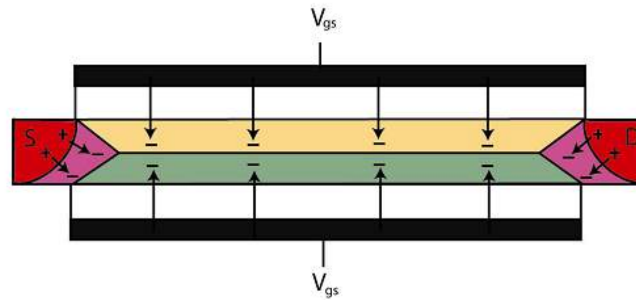


Figure 2.2: Cross section of a fully depleted double-gate MOSFET, showing the electric field and depletion charges from both gates and source and drain(THOMAS, 2011).

This ultra thin film is challenging to fabricate and is prone to self heating (SU et al., 1994). The use of a second gate, opposite from the first further improves the gate coupling over the channel, and relaxes the body thinness requirement, so that quantum confinement effects and mobility degradation due to surface scattering can be mitigated. The double-gate structure, first proposed in (Sekigawa; Hayashi, 1984), reduces short channel effects such as DIBL and subthreshold slope due to its better control of the longitudinal electric field generated by the drain (COLINGE, 2008). Fig. 2.1 presents a schematic comparison of the gate control over the channel for long and short channel bulk and SOI MOSFETs. In the short channel bulk device, it can be noted how the source and drain diffusions have a greater influence over the channel, which is mitigated in the fully depleted SOI (FDSOI) counterpart. Fig. 2.2 illustrates how a double-gate transistor has an even improved performance, regarding gate electrostatic control and the influence of the transversal drain electric field over the channel, allowing further scaling.

The main challenge, however, for the adoption of the double gate technology is the fabrication of both gates self-aligned to the source and drain. The gates also have to be perfectly aligned and of the same size, so as to provide high drive current while reducing the parasitic capacitances. Lastly, the two gates have to be connected with a low-resistance path (NOWAK et al., 2004). The final challenge for the adoption of the double gate MOSFET structure is to be compatible with the current fabrication process flow.

2.2 FinFETs

A FinFET (HISAMOTO et al., 1998; HUANG et al., 1999) is a tri- or double-gate semiconductor device with self-aligned source and drain regions and gates aligned to each other. Figure 2.3 shows a schematic of a tri-gate FinFET device with multiple fins, with most relevant lengths and thickness indicated. It is important to note that in a tri-gate FinFET, the channel width is given by $2H_{fin} + T_{fin}$ for each fin. Typical FinFET devices have several parallel fins. This geometry creates the possibility of increasing the channel width, and thus the current drive, by increasing the silicon film thickness, which controls the H_{fin}, producing a wider channel in the

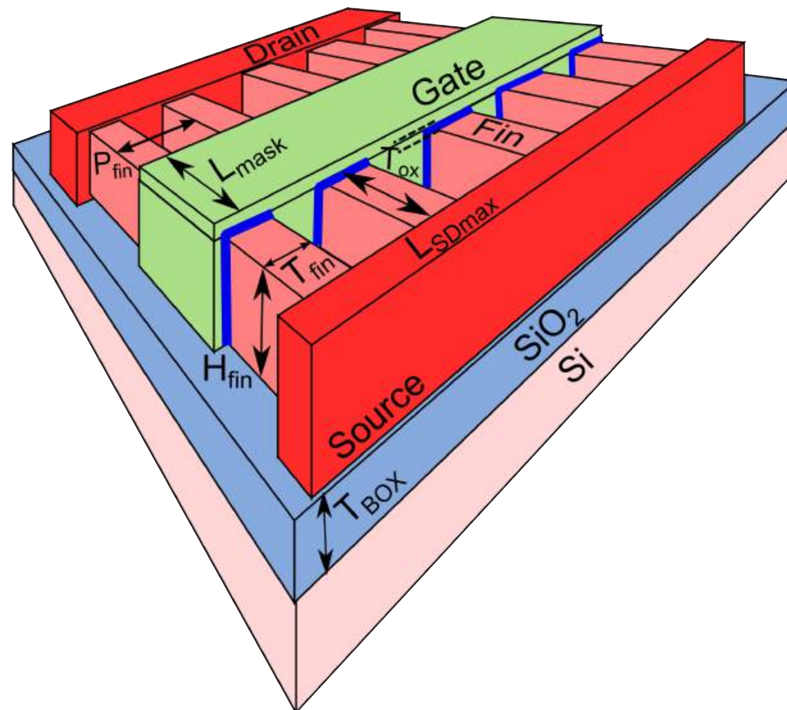


Figure 2.3: FinFET device with multiple fins

same device area.

The first FinFET device was fabricated in Berkeley in 1998 (HISAMOTO et al., 1998) called folded-channel MOSFET. The device was later named FinFET (HUANG et al., 1999) due to the fin-like structure of the silicon channel. Ten years before,though, a very similar device, called DELTA had been fabricated (HISAMOTO et al., 1989), only without the hard mask on top of the fin, as proposed by the Berkeley group. Yet, any device with a fin-like body for the channel may be called FinFET. A scanning electron microscope image of a fabricated FinFET is shown in Fig 2.4.

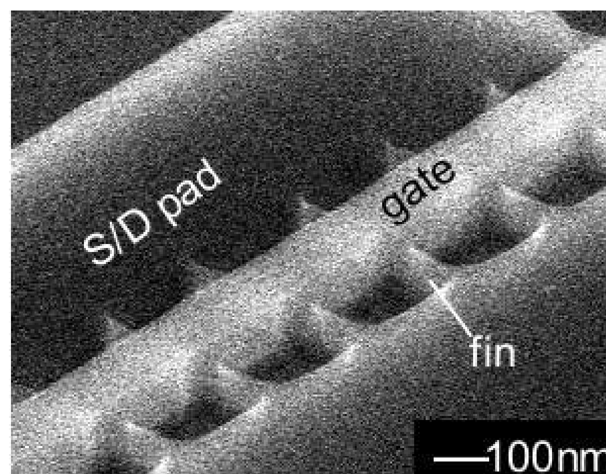
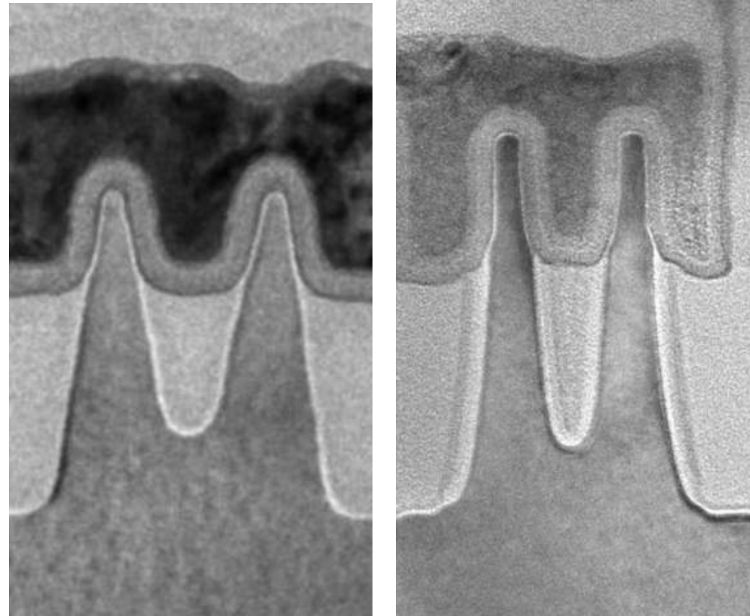


Figure 2.4: Scanning Electron Miscroscope image of a FinFET with multiple fins.

The fabrication of FinFET devices is very similar to the fabrication of conventional planar MOSFETs and holds even greater similarities with SOI devices (XIONG, 2008). The fins are patterned though steps photolithography and etch, the gate dielectric is deposited and the gate electrode is deposited on top of the fins and patterned to assume its correct dimensions. After that the source and drain regions are implanted in a carefully selected angle and the spacers are formed, similarly to planar MOSFETs. Selective epitaxial growth is performed on the fin extensions to reduce the series resistance. Metal via formation and routing follows the same steps as in traditional circuit fabrication. This compatibility with existing CMOS processing is an important reason for the adoption of this layout by the mainstream semiconductor industry and academic community. The most challenging step of the fabrication is the fin etch, which involves patterning through photolithography and etch. A perfectly smooth and uniform side-wall is desired for the fins, to reduce interface traps that degrade mobility and also decrease the variability of the metal gate work function, a factor which has a great influence in the threshold voltage of the device and thus are responsible for performance degradations (HWANG; LI; HAN, 2010; WANG et al., 2011; BELLO et al., 2013; ZIMPECK; MEINHARDT; REIS, 2014). This dependence of the threshold voltage upon the metal gate work function of the FinFET device is caused by the fact that the superior control the gate has upon the channel enables the use of undoped or lightly doped channels. As previously mentioned, lower doping concentrations are desired for better device uniformity and current drive. The threshold voltage is thus controlled essentially by the work function of the metal gate.

Intel has been the first chip maker to adopt the FinFET technology, calling it the Tri-gate Transistor. The first generation of devices is presented in Fig. 2.5a, from the work of (AUTH et al., 2012; AUTH, 2012). The fin width is 8 nm and the fin height is 34 nm, for the 22 nm gate length technology. The rounded fin are likely to reduce corner effects on the electric field, and improve reliability, but also can be due to the difficulty associated to the fin etching process. The tilted sidewalls offer higher mobility for the PMOS device, acording to (AUTH, 2012). Intel has also adopted the technology of bulk FinFET devices, rather than SOI FinFETs, probably because of price constraints. The next technological node, with 14nm gate length transistors is presented in 2.5b, extracted from a presentation of the technology (INTEL, 2014a). The fins have become taller and thinner, with 42nm of fin height, compared to 34nm. The fin pitch also lowered from 60nm to 42nm. The rounded edges is maintained, but the more vertical aspect ratio is clearly seen, which improves the performance and short channel effects control.

The review presented in (NOWAK et al., 2004), traces a brief comparison between planar bulk devices and double-gate FETs. The devices were simulated in the Taurus MEDICI simulator. Fig. 2.6a compares the $I_D x V_G$ characteristics for two devices designed to have the same subthreshold current density at V_{GS} = 0. The slope is clearly steeper in the double-gate device, indicating a better control over short channel effects, and also rendering higher drive currents at lower voltages. A lower V_{DD} power-supply voltage is possible in such devices. Fig. 2.6b presents both DIBL and subthreshold swing (also referred as subthreshold slope in other parts



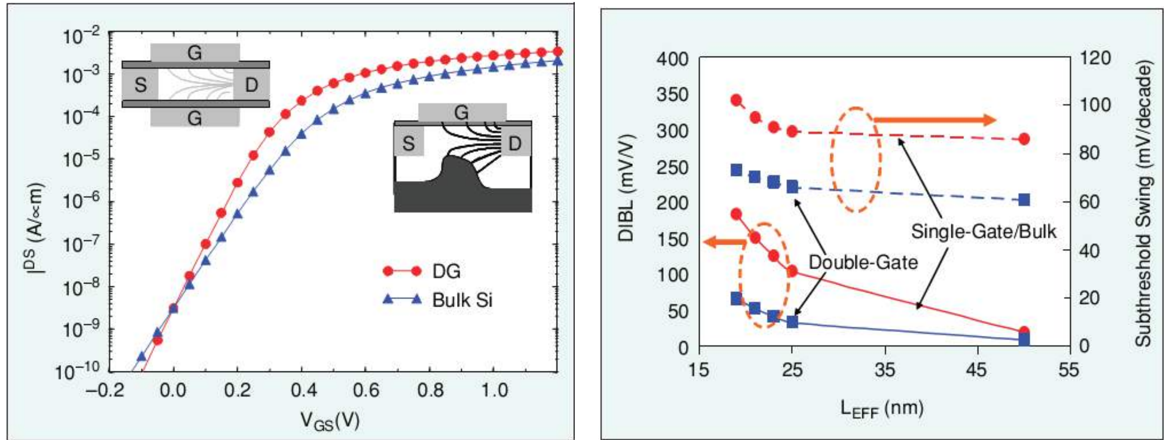
(a) TEM image of an 22nm Intel Tri-gate Transistor (AUTH et al., 2012; AUTH, 2012; INTEL, 2014a)

(b) TEM image of an 14nm Intel Tri-gate Transistor (INTEL, 2014a)

Figure 2.5: Comparison between Intel aspect ratio and fin pitch of Tri-gate transistors from different technology nodes.

of this work) for bulk single-gate and double-gate devices, for different channel lengths. Both characteristics are improved by the use of a second gate, as clearly shown in the plot. It is important to note the greater increase for DIBL and sub-threshold swing in small geometries single-gate devices. This exponential increase in undesired effects deeply limits the scaling of planar bulk devices beyond existing gate lengths. The simulation results presented in Fig. 2.6b, however, are very optimistic, showing nearly perfect subthreshold swing for FinFETs down to 20nm of effective gate length.

The IMEC Institute created experimental comparisons between planar bulk MOSFETs and SOI FinFETs for electric characteristics and performance in the works of (SUBRAMANIAN et al., 2005) and (SUBRAMANIAN et al., 2006). The FinFETs under study were fabricated on SOI wafers with 145 nm buried oxide thickness. The undoped fin height is 60nm with 25nm of fin thickness. A high-k insulator and TiN metal gate were used. The planar bulk MOSFETs were fabricated with either high-k insulator ("HiK") or SiON and TiN metal gate. Fig. 2.7a illustrates, experimentally, the already mentioned fact that the FinFET devices have superior subthreshold slope, compared to planar bulk devices. The subthreshold slope is nearly the optimal 60 mV/dec in FinFET devices with gate length greater than 100 nm, slightly rising for smaller devices. On the other hand, the planar devices present high sub-hreshold slope even for greater channel lengths, increasing exponentially for gate lengths below 100 nm.



(a) $I_D x V_G$ curves of double-gate and single-gate devices designed to have equal sub-threshold current density at V_{GS} = 0.

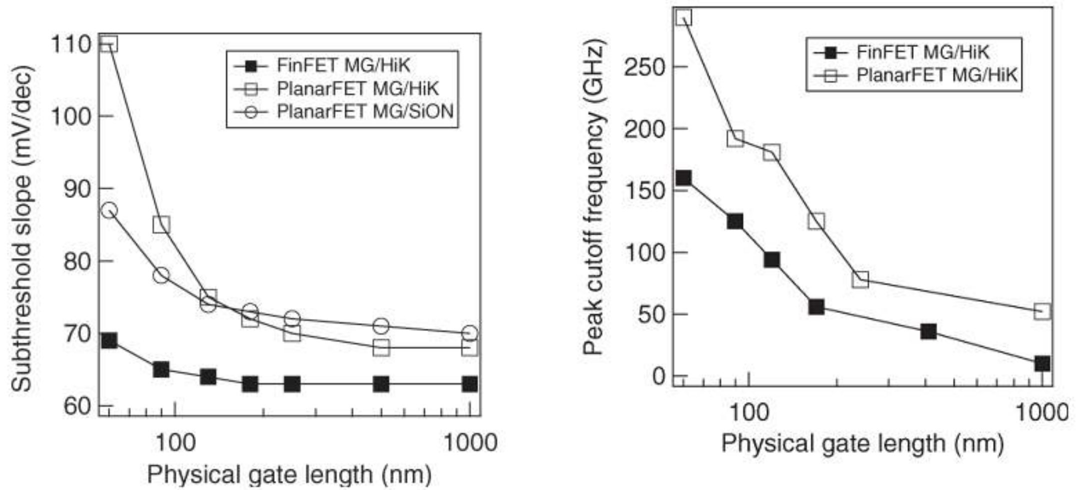
(b) DIBL and sub-threshold swing for double-gate and bulk planar devices. The double-gate device is designed with undoped body and near mid-gap gate metal.

Figure 2.6: Images removed from (NOWAK et al., 2004)

The study also points that the maximum intrinsic cutoff frequency of planar MOSFETs is greater than that of FinFETs, as seen in Fig 2.7b. The cuttof frequency is given by the peak transconductance $G_{m,max}/2\pi C_{GS}$, with C_{GS} the gate-to-source capacitance. Since FinFETs have high series resistance because of the reduced source/drain contact areas, the transconductance is lower than that of planar MOSFETs. The series resistance also increases with decreasing fin width (DIXIT et al., 2005). However, the series resistance issue can be further reduced by selective epitaxial growth of source and drain regions, as shown in (DIXIT et al., 2005; NICOLETTI, 2009).

The work presented in (CHENG; LI, 2010) simulates multiple-gate devices with different fin aspect ratios, as explained in Fig. 2.8, and compares its DC and dynamic characteristics. The simulations were performed for 16 nm gate length devices. The height and thickness (mentioned as W_{fin}) of the fin for each device are also explained in Fig. 2.8. The drive current of the FinFET device is larger, as illustrated in Fig. 2.9a, mainly because the FinFET presents a larger channel width ($= 2xH_{fin} + W_{fin}$), of 80 nm, compared to the 67.8 nm width of the Tri-gate and 64 nm channel width of the Quasi-planar simulated devices. Fig. 2.9b compares the devices regarding the DIBL each of them presents. As previously discussed, DIBL is reduced in multi-gate devices due to the superior control over the channel. FinFET devices present even smaller DIBL, because the complete volume inversion of the fin improves even further the control over the channel.

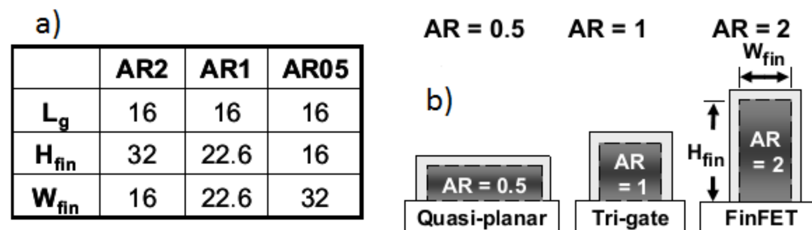
A large component of the off-state leakage current is gate-induced drain leakage current – GIDL – a quantum mechanical tunnelling between gate and drain in the drain region underneath the gate, due to high field effect in the drain junction (ROY; MAHMOODI-MEIMAND; MUKHOPADHYAY, 2003). In the accumulation region, the leakage current in mostly due to



(a) Sub-threshold slope for bulk MOSFETs and FinFETs

(b) Peak cutoff frequency at $V_{DS} = 1.2V$

Figure 2.7: Images extracted from (SUBRAMANIAN et al., 2006)



a)

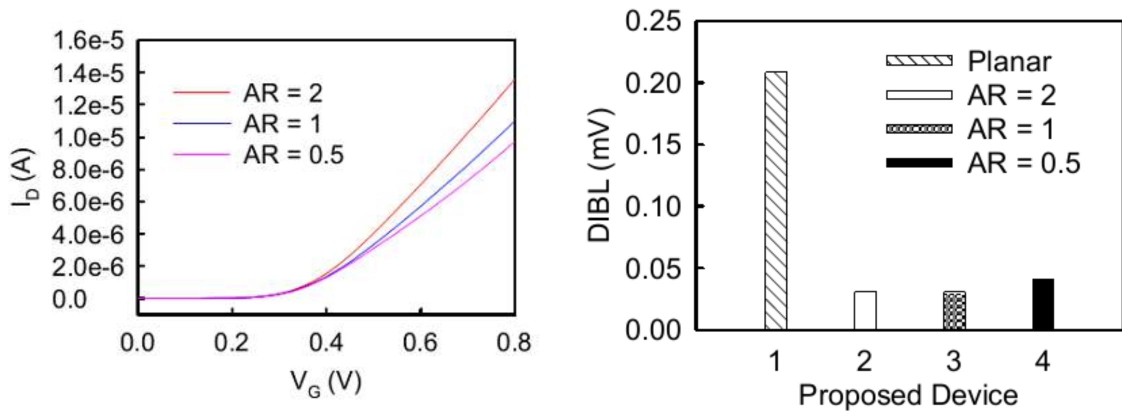
	AR2	AR1	AR05
L_g	16	16	16
H_{fin}	32	22.6	16
W_{fin}	16	22.6	32

Figure 2.8: Aspect ratios and geometries used in (CHENG; LI, 2010)

GILD. The advantage of thin body and double-gate architectures in reducing GIDL is investigated in (CHOI et al., 2003). It states that double-gate transistors have a better control over GIDL, in comparison to bulk and ultra thin body SOI devices. GIDL also decreases with a thinner silicon body – or fin, in the case of FinFETs – attributed to the lower transversal electric field and increase in tunnelling effective mass.

2.3 LDD Structure

The lightly doped drain (LDD) structure, proposed in (OGURA et al., 1980), is characterized by a lightly doped region n^- between the channel and the highly doped n^+ source and drain. The LDD device is fabricated using a first step of light doping concentration implant, after the gate stack formation, to create the self-aligned source and drain. The gate spacers are then formed and the source and drain are again implanted, this time with high doping concentrations. The schematic cross section of a LDD device is presented in Fig. 2.10, with n^- and n^+ regions shown.



(a) IDxVG curves of FinFET devices with different aspect ratio

(b) Comparison of DIBL present in planar and FinFET devices with different aspect ratio

Figure 2.9: From the work presented in (CHENG; LI, 2010)

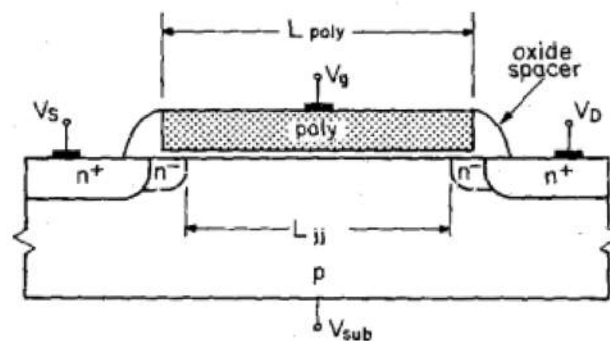


Figure 2.10: Schematic cross section of a LDD planar MOSFET device, as presented in (HU; CHANG; CHIA, 1987)

In a conventional MOSFET, the electric field has its peak near the metallurgical junction of drain and channel, and drops abruptly in the n^+ region. In a LDD device, however, the electric field spreads along the lightly doped region n^- before becoming zero at the drain, creating a “buffer zone”. The magnitude of the peak field is thus lower in the LDD MOSFET, which allows for higher device operation biases, while reducing hot electron emissions and impact ionization. Hot electrons in turn, break molecular bonds and generate interface traps, that are responsible for device degradation and reduction in its lifetime (HU et al., 1985). Thus, LDD structures, when properly designed, can increase device lifetime.

It must be noted, however, that the n^- region increases the series resistance in the device. Also, part of the lightly doped region is modulated by the gate bias, and thus the series resistance and ΔL change as a function of the gate voltage overdrive, as presented in Fig. 2.11 (SHEU et al., 1984; LIANG; DEEN, 1993; HU; CHANG; CHIA, 1987). This creates difficulties in the extraction of those parameters, which will be addressed in Chapter 4.

FinFET devices can be fabricated with LDD structures also, as is the case in (MAGNONE

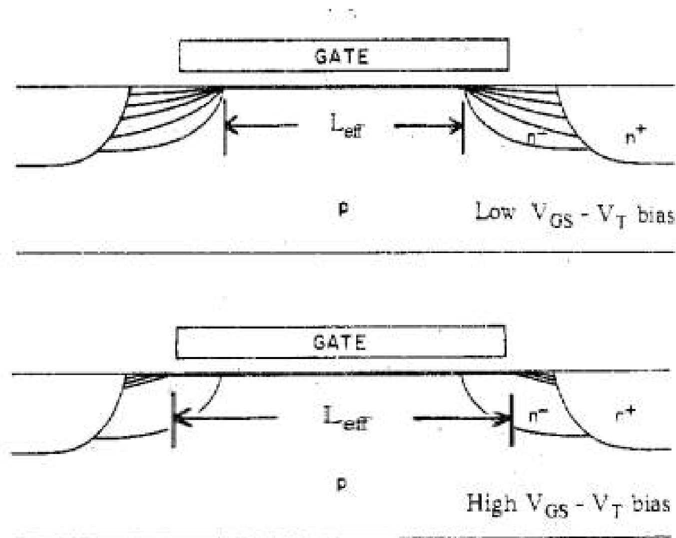


Figure 2.11: Current flow patterns in a LDD MOSFET. The top picture shows the operation in low V_{GS} bias, while the bottom is in high V_{GS} bias. The variation of L_{eff} is clearly seen in the different biases, as a result of the gate modulation of the n⁻ region. (SHEU et al., 1984)

et al., 2008) and the ones fabricated in the IMEC Institute and used in the PhD thesis of (FERREIRA, 2012) that will be studied in this work. The fabrication of FinFET LDD devices follows the same steps as in planar MOSFETs, with a lightly doping followed by spacers formation and a second implantation, with higher dopant concentration. In FinFETs, however, the implantation angle has to be carefully selected such as to prevent shadowing on the fins. This is extensively discussed in (FERREIRA, 2012).

3 COMPACT DEVICE MODELS

A device model is the interface between the fabrication process and the circuit design. All integrated circuits are designed and verified first in a circuit simulator such as SPICE, HSPICE and SPECTRE, and just then sent to actual fabrication. This simulation is performed using a compact model to describe the behaviour of a given technology. Their accuracy is essential, specially for the design of analog circuits, but also for performance and timing improvements in digital circuits. Compact models have a simplified analytical formulation to determinate the I-V or C-V characteristics of transistor, using a specific set of parameters. They avoid numerical solutions for the device properties by making assumptions that simplify the derivations of an analytical solution. Compact models also have a fine balance between their physical accuracy and their compactness, which is, their simplicity and computational efficiency. Some applications and project phases might use more simple and computationally efficient models, while others might require a higher accuracy in the predicted electrical behaviour.

This work focusses on compact models for double-gate devices, more specifically FinFETs, expanding the work presented in the XXIX South Symposium on Microelectronics. Among the large number of proposed models, the EKV Double-Gate, the BSIM-CMG and the PSP-DGFET were chosen for having planar counterparts already established as default models for different circuit applications. The BSIM-CMG has already been released and is currently integrated in commercial circuit simulators, while the other models are still academic, with some work published, but no official release. In this chapter the features of the models will be briefly reviewed and discussed, and their parameter extraction detailed in the next.

3.1 EKV Double-gate

The EKV related model for double-gate devices (SALLESE et al., 2005; PRÉGALDINY et al., 2006; DIAGNE et al., 2008; CHEVILLON et al., 2009; TANG et al., 2009; YESAYAN et al., 2011) is proposed as a simplified, design-based compact model. It is a charge-based formulation, following the same form of equations as the planar EKV (ENZ; KRUMMENACHER; VITTOZ, 1995). The long channel core model is implemented in VHDL-AMS code in (PRÉGALDINY et al., 2006) and in this work ported to MATLAB and expanded to short channel devices according to the formulation presented in the articles cited above.

The long channel I-V equations are given in normalized forms, in order to simplify the model. The normalized drain current $i = I/I_S$ is given by:

$$i = -q_m^2 + 2q_m + 2\frac{C_{si}}{C_{ox}}\, ln\left(1 - q_m \cdot \frac{C_{ox}}{2C_{si}}\right)\Bigg|_{q_{mD}}^{q_{mS}} \tag{3.1}$$

where the current normalizing factor is

$$I_s = 4C_{ox}U_T^2\frac{W}{L} \tag{3.2}$$

having

$$W = n_{fin}\left(2H_{fin}\right) \tag{3.3}$$

with the normalized charge $q_m = \frac{Q_m}{Q_0}$, the charge normalizing factor $Q_0 = 4C_{ox}U_T$ and the mobile charge given by $Q_m = 2Q_G$. C_{si} is the silicon fin capacitance, C_{ox} the gate dielectric capacitance and $U_T = \frac{k_BT}{q}$ the thermal voltage, with k_B the Boltzmann constant, T the temperature in Kelvin and q the electronic charge. The most important point to note regarding the EKV double-gate model is the similarity between this proposal and the planar MOSFET model regarding the normalizing factors (SALLESE et al., 2003). Both Q_0 and I_s are expressed, in the planar model, as half the value of the double-gate model counterparts. This implies that the formulations of equations for the EKV model assumes that a FinFET device acts essentially as two independent planar devices.

The short channel effects are expressed through the subthreshold slope degradation factor n and the threshold voltage roll off ΔV_{th}. The subthreshold slope degradation factor n is given by

$$n = \frac{dv_g}{d\varphi C_{min}} = 1\bigg/\left[1 - 2sinh\left(\alpha_n \cdot \frac{L}{l}\right)\bigg/sinh\left(\frac{L}{l}\right)\right] \tag{3.4}$$

with

$$l = \sqrt{\frac{\varepsilon_{si}W_{si}t_{OX}}{2\varepsilon_{OX}}\left(1 + \frac{\varepsilon_{OX}W_{si}}{4\varepsilon_{si}t_{OX}}\right)} \tag{3.5}$$

where l is the natural length, that controls the subthreshold behaviour for small geometry structures and α_n is the location of the minimum potential across the channel, and is fixed as 0.6 based on comparisons with 3-D simulations. W_{si} is the fin thickness, referred in this work as T_{fin}, which was kept in this style to maintain the original formulation as in (TANG et al., 2009). ε_{si} and ε_{OX} are the silicon and dielectric relative permittivity, respectively.

The threshold voltage roll off is modelled based on SCE and DIBL parameters as

$$\Delta v_{th} = 2\gamma_{SCE}\left(v_{bi} - \phi_f - v_{to}\right) + \gamma_{DIBL}v_{ds} \tag{3.6}$$

where v_{bi} is the built in potential between the source and the silicon body, ϕ_f is the normalized Fermi potential, v_{to} is the normalized threshold potential for the long channel device, and v_{ds} the normalized voltage between drain and source. The generic relationship for γ is valid for both SCE and DIBL α parameters, as

$$\gamma_i = \frac{1}{\alpha_{i1}cosh\left(\frac{\alpha_{i2}L}{l}\right)} + \alpha_{i3}\left\{1 - 0.00055\left[(L-100) + \sqrt{(L-100)^2}\right]\right\} \tag{3.7}$$

for $i = SCE$ or $DIBL$.

The threshold voltage roll off is integrated into the calculation of the normalized drain current by changing the charge calculation function to

$$qm_0 = f(v_{gs}, v_{d,s}) \text{ and } qm = f(v_{gs} - \Delta v_{th}, v_{d,s}) \tag{3.8}$$

and the subthreshold slope degradation n is used to define

$$v = \frac{v_{gs} - v_{to}}{n} - v_{d,s} \tag{3.9}$$

which is in turn used to calculate the normalized charge, as defined in (PRÉGALDINY et al., 2006). In strong inversion, which is expressed by the quadratic charge term of the drain current, the value of n is set to 1 to prevent errors.

The new relationship for the drain current is thus given by

$$i = -q_{m0}{}^2(v_{gs}, v_{ch}) + 2(v_{gs} + \Delta v_{th}, v_{ch}) + 2\frac{C_{si}}{C_{ox}} ln \left(1 - q_m(v_{gs} + \Delta v_{th}, v_{ch}) \cdot \frac{C_{ox}}{2C_{si}} \right) \Bigg|_{q_{mD}}^{q_{mS}} \tag{3.10}$$

where $v_{ch} = v_d$ for q_{mD} and $v_{ch} = v_s$ for q_{mS}.

The model assumes that the mobility is kept constant, which cannot be proven for real devices with narrow fins, specially when several scattering parameters act simultaneously (GÁMIZ; GODOY, 2008). The simplistic modelling is more focused on designer accessibility than on physical correctness, even though the group calls it a *physics-based model* (YESAYAN et al., 2011).

3.2 BSIM-CMG

The BSIM-CMG was formulated in (DUNGA et al., 2007; DUNGA, 2008; DUNGA et al., 2008) and afterwards expanded in (LU et al., 2010; LU, 2011; CHAUHAN et al., 2011). As a surface potential-based model, the currents, charges and capacitances are obtained after the surface potentials at the source and drain are calculated. Its structure is illustrated in Fig. 3.1, presented in (PAYDAVOSI et al., 2013). The core model is formulated for a long channel double-gate device. Gate poly depletion (PDE), quantum mechanical (QME) and short channel effects (SCE) are introduced in this core model, while the other real device effects are used in the carrier transport equations. In order to correctly model the devices behaviour and the mentioned effects, the BSIM-CMG has over 150 parameters, divided in device and process parameters, model controllers, physical parameters such as velocity saturation and DIBL, scaling parameters for the correct modelling of the length dependent quantities, and fitting or smoothing parameters. With all the effects considered, the BSIM-CMG qualifies less as a compact model

and more as a semi-empiric model, with a large parameter set to describe currents and charges.

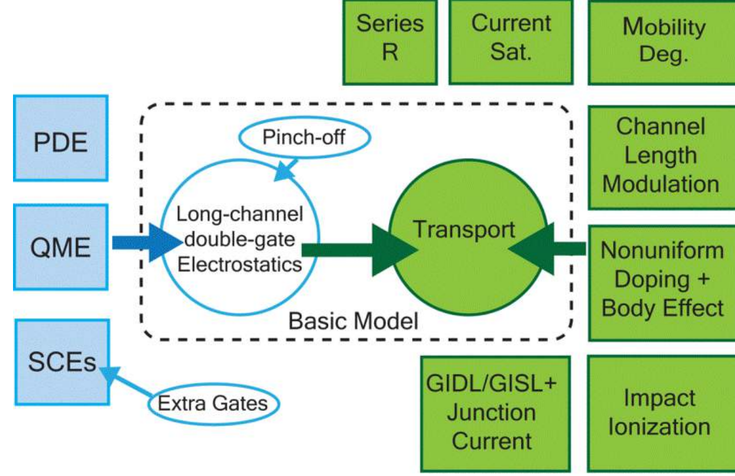


Figure 3.1: Simplified structure of the BSIM-CMG model, from (PAYDAVOSI et al., 2013)

The model is based on surface potential calculations to obtain the device behaviour. This is an important change of formulation from the early planar models of the BSIM family, that were based on the threshold voltage and employed smoothing functions (SHEU et al., 1987). This design decision is done in order to have continuous and smooth equations for all the operation regions.

The I-V model of the BSIM-CMG, after derivation of the Poisson's equation is given by

$$I_d = \mu \frac{W_{eff}}{L} [f(\psi_{s,s}) - f(\psi_{s,d})] \tag{3.11}$$

where the terms $f(\psi_{s,s})$ and$f(\psi_{s,d})$ are expressed as

$$f(\psi_s, s(d)) = \frac{Q_{inv,s(d)}^2}{2C_{ox}} + 2\frac{k_B T}{q} Q_{inv,s(d)} - \frac{k_B T}{q} \left(5C_{si} \frac{k_B T}{q} + Q_{bulk} \right) \\ .ln \left(5C_{si} \frac{k_B T}{q} + Q_{bulk} + Q_{inv,s(d)} \right) \tag{3.12}$$

The inversion and bulk charges are

$$Q_{inv,s(d)} = C_o x \left(V_g - V_{fb} - \psi_{s,s(d)} \right) - Q_{bulk} \tag{3.13}$$

and

$$Q_{bulk} = \sqrt{2qN_a \epsilon_{si} \psi_{pert}} \tag{3.14}$$

μ is the electron mobility, $W_{eff} = n_{fin} (2H_{fin} + T_{fin})$ the effective channel width, and again, C_{si} is the silicon fin capacitance, C_{ox} the gate dielectric capacitance, k_B is the Boltzmann constant, T the temperature in Kelvin, and q the electronic charge.

The equations denote a strong reliance on the charge model, used in previous BSIM for-

mulations (for planar devices). However, it is important to note the surface potential terms for source ($\psi_{s,s}$) and drain ($\psi_{s,s}$) in the inversion and bulk charge equations. ψ_{pert} is a perturbation due to body doping of the device. This correction allows the model to account for both fully doped and undoped devices as well as SOI and bulk FinFETs.

The model employs the concept of length dependent quantities (SRIRAMKUMAR et al., 2013), for mobility related (U0[L], ΔL[L], UA[L], UD[L], RDSW[L]), velocity saturation (VSAT[L], VSAT1[L], PTWAG[L]), and smoothing parameters (MEXP[L]), which enables a global modelling. The intermediate quantities U0[L] and ΔL[L] are defined as

$$U0[L] = U0_0 \times \left(1 - UP \times {L_{eff}}^{LPA}\right) \tag{3.15}$$

$$\Delta L[L] = LINT + LL \times e^{\frac{-(L+XL)}{LLN}} \tag{3.16}$$

the smoothing function MEXP[L] is given by

$$MEXP[L] = MEXP_0 + AMEXP \times {L_{eff}}^{-BMEXP} \tag{3.17}$$

and the other length dependent quantities have identical function form, represented as

$$Param[L] = Param_0 + AParam \times e^{\frac{-L_{eff}}{BParam}} \tag{3.18}$$

for example,

$$UA[L] = UA_0 + AUA \times e^{\frac{-L_{eff}}{BUA}} \tag{3.19}$$

Although essential for the correct modelling of a wide range of devices with different geometries, these length dependent quantities are notably difficult to accurately extract, in order to reflect the characteristics of all devices at the same time. It is also important to note the strong dependence of the scaling function of the value of L_{eff}, which leads to the extreme importance of the correct extraction of ΔL for the transistors. With an incorrect extraction of ΔL, the modelling of the length dependent quantities is impaired.

The very large number of model parameters renders difficulties in the device extraction. Nevertheless, it enables the description of an ample set of real device characteristics, such as gate-induced drain leakage and vertical field dependent carrier mobility, in addition to subthreshold slope degradation and DIBL (CHAUHAN et al., 2011). The BSIM-CMG model is already implemented and functional in commercial circuit simulators such as SPECTRE and HSPICE, which simplifies its parameter extraction.

3.3 PSP-DGFET

The PSP planar model (GILDENBLAT et al., 2006; SMIT et al., 2013) is hierarchically structured in two levels: the global level, that models geometry scaling effects, and the local level, with parameters that affect the electrical characteristic of devices with specific dimensions. Figure 3.2 presents the simplified model structure.

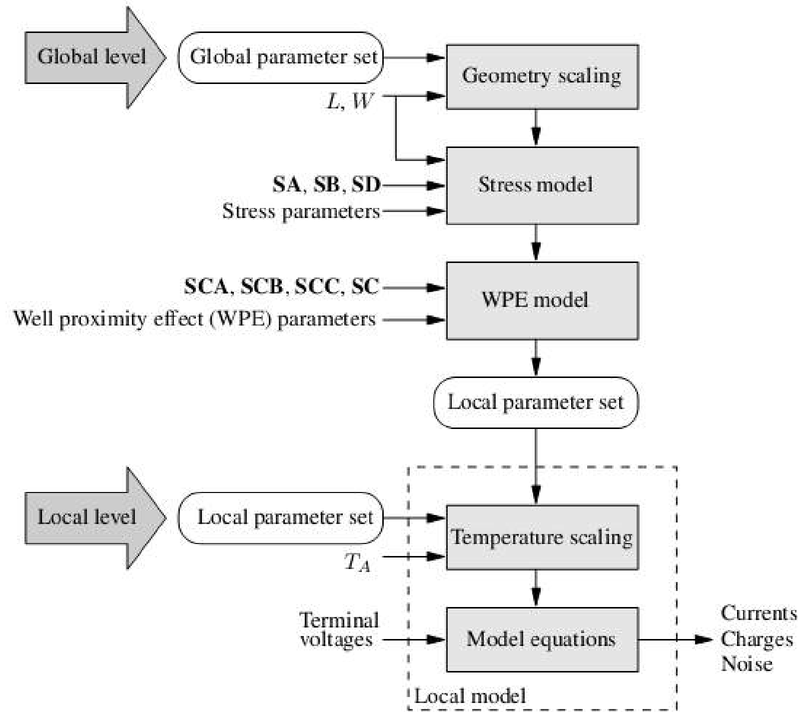


Figure 3.2: Schematic of the PSP model structure (GILDENBLAT et al., 2006)

The PSP-DGFET (SMIT et al., 2006; SMIT et al., 2007; DESSAI et al., 2009), for multi-gate devices, is a surface potential compact model that follows the same basic structure and formulation of its planar counterpart. The model assumes an undoped or lightly doped silicon channel, and ignores the edge effects in the fin corners.

The equation for the drain current is:

$$I_d = \mu \frac{W}{L} C_{ox}(v + 2\phi_t)\Delta\psi \tag{3.20}$$

with the coefficient v selected as

$$v = 2k_B V_{oxm} \tag{3.21}$$

where V_{oxm} is the oxide voltage where the surface potential has its medium value, k_B is the Boltzmann constant, C_{ox} is the oxide capacitance, $\phi_t = \frac{k_B T}{q}$ is the thermal potential (referred previously in this work as U_T) and $\Delta\psi$ the variation of the surface potential across the channel,

which is formulated as

$$\Delta\psi = \psi_{sd} - \psi_{ss} \tag{3.22}$$

where

$$\psi_s(y) = \psi_m + H\left[1 - \sqrt{1 - (2\Delta\psi/HL)\,(y - y_m)}\right] \tag{3.23}$$

The gate charge for the PSP-DGFET is given by

$$Q_G = 2C_{ox}WL\left(V_{oxm} + \frac{\Delta\psi^2}{12H}\right) \tag{3.24}$$

Similarly, the total drain charge is

$$Q_D = -2C_{ox}WL\left[\frac{V_{oxm}}{2} - \frac{\Delta\psi}{12}\left(1 - \frac{\Delta\psi}{2H} - \frac{\Delta\psi^2}{20H^2}\right)\right] \tag{3.25}$$

The coefficient H is given by $H = V_{oxm} + \phi_t$. Only this coefficient is different, comparing to the planar PSP model. The equations and structure are the same. This makes the adoption of the PSP-DGFET easier, because the code already published for the planar model can be modified and used for the double-gate model. Also, this means that the short channel effects can be added in the PSP-DGFET model in the same way they are added in the conventional PSP. The parameter extraction methodology is also very similar. The small number of publications regarding the specific DGFET model is a drawback, even considering the argument that the model is very similar to the planar PSP model.

4 PARAMETER EXTRACTION

A parameter extraction methodology can be aimed either at determining the electrical parameters of a device, such as threshold voltage and series resistance, or at obtaining a set of model parameters, in order to accurately simulate the extracted device. In the first case, known methodologies are used, such as (SUCIU; JOHNSTON, 1980) and (WONG et al., 1987), and the electrical parameters obtained by manipulations and fittings on the measured DC I-V or C-V curves of one or more devices. The objective, in general, is to quantitatively assess the electrical characteristics of the transistors, so as to compare different device architectures or technologies.

The model parameter extraction, in the other hand, uses several devices, with different geometries and in all operation regions, in order to extract the parameters that will be used by the device model in the simulation. It is usually composed of a set of steps such as parameter initialization and optimizations with different channel lengths and bias regions. In the studied compact models, the parameters have strong physical meanings, thus selecting a setup where the given physical characteristic is dominant is the key to properly extract and optimize the parameters. A common parameter extraction run, as illustrated in Figure 4.1, starts by plotting the measured data in a specific setup and simulating the compact model with default (or an association of default and already extracted) parameters. The parameters to be extracted in the given step are then iteratively changed, and the model simulated again, until a good fitting is achieved between the model and the original data, and the error minimized. This optimizations can be done either manually or automatically.

4.1 Threshold Voltage and Subthreshold Slope

The assessment of the threshold voltage in FinFET devices is an important measure of process quality. Since FinFET devices have undoped channel, the threshold voltage is mainly controlled by the gate electrode work function (NOWAK et al., 2004). The determination of V_{th} is also essential for the extraction of other parameters, such as the series resistance and channel length reduction, to be discussed in the following section. Those parameters are usually extracted using the gate voltage overdrive ($V_{GS} - V_{th}$), rather than the gate voltage V_{GS}. Finally, the extraction of this parameter is also a reliable way to analyse drain induced barrier lowering (DIBL) effects in short channel devices. This is done by calculating the V_{th} roll off, or how much the V_{th} lowers in short channel devices, in comparison to the long channel V_{th}. The extraction of the threshold voltage in this work is performed using the second derivative method, proposed in (WONG et al., 1987). It defines the value of V_{GS} where the function $\frac{\partial^2 I_{DS}}{\partial V_{GS}{}^2}$ has its maximum. It was used in the PhD thesis of (FERREIRA, 2012) and considered a reliable method for the V_{th} extraction.

The subthreshold slope S – also referred as subthreshold swing – of a transistor, in the weak

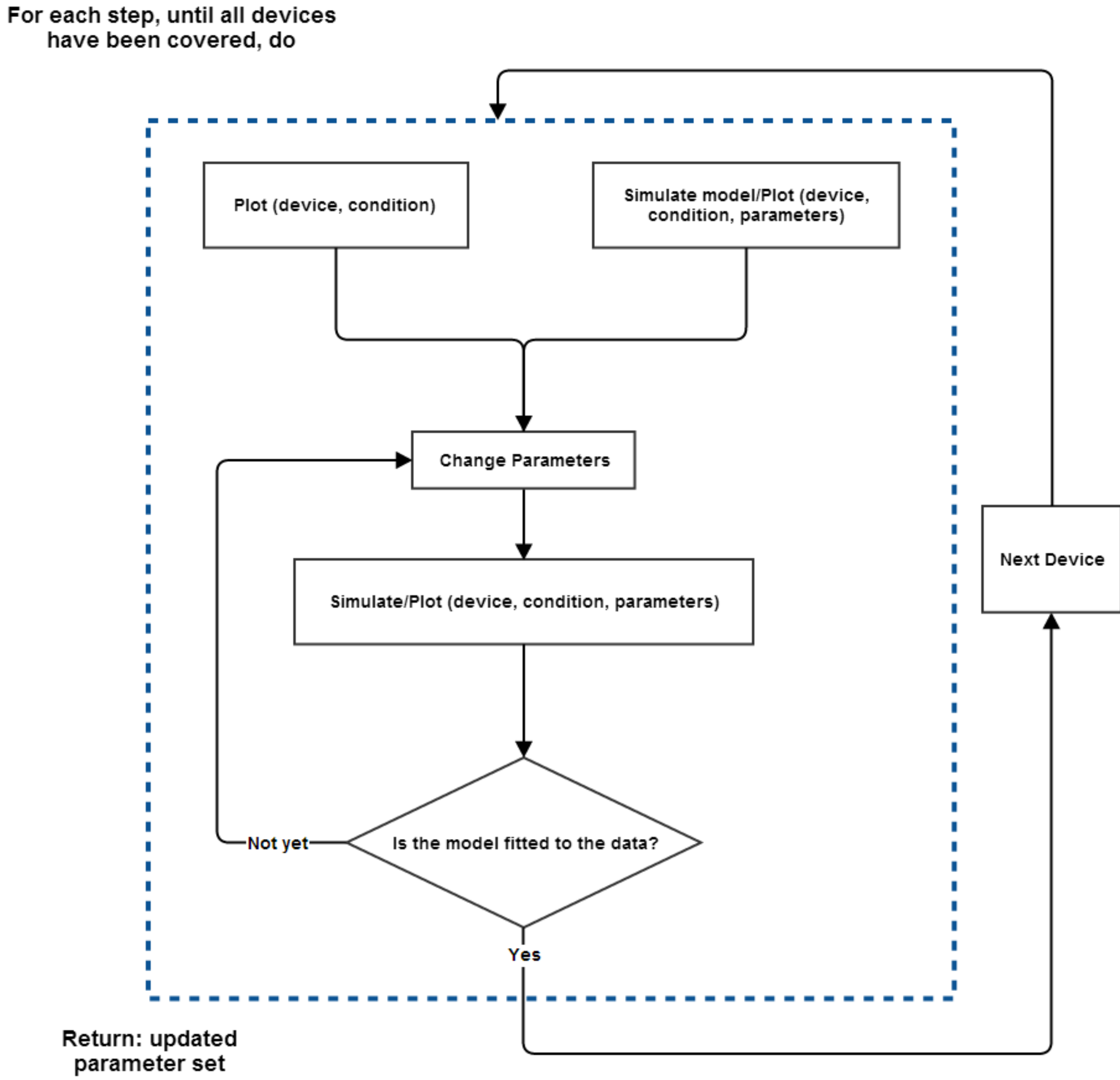


Figure 4.1: Flowchart for each step of a general device model parameter extraction procedure.

inversion regime, is given by (SZE, 1981; COLINGE, 1986)

$$S \simeq \frac{kT}{q} ln \left(10 \frac{C_{ox} + C_D + C_{it}}{C_{ox}} \right) \tag{4.1}$$

where C_D is the depletion capacitance, C_{it} the interface trap capacitance and C_{ox} the gate oxide capacitance. The minimal theoretical limit is 59.6 mV/decade at T=300K, where $S = \frac{kT}{q} ln(10)$, where the capacitance terms C_{it} and C_D approach zero. Thin film transistors, such as SOI MOSFETs and FinFETs can present optimum subthreshold slope characteristics even for sub 100-nm gate length devices if the depletion capacitance is maintained small enough and the gate oxide capacitance is high. The subthreshold slope is defined such as $S \equiv \Delta V_G / decade I_D$, which is extracted from the measured DC I-V data by the linear fitting of the subthreshold region, in logarithmic scale (log_{10}). The final value is given by the slope of the fitted line, resulting in $S = 1/Slope$. The subthreshold slope is commonly extracted for several devices and plotted

against the gate length of the devices, in order to assess the variation of subthreshold slope characteristics with the reduction of length, which indicates the severity of the short channel effects in the set of devices.

4.2 Series Resistance and Effective Length

A paper on extrinsic device parameters was submitted by the author to the International Symposium on Circuits and Systems - ISCAS, 2015 (currently under review). The source and drain regions of a MOSFET device present an associated resistance – known as series resistance – which induces a voltage drop when the current flows through them. Since the transistor channel cannot be directly probed, only through the source and drain contacts, this voltage drop has to be taken into consideration when determining the "intrinsic", or effective, characteristics of the device. These voltage drops are usually modelled considering the series resistances as external components to the intrinsic transistor.

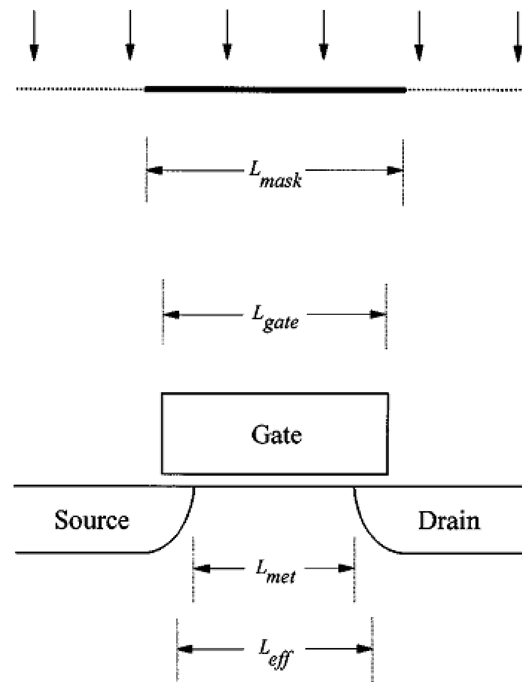


Figure 4.2: Schematic of the relationship between the different terms for the channel length, in a planar MOSFET (TAUR, 2000).

Similarly, the nominal mask length of a MOSFET device, either planar or FinFET, is not the effective channel length. The work presented in (TAUR, 2000) discusses the differences between the mask length, the gate length, the metallurgical length and the effective channel length. Fig. 4.2, extracted from the referenced work, shows the schematic of the relationship between the different terms of channel length. The most relevant quantities for this report are the mask length L_{mask} – the designed length in the etch mask, used in the fabricated process – and

the effective channel length L_{eff} – not a strictly a physical quantity, but qualitatively defined as the measure of how much gate-controlled current a MOSFET delivers in comparison to the long-channel device. The relationship between L_{mask} and L_{eff} is very complex, being influenced by the device structure, the fabrication process and related parameters, the abruptness of the source and drain junctions, among other characteristics. The effective channel length, however, is a key parameter to be extracted, in order to analyse the effective device characteristics and specially to properly compare different MOSFET devices regarding short channel effects, current drive and others.

Several extraction methods for the source and drain resistance have been developed and are reviewed in (TERADA; MUTA, 1979; SCHRODER, 2005; SáNCHEZ; ORTIZ-CONDE; LIOU, 1999). The extraction methodology has to be chosen considering its applicability for the given technology, especially if the assumptions on which it relies can be proven for the devices. Another issue is that the series resistance and the effective channel length have mutual dependence on the device behaviour. Thus, if the extracted value of one parameter is underestimated, the other cannot be properly extracted as well.

The Suciu-Johnston (SUCIU; JOHNSTON, 1980), Campbell et al. (CAMPBELL et al., 2011) and Torres-Torres (TORRES-TORRES; MURPHY-ARTEAGA, 2002) methods are explored for their proposed merits in terms of reproducibility, simplicity or accuracy in extracting the parameters from LDD devices.

4.2.1 Suciu-Johnston

The Suciu-Johnston methodology (SUCIU; JOHNSTON, 1980) has been proposed in 1980 and is still used as a way to extract both the source/drain resistance and the mobility degradation. The method uses at least two devices of different mask channel length but the results are significantly more reliable if more than two channel lengths are used in test transistors. The parameter E 4.2 is plotted as a function of the gate voltage overdrive $V_{GS} - V_{th}$ for the different devices, and then $1/\beta_0$ is extracted for each. The value of $1/\beta_0$ is given by the linear extrapolation of E, where $V_{GS} - V_{th} = 0$. The value of E shows a linear behaviour in the high gate voltage overdrive region only, and thus needs to be extrapolated only considering this region.

$$\frac{(V_{GS} - V_{th})}{I_{DS}/V_{DS}} = \frac{1 + A(V_{GS} - V_{th})}{\beta_0} \equiv E \tag{4.2}$$

where V_{DS} is the voltage between drain and source, V_{GS} the voltage between gate and source and V_{th} the threshold voltage. These parameters are the same for all the following methodologies.

The second step of the method is to plot the slope of the linear fitting of E against $1/\beta_0$,

since

$$\frac{dE}{dV_{GS}} = \frac{A}{\beta_0} = R_{DS} + \frac{\theta}{\beta_0} \tag{4.3}$$

which in turn provides the source and drain resistance R_{DS} as the intercept of the resulting straight line and the mobility degradation factor with transversal electric field (parameter θ) as the slope.

4.2.2 Campbell et al

The methodology proposed in (CAMPBELL et al., 2011) uses the same device in two different – but very close – drain biases in order to obtain the series resistance as a function of the gate voltage overdrive. The extraction relies the on ratio of two $I_D - V_G$ curves

$$\frac{I_{D1}}{I_{D2}} = \frac{\mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} \left(V_{GS} - V_{th1} - \frac{I_{D1} R_{SD}}{2}\right) \left(V_{D1} - I_{D1} R_{SD}\right)}{\mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} \left(V_{GS} - V_{th2} - \frac{I_{D2} R_{SD}}{2}\right) \left(V_{D2} - I_{D2} R_{SD}\right)} \tag{4.4}$$

where the constants μ_{eff}, C_{OX}, W_{eff} and L_{eff} can be cancelled, since the measurements are made in the same device, yielding

$$R_{SD}^2 \left(\frac{I_{D2} - I_{D1}}{2}\right) + R_{SD} \left(V_{th2} - V_{th1} + \frac{V_{D1} - V_{D2}}{2}\right) - \frac{\left(V_{GS} - V_{th1}\right) I_{D2} V_{D1} - \left(V_{GS} - V_{th2}\right) I_{D1} V_{D2}}{I_{D1} I_{D2}} = 0 \tag{4.5}$$

The source and drain resistance values are obtained after solving the polynomial equation. The method does not give a single value for the source and drain resistance, but its relationship with the gate voltage. A single value should be extracted from these curves at a very high gate voltage, as discussed in (DIXIT et al., 2005).

4.2.3 Torres-Torres

The Torres-Torres methodology (TORRES-TORRES; MURPHY-ARTEAGA, 2002) was specifically designed for LDD devices, considering the dependence of the series resistance and effective channel length on the gate bias, as discussed in a previous chapter. The main formulation of the methodology is to iteratively update both the channel length reduction ΔL and R_{SD}, which are calculated in every iteration from the plot of the total resistance R_T as a function of a parameter K, where

$$K = \frac{1 + \theta \left[V_{GS} - V_{th} - 0.5 \left(\frac{R_{SD}}{m L_{mask} + b}\right) V_{DS}\right]}{G \left(V_{GS} - V_{th} - 0.5 V_{DS}\right)} \tag{4.6}$$

$$R_T = ML_{mask} + b \tag{4.7}$$

where L_{mask} is the mask channel, and M is calculated as

$$M = K + (L - \Delta L)\frac{0.5m\theta R_{SD}V_{DS}}{G(mL_{mask} + b)^2(V_{GS} - V_{th} - 0.5V_{DS})} \tag{4.8}$$

The parameters ΔL and R_{SD}, initially set as zero, are calculated in every iteration as the slope of the function R_T versus K and the intercept, respectively. After a given number of iterations, the parameters ΔL and R_{SD} no longer update their values with new iterations, and are thus defined. The values of V_{GS} have to be few and with very small increments, for the R_T function to remain linear. The extracted ΔL and R_{SD} are strongly dependent of the chosen V_{GS} bias. Several measurements at different V_{GS} biases are required in order to extrapolate a single value at very high V_{GS}.

The Torres-Torres method depends on the value of the low field mobility μ_0 and mobility degradation parameter θ, for the determination of the gain factor $G = \mu_0 C_{OX} W$. These constants have to be both obtained with a different extraction methodologies.

4.3 EKV Double-Gate Parameter Extraction Methodology

The EKV double-gate MOSFET model has a simple formulation with a reduced parameter set, as discussed. The parameter extraction methodology is thus supposedly less complicated, since only the parameters for quantum mechanical, short channel effects and DIBL have to be extracted from the data (CHEVILLON et al., 2009). The other parameters are calculated based on process and device data. Fig. 4.3 presents the parameter extraction procedure of the EKV Double-Gate model, in a simplified manner.

The quantum mechanical functions $\alpha_{qm1,2,3}$, SCE functions $\alpha_{SCE1,2,3}$, DIBL funtions $\alpha_{DIBL1,2,3}$ and carrier velocity saturation parameter v_{sat} are extracted using the following methodology:

Step 1 Geometry and technology parameters are set according to the measured devices (such as gate length, oxide thickness, fin thickness) and parameters to be extracted are set to default values.

Step 2 Quantum mechanical functions are extracted. Long channel devices in all range of fin thickness are used. This work will not cover the quantum mechanical effects proposed in (CHEVILLON et al., 2009), however. This step will be skipped.

Step 3 SCE α_{SCE3} and DIBL α_{DIBL3} functions are simultaneously extracted, with devices with medium gate length in all range of fin thickness. FinFETs with 130nm mask length were

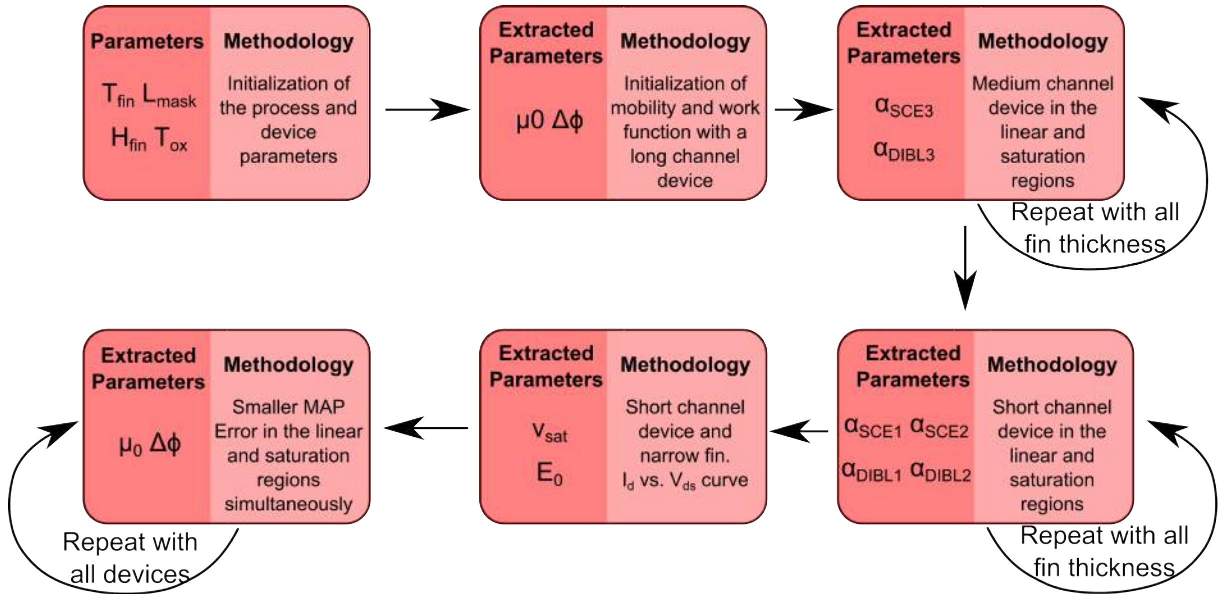


Figure 4.3: Simplified flow of the parameter extraction procedure for the EKV Double-Gate model

used. This step requires a plot of the Log(I_d)vs. V_{gs} curves in weak inversion, with low V_{ds} to optimize α_{SCE3} and with high V_{ds} to optimize α_{DIBL3}. These functions are associated to the threshold voltage roll off due to silicon fin thickness.

Step 4 SCE $\alpha_{SCE1,2}$ and DIBL $\alpha_{DIBL1,2}$ functions are simultaneously extracted using short channel (L_{mask} = 70nm) devices in all range of fin thickness. In this step, the curves for Log(I_d)vs. V_{gs} are plotted. Again the bias conditions are weak inversion and low V_{ds} to optimize $\alpha_{SCE1,2}$ and with high V_{ds} to optimize $\alpha_{DIBL1,2}$. The four functions change together the voltage threshold, so must be optimized simultaneously. Those functions, however, have a stronger impact in short channel devices.

Step 5 Carrier velocity saturation parameter v_{sat} is extracted, with very short channel and narrow fin devices. This parameter has an impact on the channel length modulation and is thus optimized with the I_d vs. V_{gs} curve in the saturation region and high V_{gs} bias.

The papers (SALLESE et al., 2005) and (CHEVILLON et al., 2009) assert that after the steps are performed and the functions and parameters are correctly extracted, the EKV double-gate compact model should ready to describe a wide set of devices in all operating regions.

An important issue with the proposed extraction procedure is that the low field mobility is set in the initialization step and considered constant for all fin thickness and all channel lengths. This is rather optimistic, if not totally inconsistent, specially considering that the EVK Double-Gate does not propose any scattering or mobility reduction effects which might scale with channel length. In order to achieve more consistent results, the low field mobility is determined individually for each device.

The work function difference between the gate electrode and intrinsic silicon $\Delta\phi$ is used to determine the effective gate voltage $v_g* = v_g - \Delta\phi$ and most importantly, when calculating the normalized long channel threshold voltage given as

$$v_{to} = \frac{\Delta\phi}{U_T} - ln\left(\frac{q.ni.t_{si}}{8.U_T.C_{Ox}}\right) \tag{4.9}$$

The parameter extraction procedure was thus modified, and the new proposed parameter extraction follows the steps to extract DIBL and SCE parameters, and then introduces a new step, where for each device the low field mobility μ_0 and the work function difference between the gate and channel $\Delta\phi$ are extracted, using the linear and saturations regions simultaneously. The mean absolute percentage (MAP) error is used as the metric to identify the best combination of μ_0 and $\Delta\phi$. This parameters are used in order to achieve a better fitting between the model and the measured data, since the EKV Double-Gate presents several issues already discussed. A trend can be thus obtained for the parameters in order to determine a formulation for μ_0 and $\Delta\phi$ as a function of the fin thickness and mask gate length. Step 5 is also modified to extract the effective field parameter E_0, that has a high influence in the saturation region current and is very difficult to be properly defined beforehand.

4.4 BSIM-CMG Parameter Extraction Methodology

The parameter extraction methodology of the BSIM-CMG model is explained in the technical manual for the latest release (SRIRAMKUMAR et al., 2013), while the original work is presented in (YAO et al., 2010). The very large set of parameters used in the BSIM-CMG, while allowing for a rather accurate modelling, also render the parameter extraction procedure lengthy and complicated. The simplified flow, showing the extraction stages and the steps of each stage, is presented in Fig. 4.4. Small changes are proposed to the original extraction flow, since strictly following the parameter extraction procedure results in large inaccuracies in the modelled device output, specially when extracting a parameter set for a wide range of FinFET geometries. This is because the length dependent variables are rather difficult to accurately define, such as to agree with the whole set of devices. In order to mitigate this issue, a weighted parameter extraction methodology was developed. An article presenting and discussing the BSIM-CMG parameter extraction, along with the proposed modifications was submitted to the Latin American Circuits and Systems Conference – LASCAS, 2015.

Proposed changes to the flow are schematically presented in Fig. 4.7. The key aspect of the proposed changes to the extraction is to evaluate the whole set of devices every few updates in parameter values, such as to guarantee that the modelling is still consistent with both long- and short-channel FinFETs. The length dependent quantities are specially delicate and should be accurately extracted. To ensure their correctness, previous steps from the extraction procedure might need to be performed again, as shown in Fig. 4.5 and Fig. 4.6. The parameter

extraction flow becomes more cyclic and lengthy, since the refinement steps are performed alongside the process, not only in the final steps. This, however, ensures that the extracted parameters are consistent with the whole set of devices, thus rendering a global parameter set that can adequately model all devices of a given technology.

Fig. 4.5 details the steps on the parameter extraction stage that only uses measured data in the linear region of the transistor operation, where $V_D = 50mV$ for all plots. The arrows indicate the extraction flow, with the downward facing arrows indicating the original extraction flow, while the proposed changes are mainly expressed by the cyclic nature of the upwards facing arrows, that indicates that a certain step has to be performed again.

Fig. 4.6 details the steps for both the saturation region parameter extraction stage and for the extraction using $I_D x V_D$ measured data. In the saturation region, all plots are presented using data where the drain FinFET bias is 1V. Again, the arrows indicate the proposed extraction flow. It should be noted the strong dependence between the saturation region and the $I_D x V_D$ stages. After the saturation region stage has extracted satisfying parameters, the $I_D x V_D$ stage steps start, but after the last step the flow goes back to the velocity saturation extraction. This cycle is repeated until the devices present an accurate modelling and the mean average percentage (MAP) error is minimized for both operation regimes.

The parameters are divided in Group A and Group B, where Group A (also called Category One parameters in the technical manual) are used to define nine length dependant intermediate quantities, and Group B (mentioned as Category Two) can be extracted directly from the experimental data.

The parameter extraction for the BSIM-CMG can be divided in four stages, as shown in Fig. 4.4, namely parameter initialization, linear region extraction, saturation region, and a stage that used $I_D x V_D$ data with different V_G biases to extract parasitic and smoothing parameters. The details of the procedure will be explained.

Stage 1 Parameter initialization using process characteristics of the fabricated FinFETs and extrinsic device parameters extraction. The channel length reduction, extracted with an appropriate method, is used to determine the parameter LINT such as that $\Delta L = 2LINT$. The series resistance R_{SD} is obtained using the methods discussed previously the parameter RDSW set accordingly.

$\Delta V_{th}(L)$ at V_{DS} = 50mV and at V_{DS} = 1V are extracted for both measured and simulated curves, using the methods discussed in the previous sections, and plotted against the devices mask length, in order to extract short channel effect and DIBL parameters. The subthreshold slope at V_{DS} = 50mV and at V_{DS} = 1V is also extracted for measured and simulated curves as previously discussed and used to extract other SCE and DIBL parameters. All other parameters are reset to the default values shown in the BSIM-CMG technical manual.

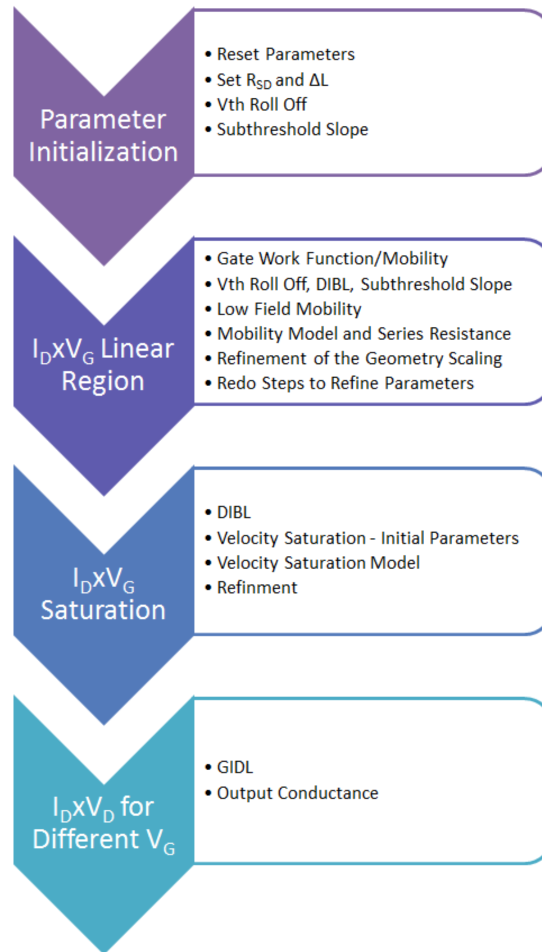


Figure 4.4: Simplified flow of the parameter extraction procedure for the BSIM-CMG model

Stage 2 Extraction and optimization of parameters in the linear region, with V_D = 50mV, using devices with different lengths. Fig. 4.5 illustrates the steps of this stage. First, the parameters related to the gate work function (PHIG), low field mobility ($U0_0$), effective field (ETAMOB), interface trap (CIT) and scattering (UA, UD, EU) are extracted, using long channel devices. For this extraction, the $I_D x V_G$ curve at V_D = 50mV is evaluated in subthreshold region, using the logarithmic scale and in the strong inversion with both linear scale and $G_m x V_G$ plots. The gate work function is evaluated in the subthreshold region, low field mobility specially in the strong inversion and the other parameters to accurately model the $G_m x V_G$ plot.

The threshold voltage roll-off, DIBL and subthreshold slope parameters are then refined with the $I_D x V_G$ curve at V_D= 50mV for short and medium devices. The curve is evaluated in the subthreshold region. As expected, the short channel device modelling is much more influenced by those parameters than the medium devices.

Now the length dependant intermediate quantities start to be used, in order to extract the low field mobility function U0[L] for long and medium devices. The parameters UP and LPA are used in the formulation of U0[L], which dominates the current in the linear region. These parameters need to be carefully extracted, and it is essential that all devices are re-simulated

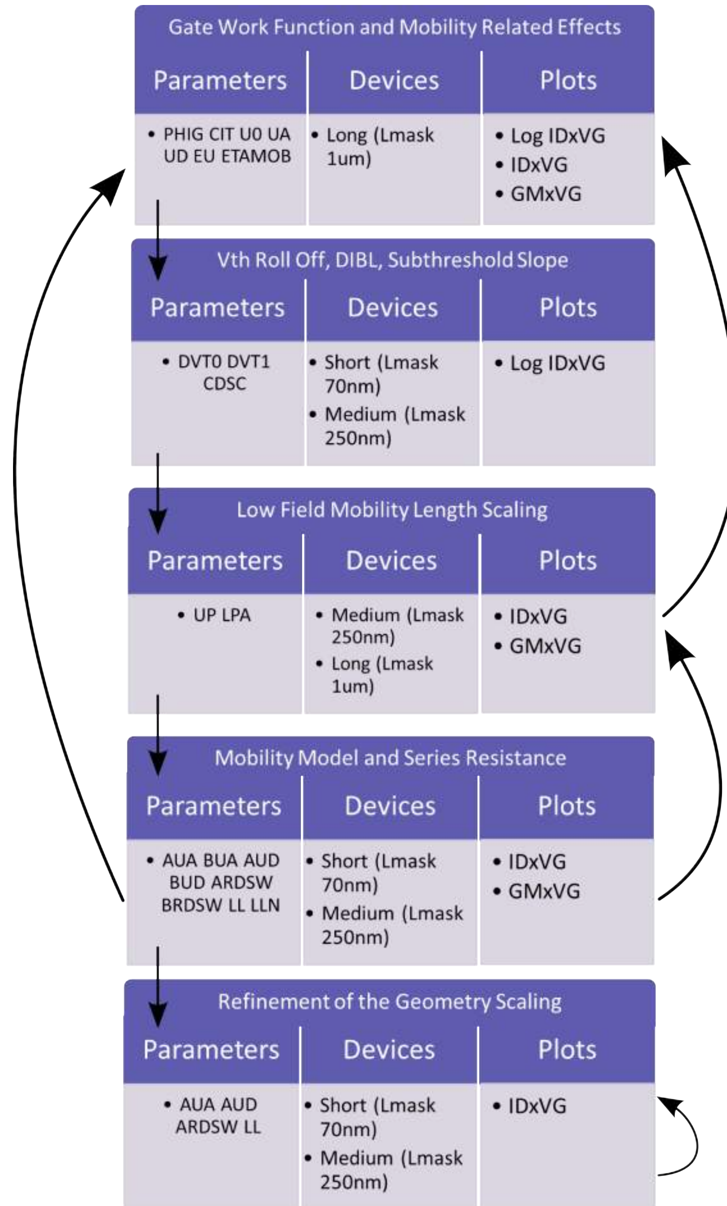


Figure 4.5: Parameter extraction flow for the linear region, for the BSIM-CMG model.

for every change in the value of the UP and LPA. If the value of U0[L] becomes too small or negative for a given mask length, the BSIM-CMG will indicate a convergence error, which is unacceptable. It is critical that the modelling of all devices in the set is consistent after this step. If no adequate modelling is achieved, the first step of this stage should be performed again, finely changing the parameter values in order to obtain better results, as shown in the cyclic iterations in Fig. 4.5.

Then, the mobility scattering and series resistance scaling parameters are extracted, using medium and short devices, in order to accurately formulate the intermediate quantities related to mobility and series resistance (UA[L], UD[L], RDSW[L] and ΔL[L]). For this step the $I_D x V_G$ and $G_m x V_G$ curves are used. This extraction is also complicated because of the scaling param-

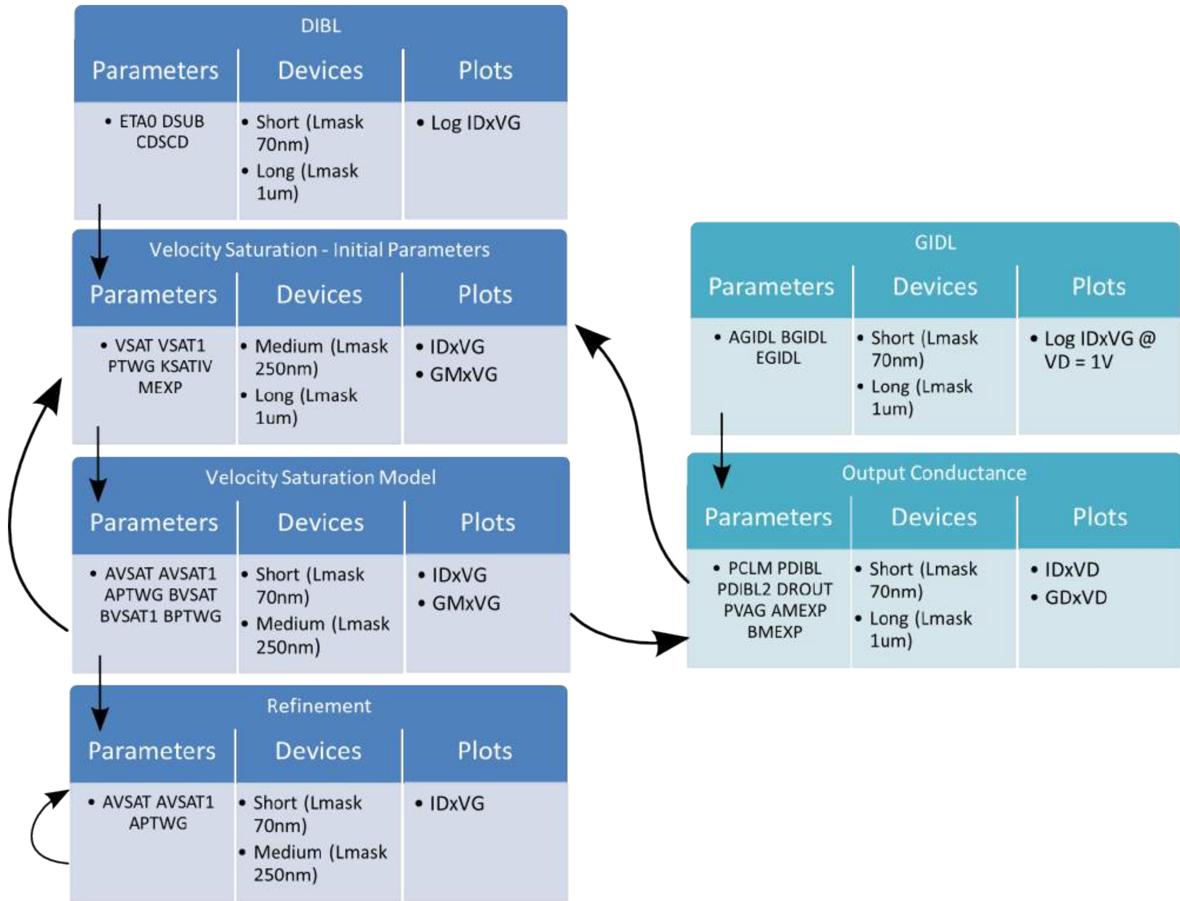


Figure 4.6: Parameter extraction flow for the saturation region and other effects, for the BSIM-CMG model.

eters, and the agreement will all devices needs to be ensured also.

The geometry scaling parameters for the mobility degradation are refined by plotting the strong inversion region for short and medium devices in the same graphic, and optimizing the parameters for all curves simultaneously.

Finally, the linear region extraction stage is ended by repeating the threshold voltage roll-off, DIBL and subthreshold slope parameters refinement step and the geometry scaling parameters for the mobility degradation refinement step. Basically this final step is performed by looping between the subthreshold and strong inversion regions, fine tuning the parameters, until the fitting is good.

Stage 3 Extraction and optimization of parameters in the saturation region, using devices with different lengths, as presented in the left side of Fig. 4.6. In this stage, the drain bias V_D is always set as 1V. This extraction begins by refining the DIBL parameters, using subthreshold $I_D x V_G$ curves for short and long devices, all in the same plot. The parameters are refined and optimized for all curves simultaneously.

Next, the velocity saturation parameters are extracted in the strong inversion region of long

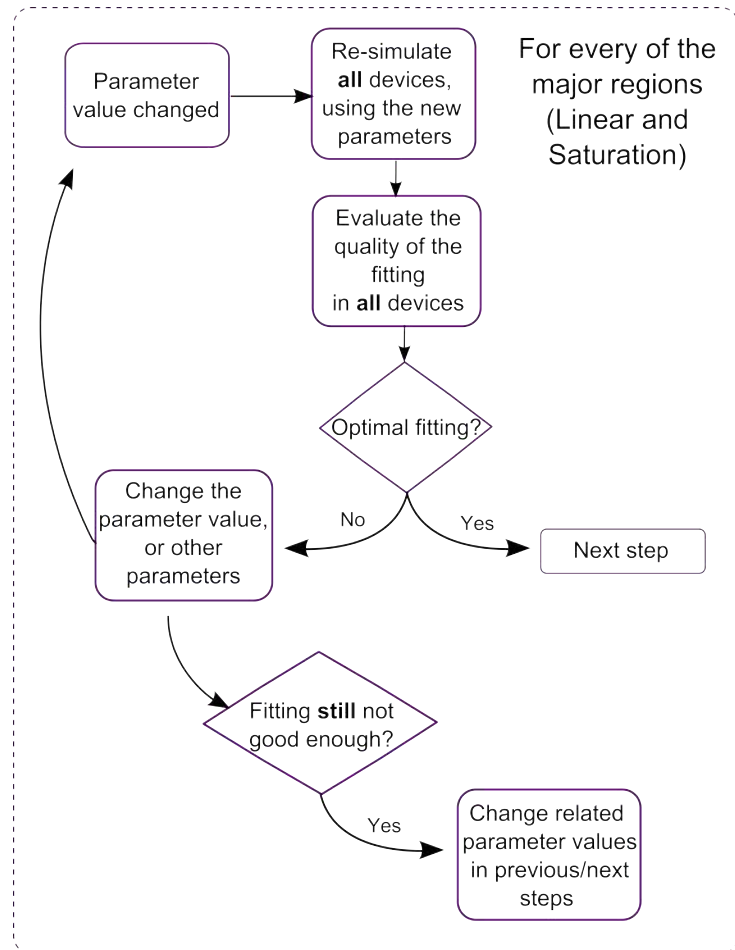


Figure 4.7: Schematic of the proposed changes to the reference BSIM-CMG extraction procedure.

and medium devices. Then, scaling velocity saturation parameters are extracted using short and medium devices. In the saturation region the drain current is dominated by the velocity saturation, and thus this extraction is specially delicate. The parameters extracted in this step and in the previous are used to formulate the velocity saturation intermediate quantities (VSAT1[L], VSAT[L] and PTWG[L]). Similar as in the linear region parameter extraction stage, the velocity saturation model has to be extracted such as to remain consistent with all devices simultaneously. This is done the same way as in the last stage, by re-simulating the model every few iterations of the parameter values. These two steps may need to be performed a few times until the modelling is consistent, as indicated in Fig. 4.6.

The geometry scaling parameters for velocity saturation are refined using short and medium devices in the strong inversion region, with all devices in the same plot (as used in other steps also).

This stage also ends with the iterative optimization of the extracted parameters in the subthreshold (DIBL parameters) and the strong inversion (velocity saturation parameters), until a good fitting is achieved for the saturation region.

Stage 4 This stage extracts other important parameters, such as GIDL and output conductance parameters, as shown in the right side of Fig. 4.6. The smoothing functions between linear and saturation regions are also addressed. The GIDL parameters are obtained by the sub-threshold region of the $I_D x V_G$ curve at saturation, for long and short channel devices. The output conductance and smoothing parameters are extracted also with short and long devices, with the $I_D x V_D$, with different V_G and with the $G_d x V_D$ curves. The smoothing length dependent quantity MEXP[L] has to be carefully extracted in order to describe the whole set of devices. In order to obtain a good fitting between the BSIM-CMG modelling of the $I_D x V_D$ curves and the measured curves, it may be necessary to refine the velocity saturation model, extracted in the previous stage, be performing again those steps. This cyclic flow is indicated by the arrows in Fig. 4.6.

The whole parameter extraction procedure need to be performed for each fin thickness group of devices separately. After all parameters have been extracted and the fitting between the simulated curves and the measured data is acceptable, a model card can be generated, providing the BSIM-CMG model parameters for further use in circuit simulation.

4.5 PSP-DGFET Parameter Extraction Methodology

The parameter extraction methodology for the FinFET PSP compact model is similar to that of the planar model, as indicated in (SMIT et al., 2007). This work will thus outline the methodology used for the PSP planar MOSFET model (GILDENBLAT et al., 2006) that can be used, with few modifications, to extract and optimize the parameters for the PSP-DGFET.

The methodology distinguished between local and global parameters. Local parameters are the ones that affect the characteristics of a single device geometry, while global parameters are used to the whole set of device dimensions. The local parameters are extracted first, and then the global parameters are extracted.

The process involves parameter initialization, extraction of local parameters at room temperature, extraction of temperature scaling parameters and finally extraction of geometry scaling parameters. Before the procedure starts, the parameters are set to initial values. The default values for local parameters are given in the PSP technical manual.

Long Channel For the local parameter extraction of long channel devices, the following steps are necessary. First, the the magnitude of the simulated I_D and the shape of the I_D - V_G is roughly set to match the measured data. Optimization of the subthreshold related parameters, neglecting DIBL. Mobility parameters are optimized, neglecting the series resistance for the moment. Velocity saturation parameter is extracted. Conductance parameters are determined based on G_m. Velocity saturation parameter is refined. Gate leakage current is obtained. Gate induced drain leakage is extracted. The final step is to loop through all steps again in order to optimize the extracted parameters.

Short Channel The parameter extraction for short channel devices then takes place. Some parameters extracted for the long channel devices are used, namely the mobility reduction and gate leakage parameters. The overall procedure is very similar to that of long channel devices. In the short channel extraction, however, the series resistance is extracted from the experimental data. DIBL parameters are also obtained in the short channel procedure.

After the parameters for the short channel device have been optimized, the extraction procedure must return to the long channel steps, in order to obtain updated values for velocity saturation and conduction parameters. The series resistance found for the short channel device should be used in this optimization of the long channel parameters.

Finally, the steps from the short channel extraction are repeated, this time using intermediate length devices. Once the parameters are properly set, the temperature scaling parameters are extracted. However, as previously mentioned, temperature effects will not be addressed in the proposed work.

Geometry Scaling Parameters Extraction of the ΔL and ΔW parameters, using an appropriate external extraction method. The geometry scaling parameter extraction takes place by first setting the global "switch" parameters to the appropriate values, and using the locally extracted values for parameters with no geometry scaling rules. This step consists of several independent sub-steps, one for each geometry dependant local parameter. The parameters are extracted using the relevant geometrical scaling rules, given in the PSP manual. This step needs modifications, due to the difference between FinFET geometry and planar devices geometry. Once all global parameters are found, optimizations can be done in the set of values. Local parameters with geometry scaling rules can be replaced by the calculated value from its global values. The local parameter extraction procedure should then be re-executed for the remaining local parameters. This optimizations are important for a good fitting between the model and the measured devices.

5 RESULTS

5.1 Experimental Devices

A series of FinFET devices have been manufactured and measured in the IMEC - Interuniversity Microelectronics Center in Belgium, and used in the Ph.D. Thesis of (FERREIRA, 2012).

The devices were fabricated on Silicon on Insulator (SOI) substrates, with fin thicknessess (T_{fin}) of 5nm, 10nm, 15nm and 20nm, and mask gate lengths (L_{mask}) varying from 10µm down to 25nm. The devices with good controllable electric characteristics are only above 10nm fin thickness and above 45nm gate length. Two runs with different process steps were used, namely the *Reference Process* and the *Highly Doped Process*.

The Reference Process starts with SOI wafers with 145nm of buried oxide (T_{box}) and 65 nm of silicon film, after the fins are etched (H_{fin}). The gate dielectric is a 2.5nm layer of SiON (T_{ox}), resulting in a 2.2nm effective oxide thickness (EOT). The gate electrode is formed of a 5 nm layer of TiN followed by a 100nm polysilicon layer. After the gate is etched, the source and drain of the device are lightly doped in a 45° angle and the nitride spacers formed. The source and drain are then highly doped and a nickel silicidation is performed on the electrodes. The Highly Doped Process has an additional step of tilted doping in the source and drain, such as the extension below the gate are increased. The schematic of the fabricated devices is presented in Fig. 5.1. It shows the cross section of a single fin. All devices have five parallel fins, with 200nm of fin pitch (P_{fin}) and 90nm of source and drain extensions (L_{SDmax}). Figure 2.3, shown previously, is created following the schematic of the manufactured devices, and most of the dimensions mentioned for such devices are indicated in this figure.

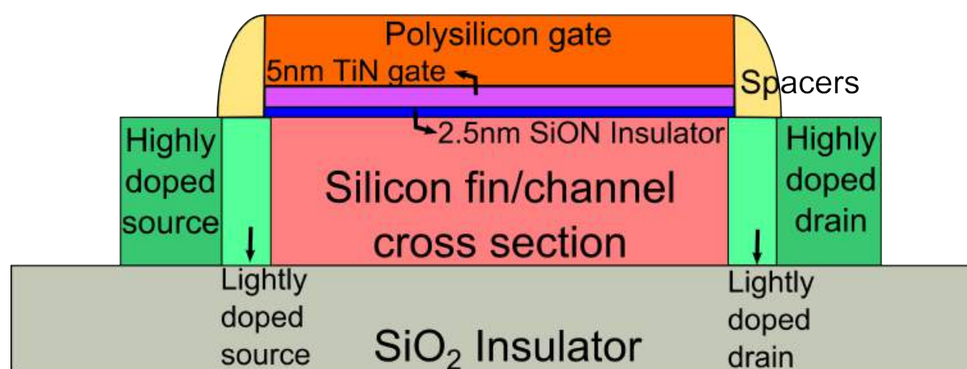


Figure 5.1: Schematic of the fabricated devices, showing the cross section of a single fin. Note the lightly doped region below the gate spacers, a characteristic of the LDD structure

The manufactured FinFETs present characteristics of lightly doped drain (LDD) devices. Such devices have a lightly doped region between the channel and the the highly doped source and drain. This structure creates challenges in the extrinsic parameter extraction, especially regarding the modulation of the source and drain resistance and effective channel length.

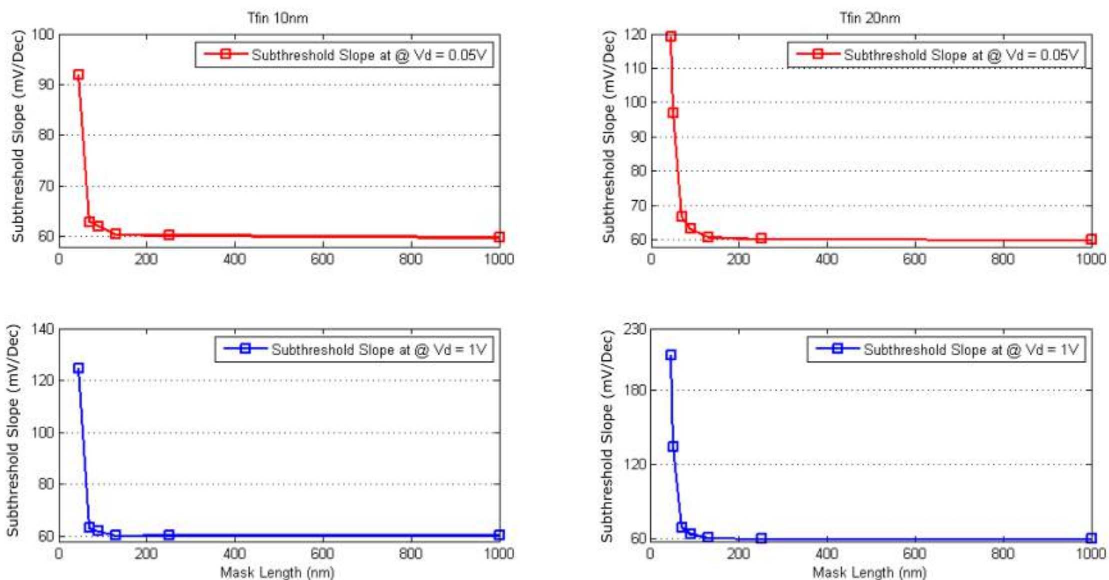
Table 5.1: Available mask gate lengths for the Reference Process FinFETs with 10nm to 20nm of fin thickness

	Mask Gate Length (nm)							
Tfin 10nm	10k	1k	250	130	90	70	45	
Tfin 15nm	10k	1k	250	130	90	70	45	
Tfin 20nm	10k	1k	250	130	90	70	50	45

The devices were measured in Belgium in the IMEC facilities. The I-V data was acquired with a probe station Suss Wafer Prober PB300 and a semiconductor parameter analyser HP4156. The dataset has $I_D x V_G$ for all modes of operation and $I_D x V_D$ for different V_G biases.

Table 5.1 presents the values of mask gate length used in this work for the devices with 10nm, 15nm and 20nm of fin thickness.

5.2 Subthreshold Slope and Threshold Voltage Extraction



(a) Subthreshold slope of FinFETs with fin thickness of 10nm, in the linear and saturation regions

(b) Subthreshold slope of FinFETs with fin thickness of 20nm, in the linear and saturation regions

Figure 5.2: Comparison of extracted subthreshold slope from devices with different fin thickness. Narrow fins provide better control of the subthreshold region and thus lower subthreshold slope.

Fig. 5.2 compares the subthreshold slope of FinFET devices with 10nm fin thickness 5.2a and with 20nm fin thickness 5.2b. On the top plots is the extraction in the linear region, and on the bottom, in the saturation region. The high slope degradation of 45nm mask length devices

is clearly visible, denoting poor subthreshold characteristics for such devices, either with 10nm or 20nm of fin thickness. The obtained results are in line with the works presented in (PEI et al., 2002; LEDERER et al., 2006; SUBRAMANIAN et al., 2007), which associate the increase in fin thickness with and increase in subthreshold slope and short channel effects. the subthreshold slope also deviates from the optimal 60 mV/dec in devices with 90nm and 70nm of mask length, denoting that the fabricated FinFET devices present inferior control over short channel effects and thus a bad coupling between gate and channel. Such characteristic is even more clearly seen as the subthreshold slope is extracted in the saturation region, with higher V_{DS} bias. In this operation region, the drain has a greater electrical influence over the silicon channel, and the subthreshold slope is even more degraded.

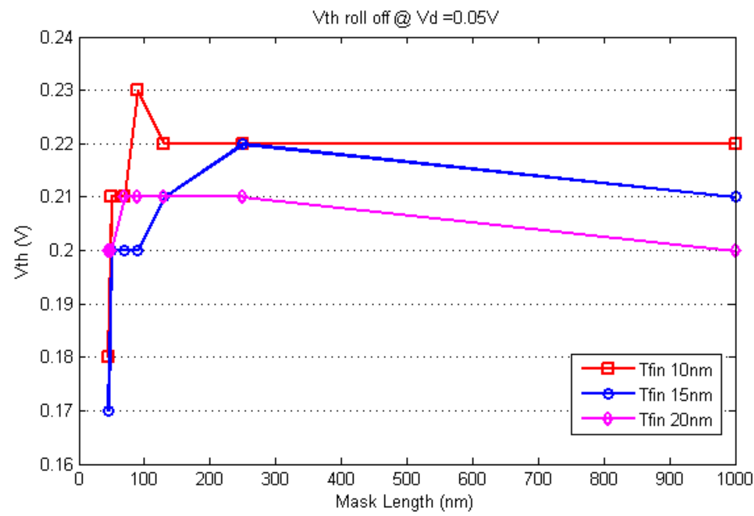


Figure 5.3: Threshold voltage extraction for all device in the linear region.

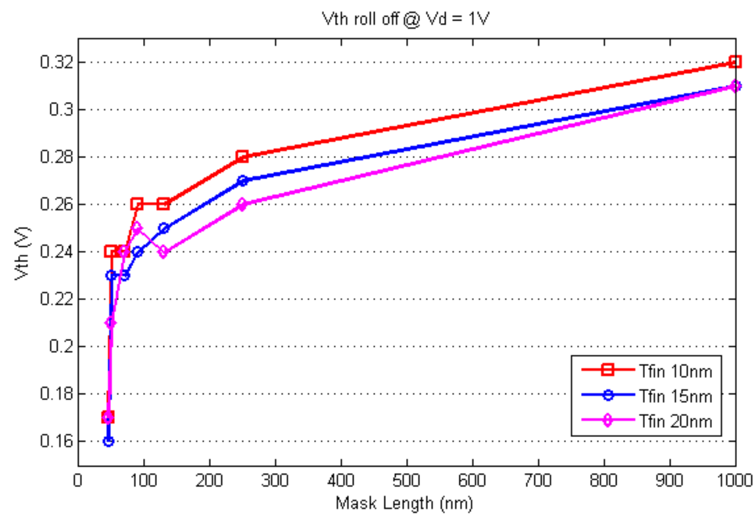


Figure 5.4: Threshold voltage extraction for all device in the saturation region.

Fig. 5.3 and Fig. 5.4 compare the extracted threshold voltage for devices with different fin

thickness. In the linear region, it is very clearly noted how the FinFETs with 20nm fin thickness have much smaller V_{th}. The threshold voltage of the devices remain relatively stable until the sub-100nm region, where the V_{th} roll off is steeper, denoting a higher DIBL in these devices. In the saturation region, the threshold voltage roll off trend is similar for all fin thickness. Thicker devices, however, present smaller V_{th}. FinFETs with 45nm mask length present very high short channel effects, shown here by a very right threshold voltage roll off. It is curious to note, however, how the device with fin thickness of 15nm and mask length of 45nm presents a smaller V_{th}, and thus higher DIBL, than the other, specially the 20nm FinFETs. This can be perceived both in the linear and saturation regions, and does not agree with the results presented in (PEI et al., 2002; LEDERER et al., 2006; SUBRAMANIAN et al., 2007) that conclude that a smaller fin results in better DIBL control. Those works, however, use devices with much thicker fins, to comparatively reach such conclusion.

5.3 Extrinsic Device Parameters

The extrinsic device parameter extraction methodologies previously discussed were applied FinFET measured data, in order to extract the R_{SD} and L_{eff} parameters. The three methods were used separately to provide results to be compared.

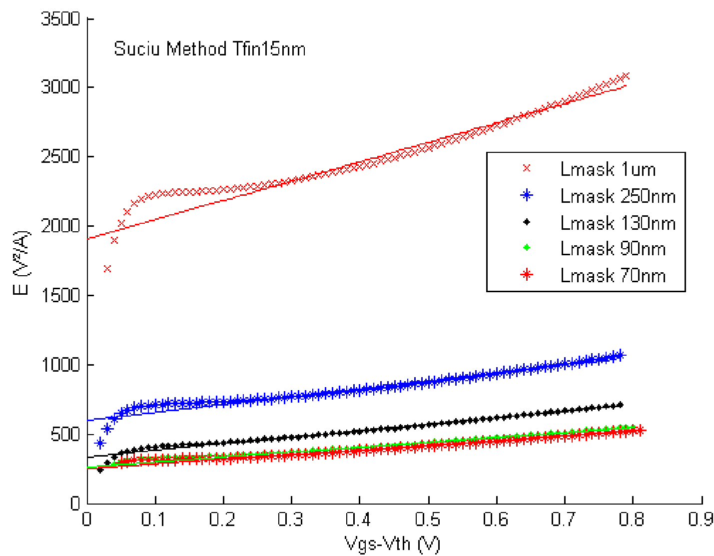


Figure 5.5: First step of Suciu-Johnston method, plotting E against the gate overdrive

The Suciu-Johnston method results are highly sensitive to the exact portion of the curve used for the linear fitting of E. Even after ignoring the clearly non-linear portion of E, in the low gate voltage overdrive region, the remaining curve is still not perfectly linear. Fig. 5.5 shows the non linearity of the $1\mu m$ mask length transistor, even for higher gate voltage overdrive. This creates a certain subjectivity in the portion of E used for the linear fitting. The choice of the interval in which the linear fitting of the Suciu-Johnston method will be made directly impacts in the final

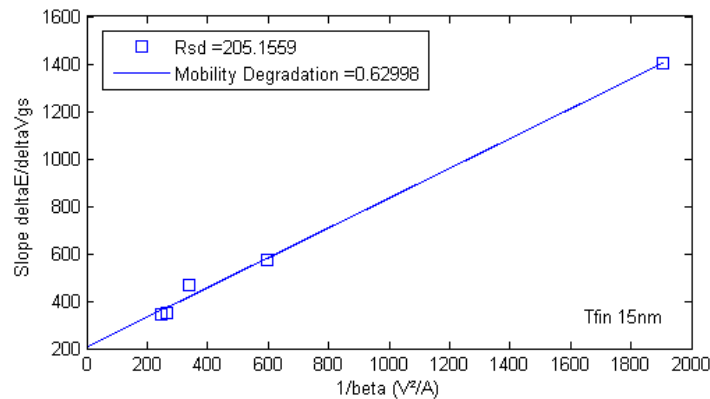


Figure 5.6: Suciu-Johnston method final results

R_{SD} extracted results, because it influences the slope and intersect of the curve shown in Fig. 5.6. This subjectivity indicates that the Suciu-Johnston method, proposed for bulk MOSFETs, may not be applicable to current nanoscale FinFET devices, and more so to the lightly doped drain FETs. Using the gate overdrive voltage interval from 0.3V to 0.8V for the linear fitting o E, in Fig. 5.5, the extracted R_{SD} is obtained as shown in Fig. 5.6, for the case of the devices with 15nm of fin thickness. The same was repeated for both 10nm and 20nm devices.

The results obtained with the Campbell methodology are shown in Fig 5.7, using V_{DS} = 50mV and V_{DS} = 100mV and FinFET devices with 20nm of fin thickness. While the series resistance varies for the different mask lengths at low gate voltage overdrive, it converges to the same value in higher biases. The dependence of the source and drain resistance with the gate voltage in the measured devices is clearly exposed. This dependence is a result of the

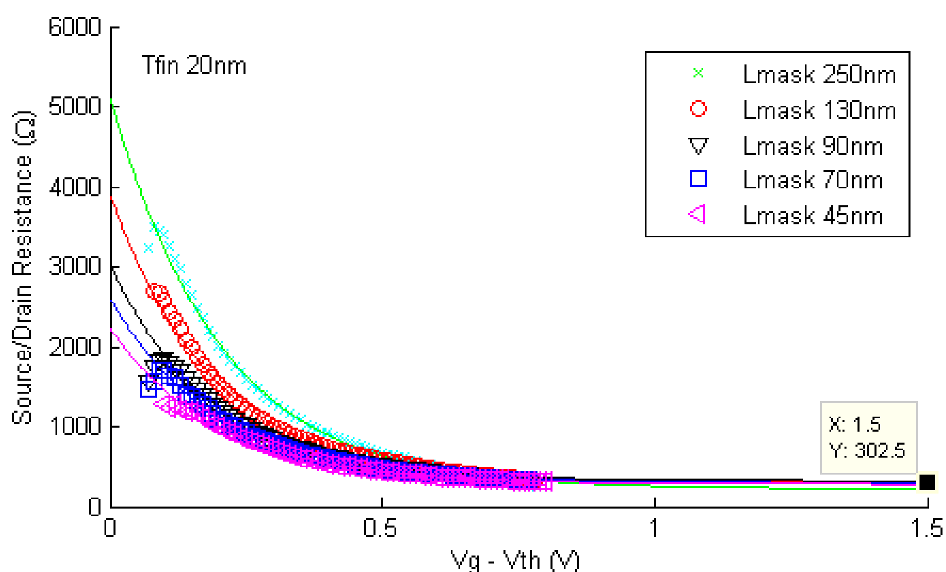


Figure 5.7: Campbell et al. method with extrapolation of the curves to yield a single value for the series resistance R_{SD}.

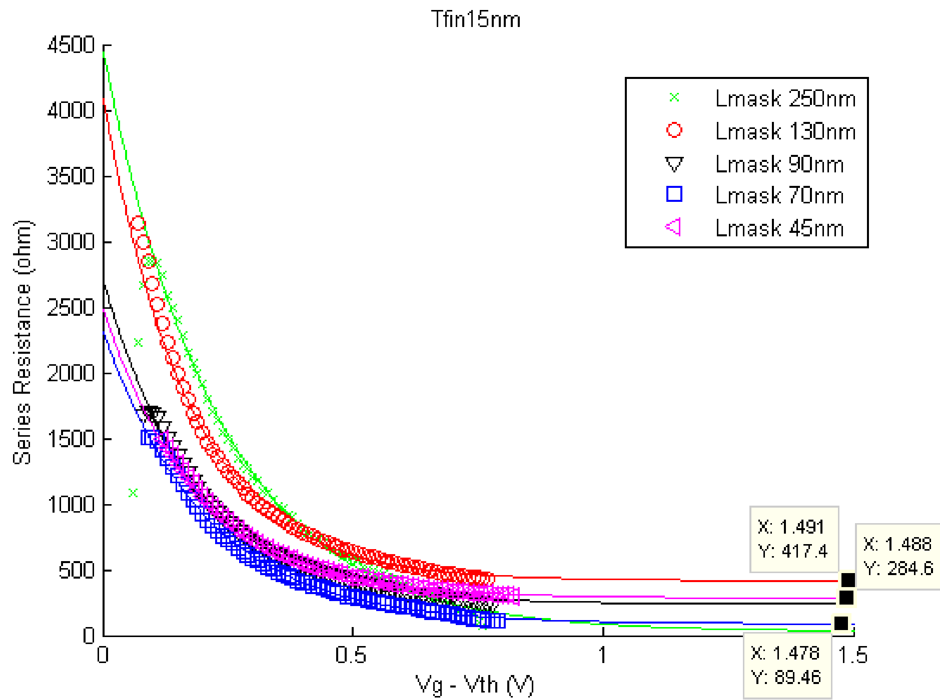


Figure 5.8: Campbell et al. method applied to the FinFETs with fin thickness of 15nm.

LDD structure of the devices, since the electric field generated from the gate changes the carrier density in the lightly doped regions, which in turn changes the series resistance (OGURA et al., 1980; HU; CHANG; CHIA, 1987; SHEU et al., 1984). For most modelling purposes, however, a single value of R_{SD} is required. This single parameter is extracted for a large gate voltage overdrive, while the exponential curve fitting is applied at low voltage overdrive, as shown in Fig 5.7.

The Campbell et al. method only assumes that μ_{eff}, C_{OX} and geometry parameters are constant for the same device in two very close drain bias, and thus it yields consistent results. The main weakness of the methodology lies in the sensitivity to device-to-device variations and in the lack of a procedure to obtain the effective channel length L_{eff}. Fig. 5.8 shows how devices with fin thickness of 15nm present a high variability in the evaluated value of R_{SD}. This can be advantageous if the objective is a very focused local modelling that extracts the exact series resistance of each different device. For a global parameter extraction, as in the case of this work, a single R_{SD} value is needed for the whole set of devices with the same fin thickness. The average value of the evaluated resistances was then used in the modelling.

The Torres-Torres is the most complex and computationally intensive of the studied methodologies. Fig. 5.9 exposes the results for the case of FinFETs with fin thickness of 10nm; The mobility degradation parameter θ used in the Torres-Torres method was extracted from the Suciu-Johnston method, as 0.53 for T_{fin} 20nm, 0.63 for T_{fin} 15nm and 0.65 for T_{fin} 10nm. The low field mobility parameter μ_0 was iteratively extracted from the $U0_0$ parameter of the BSIM-CMG model, as $680cm^2/Vs$, $640cm^2/Vs$ and $620cm^2/Vs$ for 20nm, 15nm and 10nm

fin thickness devices, respectively. This was the first iteration of the extracted parameters from the BSIM-CMG. The final low field mobility values was a little higher, but the results from the Torres-Torres method presented insignificant variation. Since this method extracts R_{SD} and ΔL as a function of the gate bias, the curves are extrapolated in order to determine the asymptotic values for the parameters. The effective channel length L_{eff} is given by $L_{eff} = L_{mask} - \Delta L$. The asymptotic ΔL value is considered exceptionally small, and was expected to be much higher because of the FinFETs fabrication process and the qualitative analysis of the I-V measurements. Although the variation of ΔL with the gate bias is almost insignificant, from 1.5nm to 1.8nm, in Fig 5.9, the presented trend does not agree with the expected results from LDD devices, where the effective length increases (and thus ΔL decreases) with the increasing of the gate bias (SHEU et al., 1984), not the opposite.

An important weakness of the Torres-Torres method is the dependence on auxiliary extractions to determine the gain factor G and the mobility degradation. The extracted channel length reduction ΔL was then assessed considering this important weakness. Fig. 5.10 explores the sensitivity analysis of the extracted channel length reduction ΔL with variations of the low field mobility μ_0 and the mobility degradation θ, for devices with 10nm of fin thickness. For the sensitivity analysis to the variation of low field mobility μ_0, the mobility degradation θ was fixed as the value extracted by the Suciu-Johnston method. For the assessment of sensitivity to the mobility degradation variations, μ_0 was set as the value extracted from the BSIM-CMG. However, Fig. 5.10 shows that the sensitivity of ΔL with the parameters is very small, presenting a

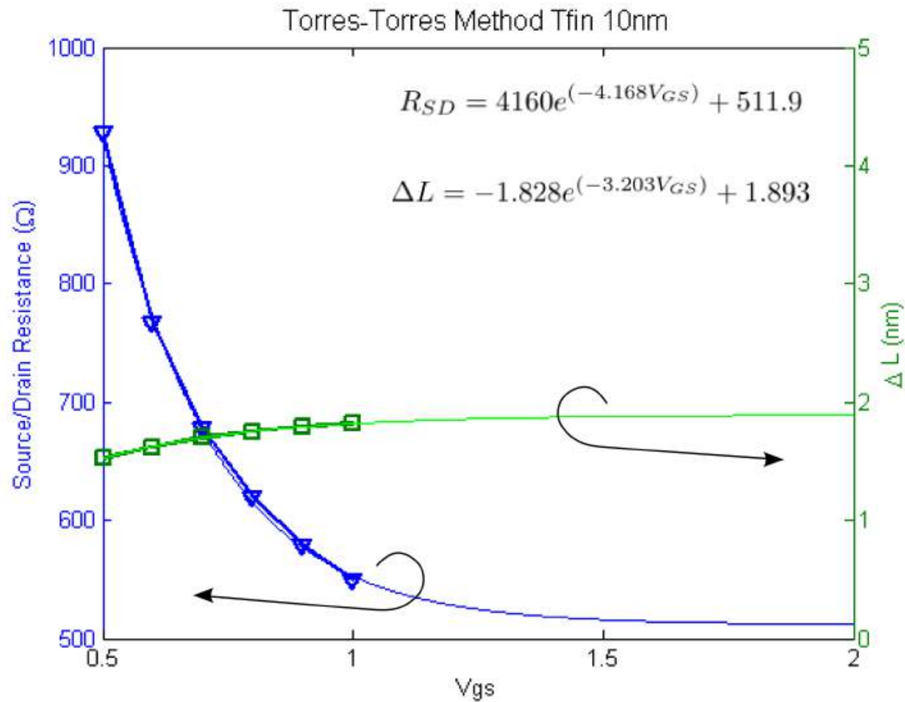


Figure 5.9: Torres-Torres method results, presenting the extracted R_{SD} and ΔL, along with their dependence on V_{GS}.

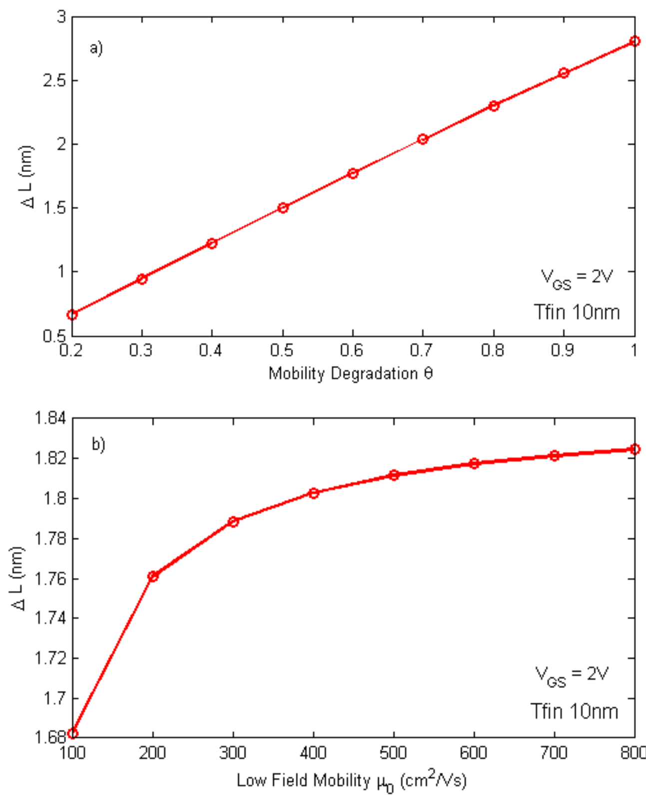


Figure 5.10: a) ΔL sensitivity on the mobility degradation θ and b) a low field mobility μ_0, in the Torres-Torres method.

limited amplitude. The Torres-Torres is considered thus to fail at extracting the channel length reduction, partly for its exceptionally small values, but also for the presented trend, which is not characteristic of LDD devices.

The extracted series resistance across different fin thickness for the different methods is shown in Fig. 5.11. The increase in resistance for narrow FinFETs is expected, since the series resistance is inversely proportional to the fin thickness, mainly due to the contact resistance and the sheet resistance, as reported in (MAGNONE et al., 2008; SUBRAMANIAN et al., 2007; DIXIT et al., 2005). The Campbell and Torres-Torres methods produced very consistent values. The Suciu-Johnston methodology highly underestimates the series resistance, which in turn can lead to an incorrect extraction of other parameters.

A 300Ω resistance in the device – as shown in the 20nm fin thickness case – indicates that each of the five fins has R_{series} approximately $1.5K\Omega$. This very high resistance is a result of the narrowness of the fin and the lack of selective epitaxial growth over the fins. A value of series resistance per fin is important as a figure of merit for the FinFET technology, since the devices may have different number of parallel fins, according to design decisions.

Table 5.2 presents the extracted values for both series resistance and channel length reduction. The values for R_{SD} are directly extracted from the agreement of the Campbell and Torres-Torres methods, shown in Fig. 5.11. The channel length reduction was obtained from the

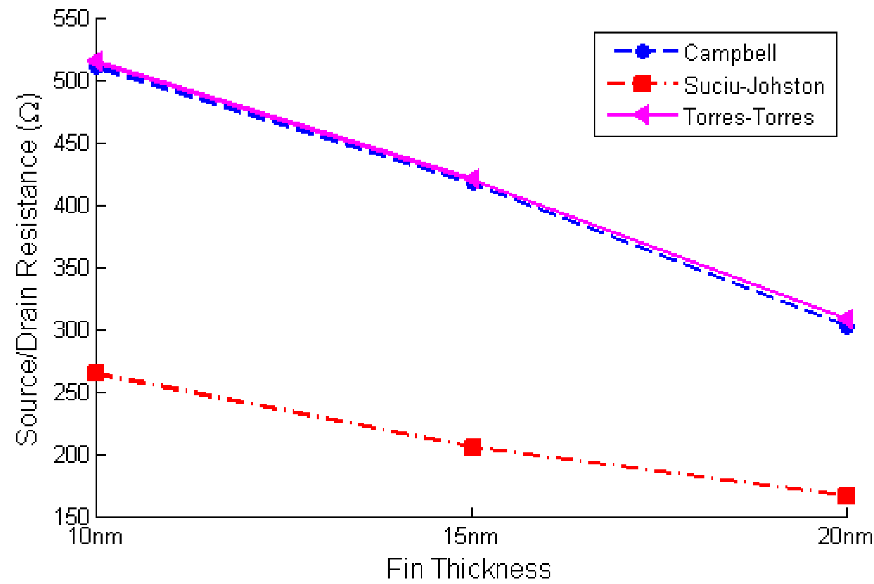


Figure 5.11: Source and drain resistance relationship with fin thickness for the explored methods

Table 5.2: Extracted values of series resistance and channel length reduction. The following values were used as initial parameters for the models.

	Series Resistance	**Channel Length Reduction**
Tfin 10nm	514 Ω	14 nm
Tfin 15nm	440 Ω	15 nm
Tfin 20nm	300 Ω	16 nm

BSIM-CMG parameter extraction, using several iterations, that will be further detailed in section 5.5. The values for the channel length reduction extracted from the Torres-Torres method were considered exceptionally small and inaccurate, as mentioned, and rendered higher errors in the modelling, thus the alternative extraction employed. A new methodology for the extraction of the effective channel length should be created to specifically address the deca-nanometer FinFET technology node in order to obtain precise values.

5.4 EKV Double-Gate Implementation

The EKV Double-Gate model implementation was partly available in (PRÉGALDINY et al., 2006). However, the code is in VHDL and only the core model, for long channel FinFETs, was implemented. The model was thus ported to MATLAB code, in order to provide better accessibility and to ease the implementation of short channel effects and the parameter extraction procedure. The effective mobility, DIBL and SCE were added to the core model, mainly following the proposed equations on (DIAGNE et al., 2008; TANG et al., 2009), but also con-

sidering the changes in (YESAYAN et al., 2011). The effects that have been added to the core long channel formulation are presented in table 5.3.

Table 5.3: Added effects to the MATLAB implementation of the long channel core model of the EKV Double-Gate

Formulation	**Description**
$n = \frac{1}{\left(1 - 2sinh\left(\frac{0.6L}{l}\right)/sinh\left(\frac{L}{l}\right)\right)}$	Subthreshold slope degradation factor, related to geometrical parameters
$\Delta L = l.ln\left(\frac{a + b + \sqrt{b^2 + s \cdot a \cdot b + 1}}{a+1}\right)$ with $a = \frac{l}{L-2\cdot l}$ and $b = \frac{v_d - v_{dsat}}{e_{sat_long} \cdot l}$	Channel length modulation in the saturation region
$\mu_{eff} = \frac{\mu_T}{1 + \frac{\mu_T}{v_{sat}} \cdot \frac{v_{ds}.U_T}{L}}$	Carrier mobility degradation due to transversal electric field – in the formulation of μ_T – and velocity saturation
$\Delta v_{th} = 2 \cdot \gamma_{SCE} \cdot (v_{bi} - \phi_f - v_{to}) + \gamma_{DIBL} \cdot v_{ds}$	Threshold voltage roll off as a function of SCE and DIBL. Refer to 3.7 for more details

The implementation of the EKV Double-Gate model extracted from (PRÉGALDINY et al., 2006) had several issues, such as not explicitly setting parameters to zero, but rather concealing them, which is the case of $\Delta\phi$ in the formulation of the long channel threshold voltage v_{to} and also using the channel width as an input parameter, rather than the fin height and thickness as other models. The set of works that compose the formulation of the EKV Double-Gate model are also confusing, specially regarding where parameters should be normalized and where should not. The voltage normalizations, rather than ease the modelling, as suggested in (SALLESE et al., 2005), makes it more difficult, since the normalized voltages have no immediate meaning, and thus formulation and implementation errors are harder to detect.

The parameter extraction procedure was implemented in MATLAB, following the steps and considerations discussed in previous sections. A series of graphic interfaces leads the user through the process, and in the final step the values for the low field mobility μ_0 and work function difference between the gate electrode and silicon channel $\Delta\phi$ are tuned for each individual device.

Fig. 5.12 presents the Mean Absolute Percentage (MAP) Error for the data fitting between the EKV model and the measured FinFET DC I-V data, after the parameters are extracted. Since the EKV model does not account for GIDL, the MAP error was calculated only from $V_{GS} = 0V$

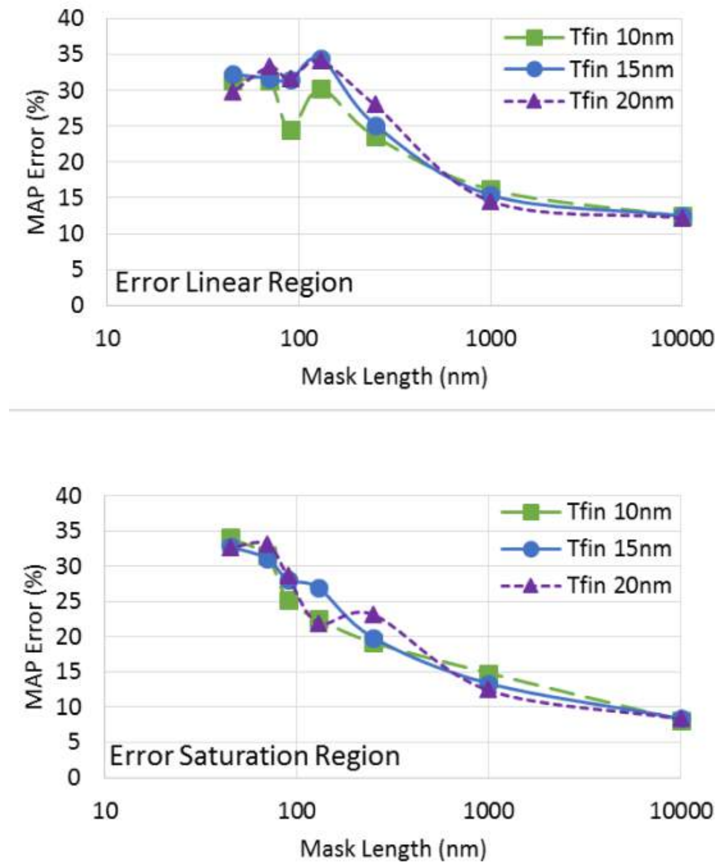


Figure 5.12: Mean Absolute Percentage Error between EKV Double-Gate model and measurements, for all devices in the linear and saturation regions. Mask length is shown in logarithmic scale for better visualization

up, otherwise the accumulation region error would dominate. Although the mean error does not seem overly high, Fig. 5.13 shows how the model barely fits the data, having serious problems to correctly model the subthreshold slope and the above-threshold current slope in the saturation region. This can be explained by the lack of modelling of several physical effects, such as mobility scattering, and the simplistic modelling of others, for example the mentioned subthreshold slope degradation and velocity saturation of carriers.

5.4.1 EKV Double-gate Extracted Parameters

The extracted values for μ_0 and $\Delta\phi$ are plotted in Fig. 5.14 after finely tuning them to achieve the smaller possible error in the linear and saturation regions simultaneously. The variation in the low field mobility is expected, following other model formulations (SRIRAMKUMAR et al., 2013) and theoretical observations (FISCHETTI et al., 2007), the electronic transport mobility lowers in short channel devices.

Such a variation in $\Delta\phi$, is due to the simplicity of the EKV Double-Gate compact model.

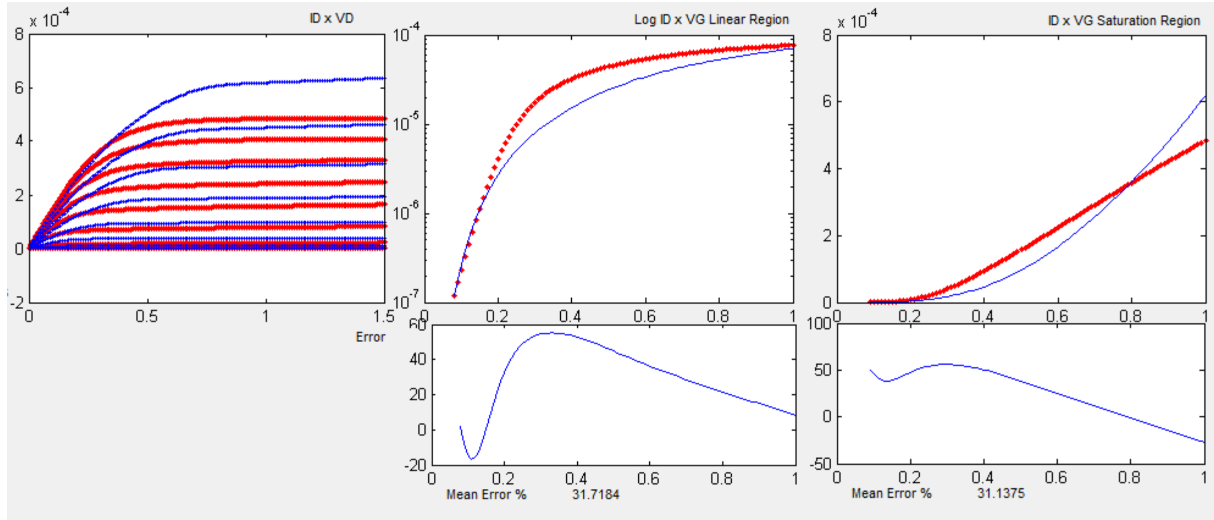


Figure 5.13: Fitting of the EKV - DG model to the data measured from a FinFET with fin thickness of 20nm and mask gate length of 70nm

The devices do not present so much statistical process variability regarding the gate electrode work function, and specially not such a "well-behaved" variation as a function of the mask length. It is simply a model weakness, that in order to obtain a minimally good fitting with the measured data, this parameter has to be changed as well. The work function of the gate metal TiN can be controlled by varying the deposited film thickness (KADOSHIMA et al., 2009), but it was not the case in the fabricated FinFETs.

The DIBL and SCE extracted parameters are presented in Table 5.4. Those parameters are used to model the threshold voltage variation Δv_{th}.

Table 5.4: Extracted values of series resistance and channel length reduction. The following values were used as initial parameters for the models.

	α_{SCE1}	α_{SCE2}	α_{SCE3}	α_{DIBL1}	α_{DIBL2}	α_{DIBL3}
Tfin 10nm	3.2	0.388	0.02	1.22	0.6	0.004
Tfin 15nm	0.5	0.558	0.02	0.32	0.86	0.0054
Tfin 20nm	-2.2	0.728	0.02	0.005	1.12	0.0068

The sensitivity of the threshold voltage variation Δv_{th} to the parameters related to short channel effects and DIBL are presented in Fig. 5.15. The extracted parameters presented in table 5.4 were used as reference, while the each of them was individually varied. The device under test was the FinFET with fin thickness of 20nm and mask gate length of 70nm, in order to observe short channel effects.

But this sensitivity to DIBL and short channel effects is not enough to correctly model the subthreshold region because the formulation of the EKV Double-Gate relies solely on a subthreshold slope degradation parameter n that modulates the gate voltage. This simplistic formulation does no provide enough accuracy to the modelling. Fig. 5.13 has already demonstrated

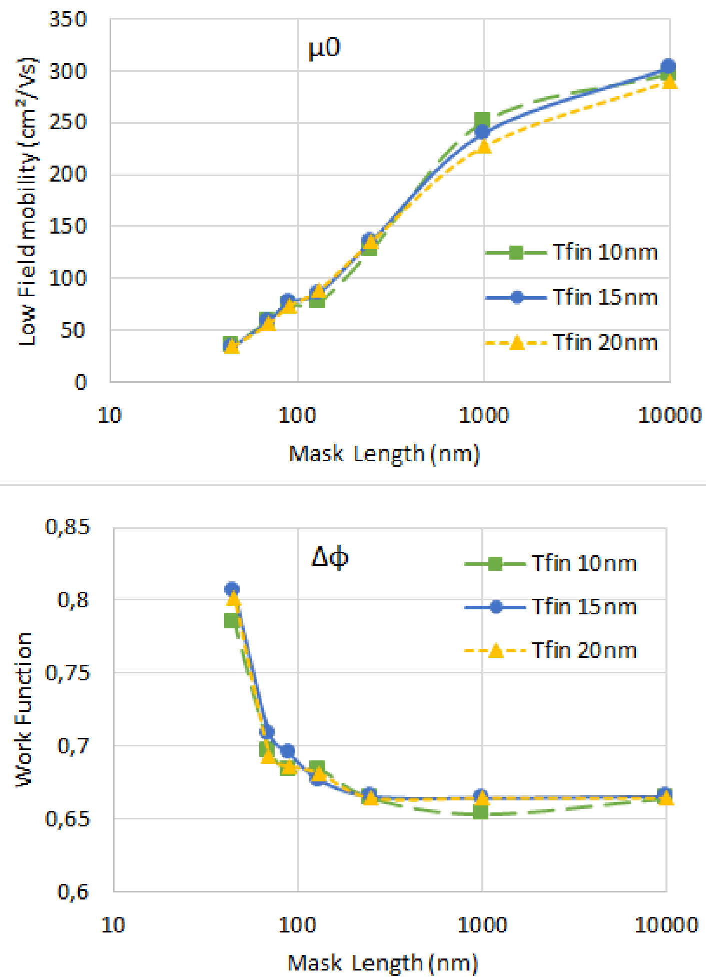
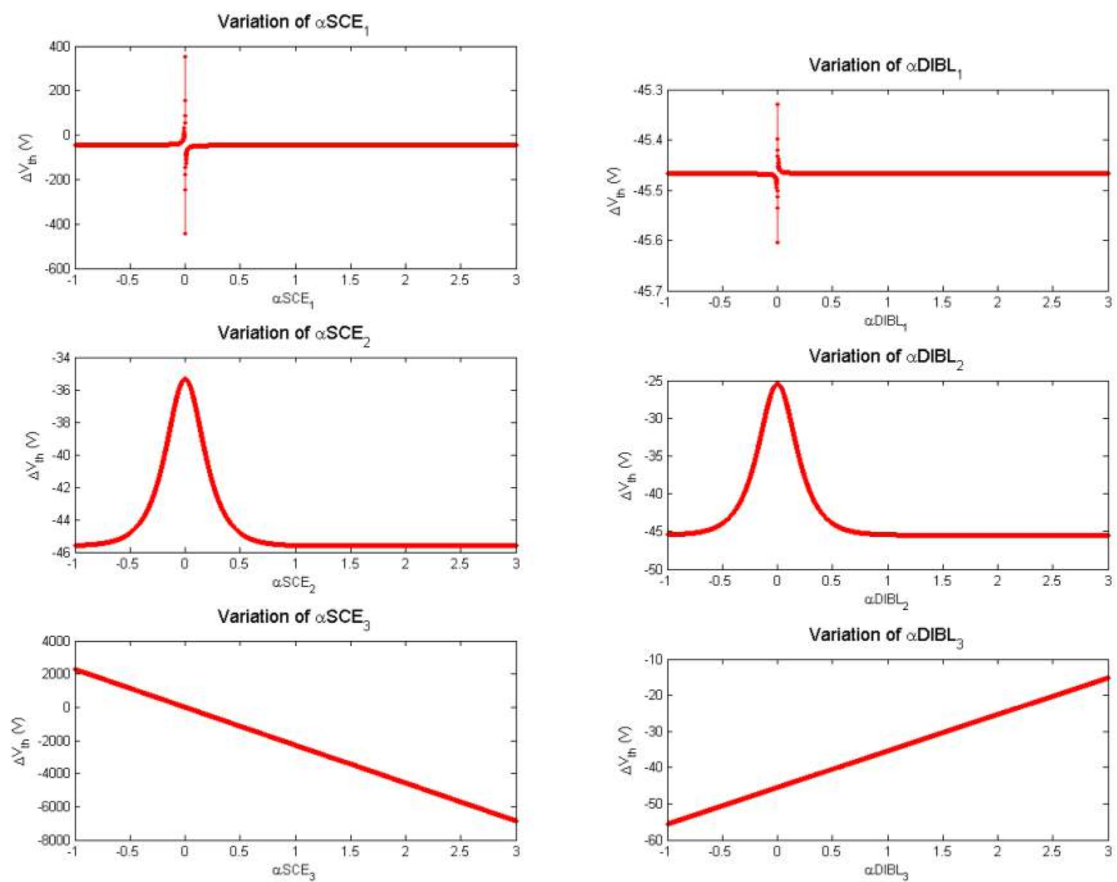


Figure 5.14: Extracted low field mobility and $\Delta\phi$ for the EKV Double-Gate model using devices with fin thickness from 10nm to 20nm

how the model fails to properly model mobility reduction and DIBL effects.



(a) Parameters related to short channel effects

(b) DIBL-related parameters

Figure 5.15: Sensitivity of the threshold voltage reduction Δv_{th} to the parameters related to short channel effects and DIBL

5.5 BSIM-CMG Parameter Extraction Procedure Implementation

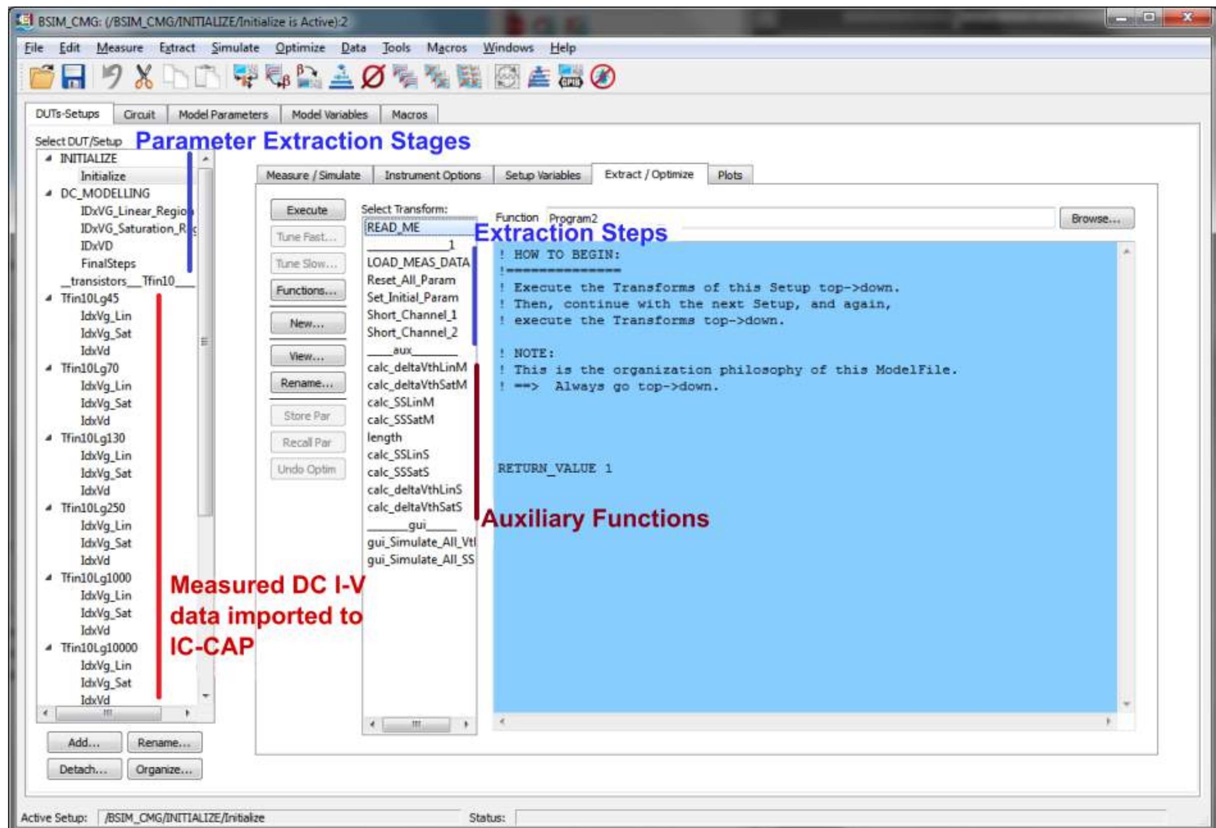


Figure 5.16: Basic structure of the IC-CAP implementation of the parameter extraction for the BSIM-CMG model.

The parameter extraction procedure proposed in (SRIRAMKUMAR et al., 2013) was implemented using the Keysight IC-CAP Modeling Software (KEYSIGHT TECHNOLOGIES, 2014) using the software infrastructure kindly provided by CEITEC S.A. Semiconductors. Fig. 5.16 presents the basic structure developed in IC-CAP for the parameter extraction. In the lower part of the left menu are the devices under test (DUT), with the different setups loaded from the DC I-V measurement files. The devices have different fin thickness and mask gate length, and each of them has linear and saturation region $I_{DS}xV_{GS}$ measurements and also $I_{DS}xV_{DS}$. The parameter extraction stages are divided in an initialization stage and extractions using data from the different operation regions. In each of the setups of the parameter extraction stages, there are different steps to be performed, that reflect the parameter extraction procedure discussed in section 4.4. This steps are in the Extract/Optimize tab, listed in the menu. Auxiliary functions are needed to provide calculations over the measurement data, such as threshold voltage extractions and others. Most of the parameter extraction steps have been implemented using the example model library called *DEPOTS*, that provides graphic interface utility. The different plots needed were created using different devices and operation setups, to accurately reflect the extraction procedure.

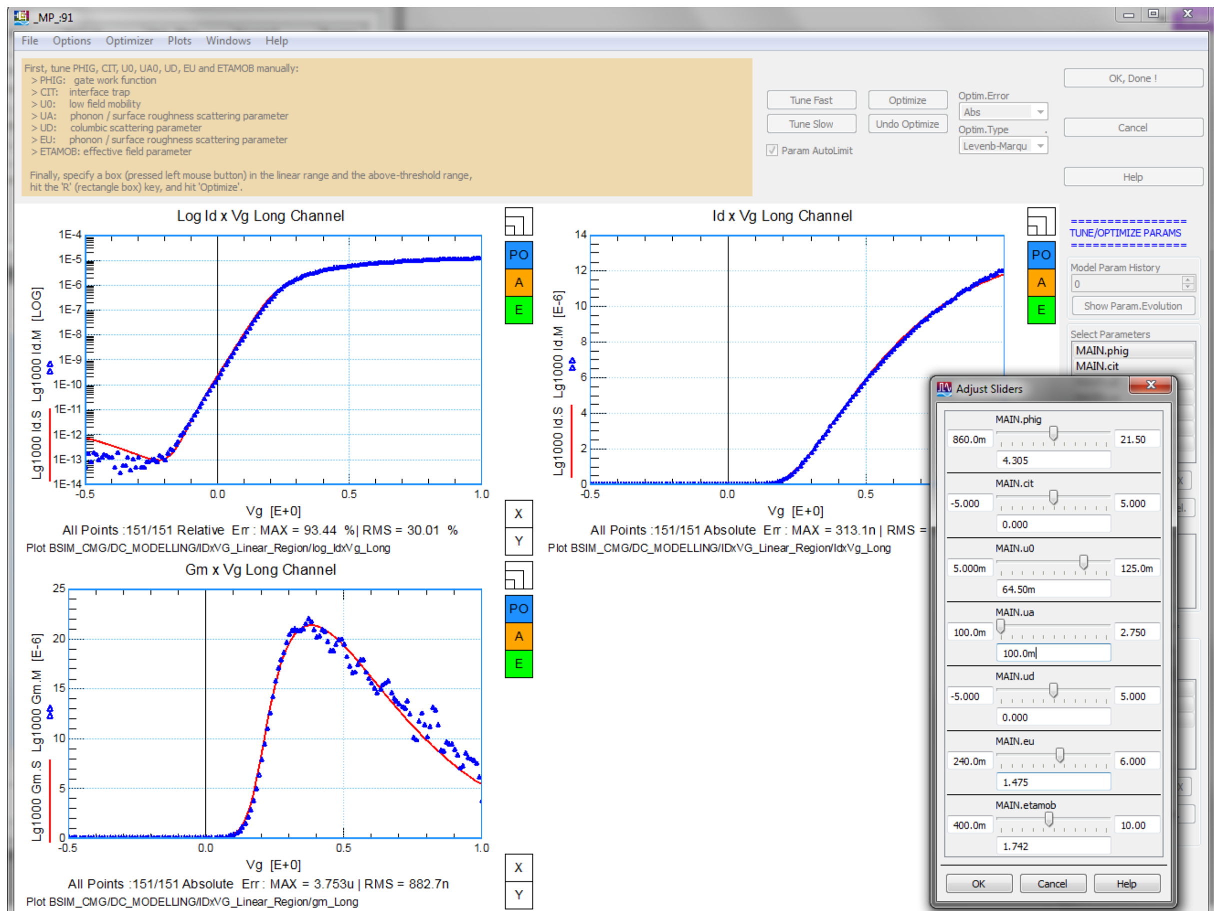


Figure 5.17: Example extraction graphic interface implemented in IC-CAP, showing the sliders that change the value of the parameters being extracted. Every time a slider is moved, the program simulates the all setups again and refresh the plots.

Strictly following the standard procedure resulted in inaccuracies in the modelling of smaller devices, mainly because the length dependent quantities are challenging to extract. To improve the extraction, we proposed changes to the flow, detailed in section 4.4, which were implemented as well. The main aspect of the new proposed implementation was a graphic interface presenting the plots of a certain operation setup for all devices, similar to Fig. 5.18. Once the key parameters were changed in a regular parameter extraction step, an auxiliary function to perform the simulation of all devices was executed and all plots refreshed. With this extra step, it could be guaranteed that the parameters were consistent throughout the whole procedure, for all devices.

Another key aspect of the parameter extraction was that the channel length reduction ΔL obtained from the Torres-Torres method induced great discrepancies between the simulated curves and the measured FinFET data. The parameter LINT, initialized as LINT = $\Delta L/2$ is in the formulation of every length dependent quantity, which in turn are central to the BSIM-CMG equations. An erroneous value for this parameter result in inaccuracies in the modelling and thus interfere in the correct parameter extraction. In order to obtain a correct value for

the parameter LINT, an iterative extraction was performed, where LINT was changed and the whole set of devices re-simulated, and other parameters, mainly in the linear region parameter extraction stage, also adjusted, in order to improve the modelling. After some iterations of this process the value of the channel length reduction LINT was set with confidence.

Fig. 5.18 shows the resulting curves, after the parameters were successfully extracted, for devices with 20nm of fin thickness, in the linear region. The model shows a very good agreement to the data. The smaller devices are not as well fitted to the data because the BSIM-CMG does not consider the physical transport effects in the smaller devices, but rather tries to fit them with the length dependent model parameters.

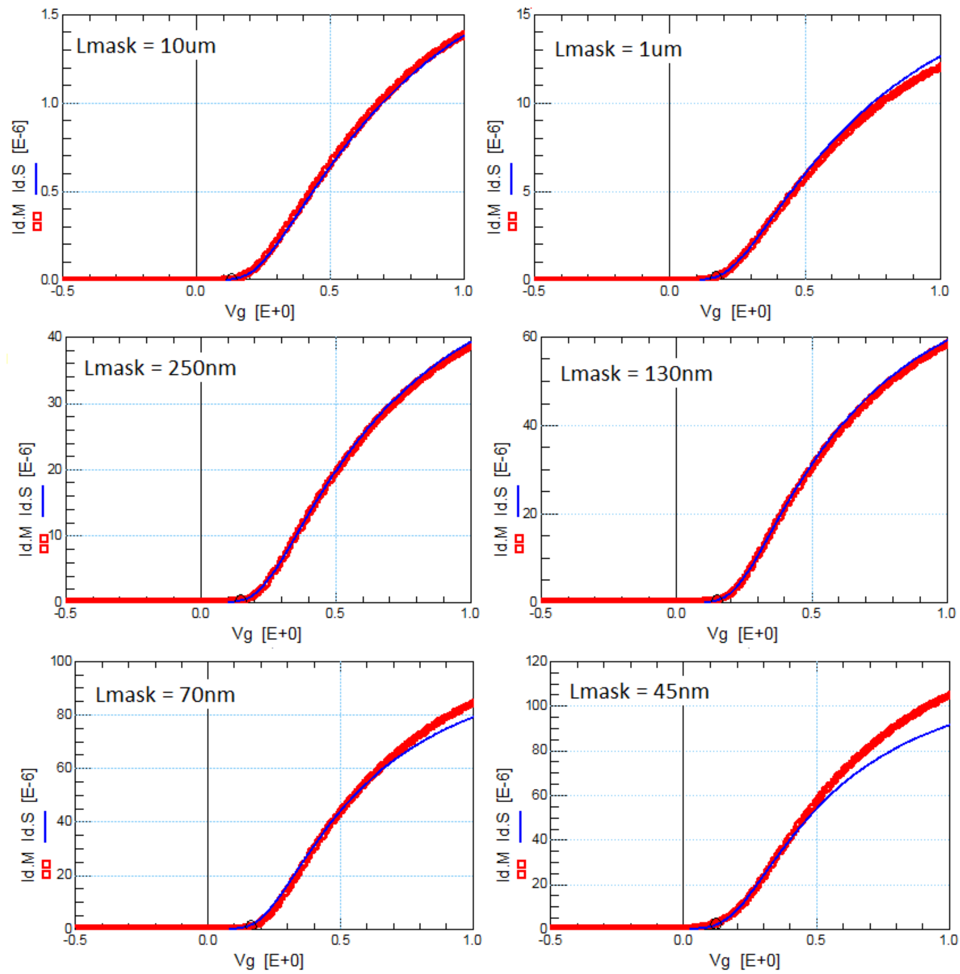


Figure 5.18: Resulting plots for devices with 20nm of fin thickness.

For analysing the quality of the modelling, we used the Mean Absolute Percentage Error (MAP Error) metric, according to the definition:

$$MAPE = \frac{1}{n}\sum_{i=1}^{n}\left|\frac{y_{i(Simulated)} - y_{i(Measured)}}{y_{i(Measured)}}\right| \tag{5.1}$$

The advantage of the Mean Absolute Percentage Error is that it places equal importance in

errors in the subthreshold and in the strong inversion region.

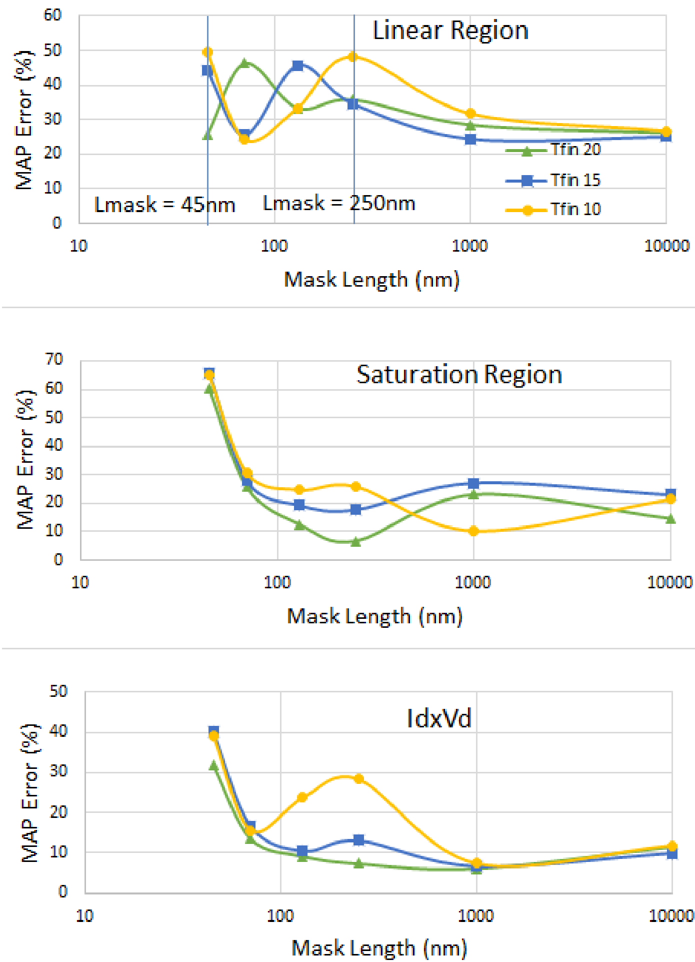


Figure 5.19: Mean Absolute Percentage Error for all devices in each of the operation regions. Mask length is shown in logarithmic scale for better visualization

Fig. 5.19 shows the MAP error of the model fitting in the different operating regions of the FinFETs. The graphics plot the device mask length against the MAP error, for different fin thickness. We notice that the mean error stays below 50% in the linear region, for all devices. In the saturation region the error stays below 30% for devices with mask length grater than 45nm. When assessing the I_{DS} x V_{DS} data, the MAP error is even smaller, around 10% for most cases. The 45nm channel length device presents a bigger mean percentage error mainly due to the poor subtheshold characteristics and the BSIM-CMG issues regarding parameter scaling, mentioned above.

The BSIM-CMG models has an excellent fitting for the subthreshold drain current of devices with mask length above 70nm. The subthreshold slope of the model matches the measured DC I-V curves in both linear and saturation regions, as seen in Fig. 5.20 and Fig. 5.21 for devices with mask length of 70nm and 250nm respectively. The plots show that even for different fin thickness, the model predicts very well the electrical behaviour of the FinFETs. Event the drain

current due to GIDL is accounted for, as noted in the saturation region plots. This excellent fitting in the subthreshold and immediately above is important in ultra low voltage and ultra low power applications, which operate in the near-threshold region to reduce power consumption while achieving sufficient performance (DRESLINSKI et al., 2010; MARKOVIC et al., 2010).

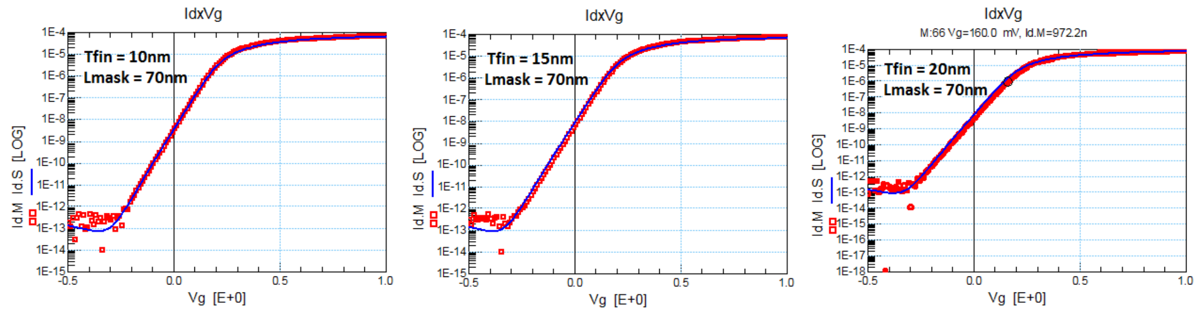


Figure 5.20: Modelling of devices with 70nm of mask gate length, with fin thickness of 10nm, 15nm and 20nm, operating in the linear region. The subthreshold region is very well fitted, showing accuracy in the formulation of SCE and DIBL.

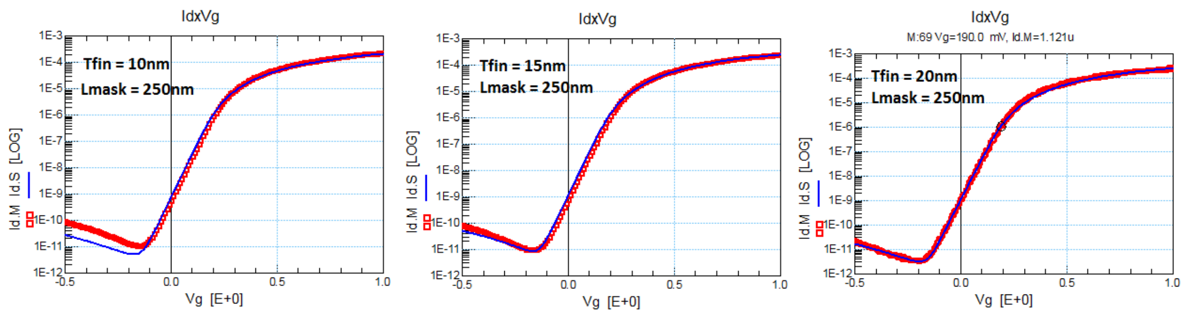


Figure 5.21: Modelling of devices with 250nm of mask gate length, with fin thickness of 10nm, 15nm and 20nm, operating in the saturation region. The both the accumulation and subthreshold regions are very well fitted, showing how GIDL was properly modelled in the BSIM-CMG. This effect is not accounted for in other double-gate compact models.

5.5.1 BSIM-CMG Extracted Parameters

The complete parameter set is given in Appendix A, organized in three model cards for the BSIM-CMG model, in SPECTRE syntax. Each model card is for devices with different fin thickness. This work assumed that the difference in fin thickness would imply in differences in electrical behaviour, specially transversal electric field, carrier mobility, velocity saturation and others.

Fig. 5.22 shows the behaviour of the length dependent quantity U0[L], the low field mobility, for devices with different channel lengths and fin thickness of 20nm. The same power-law trend repeats itself in both 15nm and 10nm devices. FinFETs with smaller channel lengths

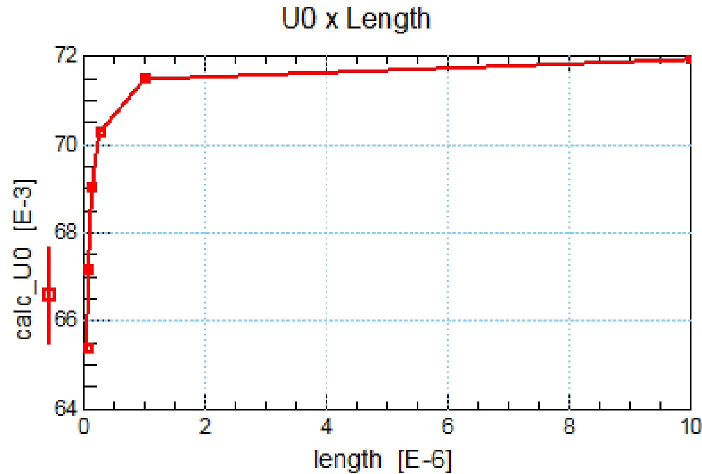


Figure 5.22: Low field mobility μ_0 scaling with mask length, for devices with 20nm of fin thickness

present smaller low field mobility because the drain current in the linear region is scaled down by this parameter, which in turn is formulated as a power-law to accommodate all channel lengths with a single set of parameters (YAO et al., 2010). This reflects theoretical observations presented in (FISCHETTI et al., 2007).

For each of the different extractions, the set of parameters slightly changed, and Fig. 5.23 presents an analysis of the physically relevant parameter variation with the transistor fin thickness. The low field mobility parameter $U0_0$ modulates the current in the linear region of device operation, while the velocity saturation parameters $VSAT_0$ and $VSAT1_0$ modulate in the saturation region. The last two parameters were chosen to be kept with the same value to improve the extraction and understanding. This clearly indicates that the current drive is higher as the fin becomes thicker. This behaviour is expected, since the channel width of a FinFET is given by $n_{fin}\left(2H_{fin}+T_{fin}\right)$, and an increase in fin thickness result in an increase in current drive. The magnitude of the current drive increase due to top gate conduction is a matter of discussion, however, specially in NMOS devices that present lower electron mobility in the top surface (GÁMIZ; GODOY, 2008; IYENGAR et al., 2007). In the PhD Thesis of (FERREIRA, 2012), the increase in drain current and transconductance in triple gate devices is almost insignificant, in comparison to double-gate FinFETs. Also, for nanoscale FinFETs such as the ones herein studied, is is questionable the application of the carrier mobility transfer model (VASILESKA; GOODNICK, 2002; VASILESKA et al., 2010). The mobility transfer model is in fact stretched to describe sub-100nm transistors, using fitting parameters to improve the final results, but not considering the physical meaning of the formulation.

The gate work function parameter PHIG has a very fine variation, with less than 0.02 eV, as also seen in Fig. 5.23. This is a reflex of the smaller long channel threshold voltage of 20nm fin thickness devices, in comparison to 10nm FinFETs, already described in Fig. 5.3 and Fig. 5.4.

Probably the most relevant parameter of the whole extraction for the BSIM-CMG, the channel length reduction LINT, shows a significant variation, from 7nm for FinFETs with 10nm of

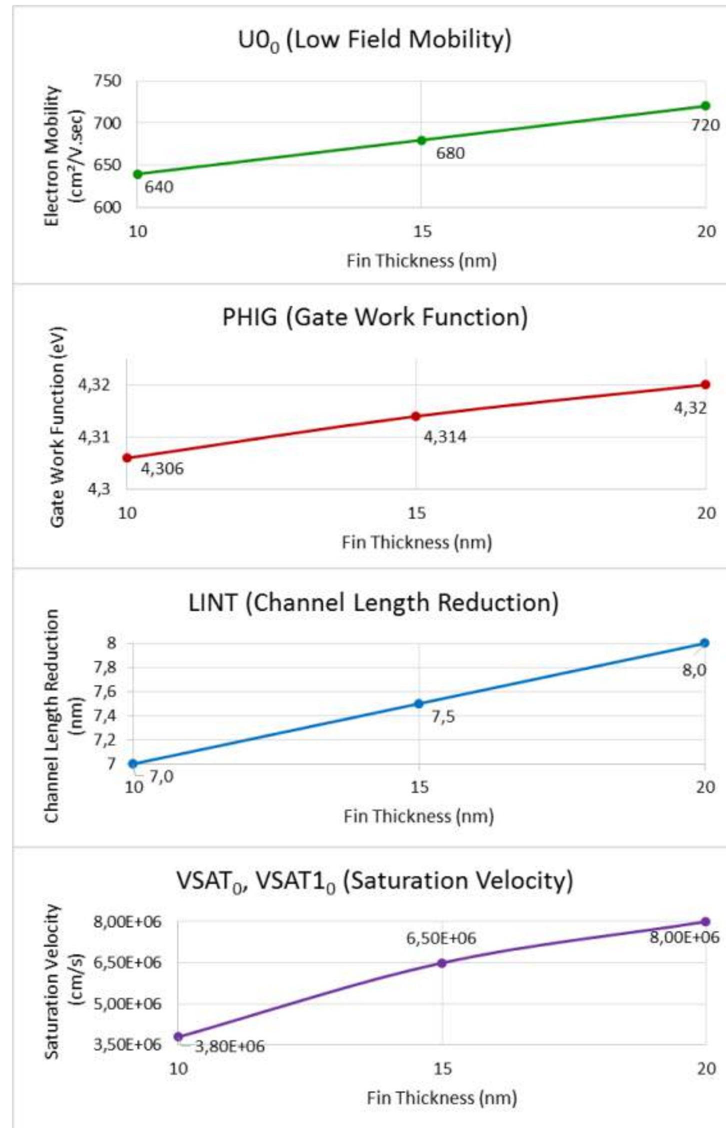


Figure 5.23: Comparison of physically relevant parameters extracted for devices with different fin thickness

fin thickness, to 8nm for devices with 20nm of fin thickness. LINT is the reduction in each end of the channel, which represents a total channel length reduction of 14nm to 16nm. This means that the FinFETs with mask channel length of 45nm have a effective channel length of 31nm to 29nm, depending on their fin thickness.

Fig. 5.24 in turn presents the extracted parameters that influence parasitic and short channel effects. The coupling capacitance between S/D and channel parameters CDSC and CDSCD indicate how strongly short channel effects influence the devices, specially regarding subthreshold slope degradation. Both parameters increase with thicker fins, supporting the conclusion that devices with narrow fins presents improved subthreshold slope characteristics, as seen in Fig. 5.2. The parameter CDSCD, however small, increases two orders of magnitude and has a strong effect of the subthreshold slope, since it is the model sensitivity to the parameter CDSC.

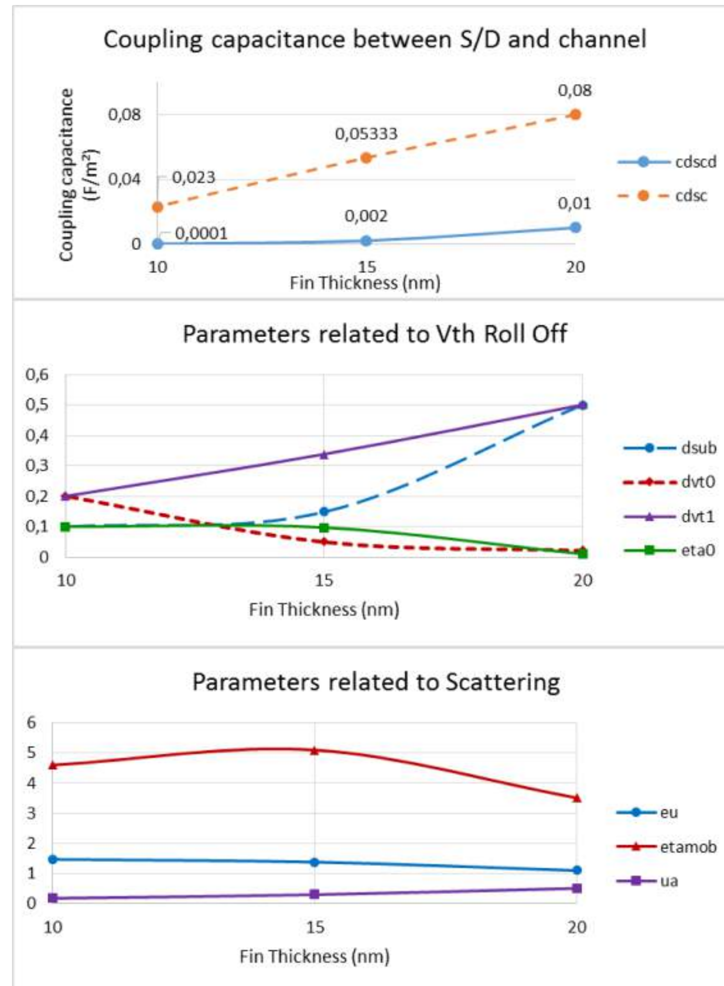


Figure 5.24: Comparison of short channel effect related parameters, extracted for devices with different fin thickness

DSUB and ETA0 are related to DIBL and have a higher effect in the saturation region, while DVT1 and DVT0 are related to SCE and affect the linear region characteristics. They change the threshold voltage roll off simultaneously, and are first extracted in the initialization step of the BSIM-CMG parameter extraction. The increase in DSUB and DVT1 reflect also an increase in the threshold voltage roll off, for devices with fin thickness of 20nm.

The last graphic shows the evolution of parameters related to electron scattering mechanisms. ETAMOB is the effective field parameter, UA is a phonon and surface roughness scattering parameter and EU is the exponent for the scattering formulation. These parameters controls the carrier mobility degradation. The effective field is lower in thicker devices because the two parallel gates are further apart. In very narrow fins, the effective field the electrons are imposed is extremely high and changes their trajectory to the sidewalls, and so the center of the fin presents minimal current density (MAGNONE et al., 2008; GÁMIZ; GODOY, 2008; MODY et al., 2010).

5.6 Discussions

The extractions of subthreshold slope and threshold voltage roll characteristics of the devices is an important key to assess their electrical behaviour and provide objective comparisons with other devices proposed in the literature, and FinFETs to be fabricated in future works. Similarly, extraction the series resistance from the experimental FinFETs helps identify weaknesses in the fabrication, such as the lack of selective epitaxial growth. Another important aspect to assess device performance is the leakage current due to GIDL, which greatly influences the OFF state current. It can be determined as the drain current in the accumulation region, which is shown Fig. 5.25 for devices with same mask gate length, but different fin thickness. The accumulation region current increases as the fin gets narrower, indicating that the effect of GIDL is greater, the opposite behaviour as reported in (CHOI et al., 2003). This result could be attributed to factors such as an increased electric field density in narrow fins – the work presented in (CHOI et al., 2003) measures devices only down to 26nm of silicon thickness – or even fabrication issues such as interface defects between the silicon fin and the dielectric. Those are all assumptions, however, and this non-agreement should be further studied.

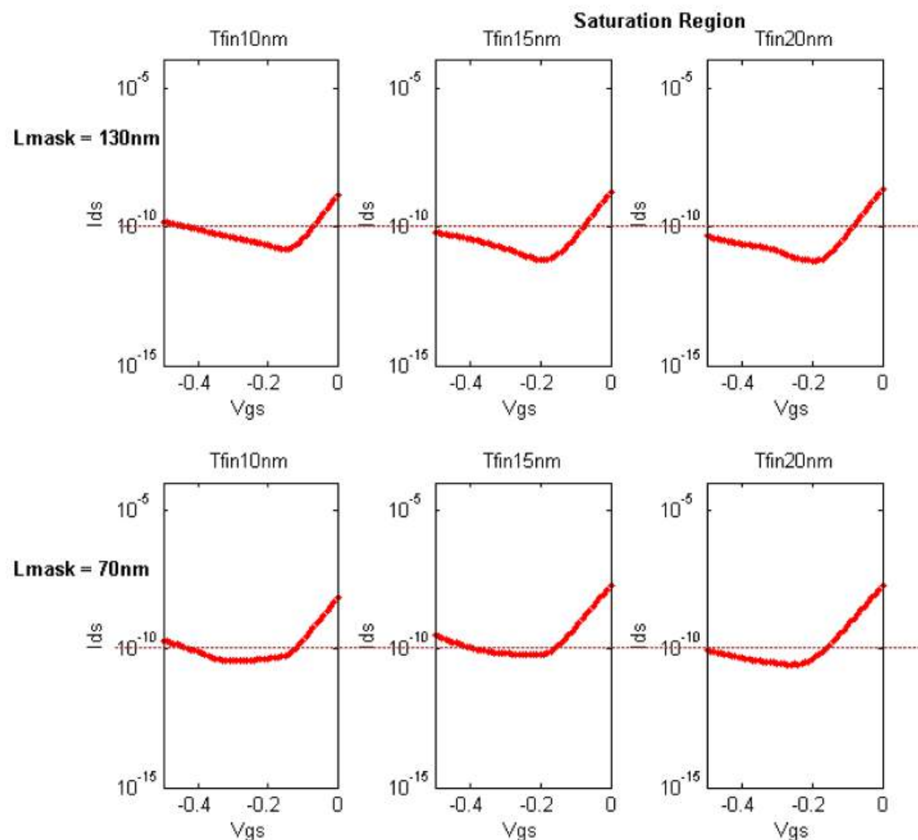


Figure 5.25: Leakage current in the saturation region due to GIDL for devices with the same mask length, but different fin thickness

The EKV Double-Gate model has several issues and ultimately fails at simulating the devices. Its formulation simplicity, and specially the reduced number of parameters diminish the ability of the model to correctly determinate the experimental FinFETs DC I-V characteristics. The main assumption of the EKV Double-Gate model, that enable the similarity to the planar MOSFET model, is that a FinFET acts as two planar MOSFETs in strong inversion (DIAGNE et al., 2008). This assumption, however, does not take into account real device parasitics such mobility degradation arising from the constrainment of the carriers to the channel surfaces. Since leakage currents in the accumulation region are also not included in the formulation, the model can only be applied to weak and strong inversion applications. Even then, only to provide a fast insight to the FinFET I-V curve, not an exact modelling. The papers which describe the model only use simulation data to validate the formulation, and in this lies the lack of agreement of this work with those papers regarding the accuracy of the device modelling. The presented simulations have sometimes even doubtful geometry parameters, such as in (YESAYAN et al., 2011) that uses a FinFET with 3nm of fin thickness and 50nm of fin height, granting a device with very high aspect ratio, but with several difficulties to be actually fabricated.

The improvements to the BSIM-CMG parameter extraction procedure allow the global modelling of a very large set of devices. A single set of parameters can be used to simulate FinFETs from 10µm to 70nm mask lengths with good accuracy, and 45nm devices with an acceptable error, depending on the application. To drastically reduce the modelling error, a local parameter extraction is necessary, such as to define parameters that very finely describe the electrical characteristics of a specific transistor geometry. A global model card is much more convenient for circuit designers while performing transistor size optimizations.

The extraction of the effective channel length from 31nm to 29nm, for the case of the 45nm mask gate length devices, clearly indicates that the fabricated FinFETs do not have adequate gate to channel coupling, since the smaller transistor presents heavy influence of short channel effects while its effective channel is not so small. FinFETs are able to properly control short channel effects with gate lengths down to 14nm as a current industry technology node, and 10nm in the next few years (INTEL, 2014a; INTEL, 2014b). To achieve this performance, one possibility is to use a gate insulator with higher dielectric constant, such as HfSiO and smaller effective thickness, that will provide better gate control over the channel, reducing DIBL and SCE (DAL et al., 2007).

6 CONCLUSIONS AND FUTURE WORK

This work has presented a theoretical insight in the issues regarding planar MOSFETs, the FinFET technology, and also the study on compact models for double-gate semiconductor devices, along with their parameter extraction methodologies. Several issues have been pointed regarding both the formulation of the models and the weakness in their parameter extraction procedures. Several changes have been proposed in order to improve the fitting of the model to the measured FinFET devices and to extract parameters that correctly reflect the electrical behaviour.

The parameter extraction procedure changes have resulted in excellent results, specially regarding the BSIM-CMG model. Using the modifications in the parameter extraction flow, the model parameters could be extracted for a wide range of FinFET mask channel lengths, from 10µm down to 45nm, presenting modelling errors around 20%, and even below 10% in certain cases.

The EKV Double-Gate compact model was implemented in MATLAB following the VHDL-AMS implementation of the long-channel core model and all short channel effects added as proposed in the literature. The parameter extraction procedure was performed and changed to improve the fitting between the simulated curves and the measured devices. Even after a careful extraction, the compact model presents weaknesses that render it unreliable for the correct simulation of FinFET devices.

The evolution of extracted parameters has been discussed for both models, with technological considerations. The BSIM-CMG extracts a single set of parameters and uses the length dependent quantities to allows for the modelling of devices with a wide range of channel lengths simultaneously. The variation of model parameters with the FinFET fin thickness follows expected trends and is considered an interesting analysis to be considered. The EKV Double-Gate extracted parameters, however, further reinforce the conclusion that the model simplicity is detrimental. That is because parameters that should not present a strong variation with the channel length, such as $\Delta\phi$, need to be used to force a better fitting between the model and the FinFET data, which in turn renders $\Delta\phi$ as a function of the channel length.

The importance of this work also lies in the determination of a complete set of parameters that correctly reflect the fabricated FinFET devices and allow for future circuit simulations. Additionally, this work has raised several points to be further discussed, due to its amplitude. Among them stands out the following topics that are intended to be addressed in the future:

Refinement of the parameter extraction method for the BSIM-CMG model, in order to achieve a better fitting still. The strategy will be to extract a parameter set for a restricted range of FinFET channel lengths. This approach is recommended to avoid the difficulties associated with the semi-empirical model and specially the complexity of the electronic transport, which is not accurately modelled for all devices at the same time. To precisely describe characteristics of very large devices, with L_{mask} of 10µm, down to deca-nanometer FinFETs, with

L_{mask} of 45nm, with a single parameter set and formulation is extremely difficult. Even though the results presented in this work were excellent – mainly due to the changes in the extraction procedure – a very fine modelling is possible using a smaller set of channel lengths.

Development of a reliable methodology to accurately extract L_{eff} in nanoscale FinFETS, so as to obtain this important electrical parameter in a simple and straightforward manner. The extrinsic parameters extraction methodologies covered in this work, while providing consistent values for the series resistance R_{SD}, failed to provide accurate and reliable values for the effective channel length L_{eff}.

Further study of FinFET fabrication processes and materials to improve the control over short channel effects and DIBL, improving their performance in the subthreshold region, in order to obtain sub-22nm and even sub-14nm channel length FinFETs with satisfying electrical characteristics. In order to provide objective quantitative comparisons between the different FinFET devices to be fabricated and even between those and the ones studies in this work it is important to similarly extract the device parameters. To assess different device characteristics such as mobility reduction arising from surface scattering and effective transversal field, a BSIM-CMG parameter extraction, with the methodology proposed in this work should also be performed.

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APPENDIX A BSIM-CMG MODEL CARDS

Table A.1: Tfin 20nm BSIM-CMG Model Card

```
subckt BSIM_CMGTfin20 (drain gate source bulk )
parameters Length=45n FIN=10n

// — Transistor —
X1 drain gate source bulk MAIN l = Length tfin = FIN

//——Model——

model MAIN bsimcmg
+ version = 107 bulkmod = 0 nfin = 5 capmod = 0 coremod = 1 cgeomod = 0
+ devtype = NMOS geomod = 1 gidlmod = 1 igbmod = 0 igcmod = 1 iimod = 0
+ ngate = 0 nqsmod = 0 rdsmod = 0 rgatemod = 0 rgeomod = 0 nseg = 5
+ sdterm = 1 shmod = 0 agidl = 8.7E-012 agisl = 1E-012 aigc = 0.014
+ aigd = 0.0136 aigs = 0.0136 at = 0.00156 ardsw = 0 aua = 0.01 aud = 0.00414
+ avsat = -2.5E+004 avsat1 = -1.8E+004 aptwg = 5 amexp = -0.4 bg0sub = 1.12
+ bgidl = 7E+008 bgisl = 3E+008 bigc = 0.0017 bigd = 0.0017 bigs = 0.0017
+ bua = 0.01 bud = 2E-008 brdsw = 0 bvsat = 3E-006 bvsat1 = 3E-006
+ bptwg = 6E-007 bmexp = 0.1556 cdsc = 0.08 cdscd = 0.01 cfd = 2E-011 cfs = 2E-011
+ cgbl = 0 cgbo = 0 cgdl = 0 cgdo = 1E-010 cgsl = 0 cgso = 1E-010 cigc = 0.075
+ cigd = 0.075 cigs = 0.075 cit = 0 ckappad = 0.6 ckappas = 0.6 cth0 = 1.243E-006
+ deltavsat = 1 deltaw = 0 deltawcv = 0 dlbin = 0 dlc = 0 dlcigd = 1E-009
+ dlcigs = 1E-009 drout = 0.51 dsub = 0.5 dvt0 = 0.022 dvt1 = 0.5008 dvtshift = 0
+ easub = 4.05 egidl = 0.7 egisl = 0.2 eot = 2.2E-009 eotacc = 2.2E-009
+ eotbox = 1.45E-007 epsrox = 4.43 epsrsp = 3.9 epsrsub = 11.9 eta0 = 0.01
+ etamob = 3.51 etaqm = 0.54 eu = 1.1 fpitch = 2E-007 hfin = 6.5E-008 igt = 2.5
+ k1rsce = -0.03 ksativ = 0.898 kt1 = 0 kt1l = 0 lint = 8E-009 lpe0 = 0
+ lpa = 0.9603 lcdscd = 5E-005 lcdscdr = 5E-005 ll = -2.4E-008 lln = 1
+ mexp = 9 nbody = 1E+018 nc0sub = 2.86E+025 ni0sub = 1.1E+016 nigc = 1 nsd = 2E+026
+ pclm = 0.009 pclmcv = 0.013 pclmg = 0 pclmgcv = 0 pdibl1 = 4 pdibl2 = 0.0005
+ phig = 4.32 phin = 0.05 poxedge = 1.1 pqm = 0.66 prt = 0 prwg = 0 ptwg = -0.08
+ ptwgt = 0.004 pvag = 1.1 qm0 = 0.001 qmfactor = 2.5 rdsw = 300 rdswmin = 0
+ rdwmin = 0 rshd = 0 rshs = 0 rswmin = 0 rth0 = 0.225 tbgasub = 0.000473
+ tbgbsub = 636 tgidl = -0.007 tmexp = 0 tnom = 25 toxp = 2.5E-009 u0 = 0.072
+ ua = 0.51 ua1 = 0.001032 ucs = 1 ucste = -0.004775 ud = 0.2 ud1 = 0
+ up = 2.5E-008 ute = 0 utl = -0.0015 vasat = 0.5 vsat1 = 8E+004
+ vasatcv = 0.2 vsat = 8E+004 wr = 1 wth0 = 2.6E-007 xl = 0

ends BSIM_CMGTfin20
```

Table A.2: Tfin 15nm BSIM-CMG Model Card

```
subckt BSIM_CMGTfin15 (drain gate source bulk )
parameters Length=45n FIN=10n

// — Transistor —
X1 drain gate source bulk MAIN l = Length tfin = FIN

//——Model——

model MAIN bsimcmg
+ version = 107 bulkmod = 0 nfin = 5 capmod = 0 coremod = 1 cgeomod = 0
+ devtype = NMOS geomod = 1 gidlmod = 1 igbmod = 0 igcmod = 1 iimod = 0
+ ngate = 0 nqsmod = 0 rdsmod = 0 rgatemod = 0 rgeomod = 0 nseg = 5
+ sdterm = 1 shmod = 0 agidl = 1E-011 agisl = 1E-012 aigc = 0.014
+ aigd = 0.0136 aigs = 0.0136 at = 0.00156 ardsw = -30 aua = -0.095
+ aud = 0.00414 avsat = -1500 avsat1 = -1500 aptwg = 7 amexp = -0.25
+ bg0sub = 1.12 bgidl = 4.5E+008 bgisl = 3E+008 bigc = 0.0017 bigd = 0.0017
+ bigs = 0.0017 bua = 1 bud = 2E-008 brdsw = 0.8 bvsat = 7E-007 bvsat1 = 7E-007
+ bptwg = 4E-007 bmexp = 0.15 cdsc = 0.05333 cdscd = 0.002 cfd = 2E-011
+ cfs = 2E-011 cgbl = 0 cgbo = 0 cgdl = 0 gdo = 1E-010 cgsl = 0 cgso = 1E-010
+ cigc = 0.075 cigd = 0.075 cigs = 0.075 cit = 3E-005 ckappad = 0.6 ckappas = 0.6
+ cth0 = 1.243E-006 deltavsat = 1 deltaw = 0 deltawcv = 0 dlbin = 0 dlc = 0
+ dlcigd = 1E-009 dlcigs = 1E-009 drout = 20 dsub = 0.1481 dvt0 = 0.05 dvt1 = 0.3382
+ dvtshift = 0 easub = 4.05 egidl = 0.8 egisl = 0.2 eot = 2.2E-009 eotacc = 2.2E-009
+ eotbox = 1.45E-007 epsrox = 4.43 epsrsp = 3.9 epsrsub = 11.9 eta0 = 0.09705
+ etamob = 5.1 etaqm = 0.54 eu = 1.38 fpitch = 2E-007 hfin = 6.5E-008 igt = 2.5
+ k1rsce = 0 ksativ = 0.88 kt1 = 0 kt1l = 0 lint = 7.5E-009 lpe0 = 0 lpa = 0.9853
+ lcdscd = 5E-005 lcdscdr = 5E-005 ll = -2.6E-008 lln = 1 mexp = 7 nbody = 1E+018
+ nc0sub = 2.86E+025 ni0sub = 1.1E+016 nigc = 1 nsd = 2E+026 pclm = 0.008
+ pclmcv = 0.013 pclmg = 0 pclmgcv = 0 pdibl1 = 1.749 pdibl2 = 0.0003 phig = 4.314
+ phin = 0.05 poxedge = 1.1 pqm = 0.66 prt = 0 prwg = 0 ptwg = 0 ptwgt = 0.004
+ pvag = 1.02 qm0 = 0.001 qmfactor = 2.5 rdsw = 440 rdswmin = 0 rdwmin = 0
+ rshd = 0 rshs = 0 rswmin = 0 rth0 = 0.225 tbgasub = 0.000473 tbgbsub = 636
+ tgidl = -0.007 tmexp = 0 tnom = 25 toxp = 2.5E-009 u0 = 0.068 ua = 0.3
+ ua1 = 0.001032 ucs = 1 ucste = -0.004775 ud = 0.2 ud1 = 0 up = 1E-008
+ ute = 0 utl = -0.0015 vasat = 0.5 vsat1 = 6.5E+004 vasatcv = 0.2
+ vsat = 6.5E+004 wr = 1 wth0 = 2.6E-007 xl = 0

ends BSIM_CMGTfin15
```

Table A.3: Tfin 10nm BSIM-CMG Model Card

```
subckt BSIM_CMG (drain gate source bulk )
parameters Length=45n FIN=10n

// — Transistor —
X1 drain gate source bulk MAIN l = Length tfin = FIN

//——Model——

model MAIN bsimcmg
+ version = 107 bulkmod = 0 nfin = 5 capmod = 0 coremod = 1 cgeomod = 0
+ devtype = NMOS geomod = 1 gidlmod = 1 igbmod = 0 igcmod = 1 iimod = 0
+ ngate = 0 nqsmod = 0 rdsmod = 0 rgatemod = 0 rgeomod = 0 nseg = 5
+ sdterm = 1 shmod = 0 agidl = 4.2E-011 agisl = 1E-012 aigc = 0.014
+ aigd = 0.0136 aigs = 0.0136 at = 0.00156 ardsw = -800 aua = -0.4
+ aud = -0.005 avsat = 3E+005 avsat1 = 3E+005 aptwg = 2.3 amexp = -0.25
+ bg0sub = 1.12 bgidl = 1.122E+009 bgisl = 3E+008 bigc = 0.0017 bigd = 0.0017
+ bigs = 0.0017 bua = 5.3E-008 bud = 4E-006 brdsw = 5.2E-008 bvsat = 4.3E-008
+ bvsat1 = 4.3E-008 bptwg = 4E-007 bmexp = 0.15 cdsc = 0.023 cdscd = 0.0001
+ cfd = 2E-011 cfs = 2E-011 cgbl = 0 cgbo = 0 cgdl = 0 cgdo = 1E-010
+ cgsl = 0 cgso = 1E-010 cigc = 0.075 cigd = 0.075 cigs = 0.075 cit = 3E-005
+ ckappad = 0.6 ckappas = 0.6 cth0 = 1.243E-006 deltavsat = 1 deltaw = 0
+ deltawcv = 0 dlbin = 0 dlc = 0 dlcigd = 1E-009 dlcigs = 1E-009 drout = 20
+ dsub = 0.1001 dvt0 = 0.2 dvt1 = 0.2 dvtshift = 0 easub = 4.05 egidl = 0.4009
+ egisl = 0.2 eot = 2.2E-009 eotacc = 2.2E-009 eotbox = 1.45E-007 epsrox = 4.43
+ epsrsp = 3.9 epsrsub = 11.9 eta0 = 0.1 etamob = 4.6 etaqm = 0.54 eu = 1.47
+ fpitch = 2E-007 hfin = 6.5E-008 igt = 2.5 k1rsce = 0 ksativ = 0.92 kt1 = 0
+ kt1l = 0 lint = 7E-009 lpe0 = 0 lpa = 0.9501 lcdscd = 5E-005 lcdscdr = 5E-005
+ ll = -3.3E-008 lln = 1 mexp = 8 nbody = 1E+018 nc0sub = 2.86E+025
+ ni0sub = 1.1E+016 nigc = 1 nsd = 2E+026 pclm = 0.008 pclmcv = 0.013 pclmg = 0
+ pclmgcv = 0 pdibl1 = 1.749 pdibl2 = 0.0003 phig = 4.306 phin = 0.05
+ poxedge = 1.1 pqm = 0.66 prt = 0 prwg = 0 ptwg = -0.08 ptwgt = 0.004
+ pvag = 1.02 qm0 = 0.001 qmfactor = 2.5 rdsw = 514 rdswmin = 0
+ rdwmin = 0 rshd = 0 rshs = 0 rswmin = 0 rth0 = 0.225 tbgasub = 0.000473
+ tbgbsub = 636 tgidl = -0.007 tmexp = 0 tnom = 25 toxp = 2.5E-009 u0 = 0.064
+ ua = 0.18 ua1 = 0.001032 ucs = 1 ucste = -0.004775 ud = 0.2 ud1 = 0 up = 1E-008
+ ute = 0 utl = -0.0015 vasat = 0.5 vsat1 = 3.8E+004 vasatcv = 0.2
+ vsat = 3.8E+004 wr = 1 wth0 = 2.6E-007 xl = 0

ends BSIM_CMG
```

APPENDIX B PARAMETER EXTRACTION PLOTS

B.1 Suciu-Johnston Method

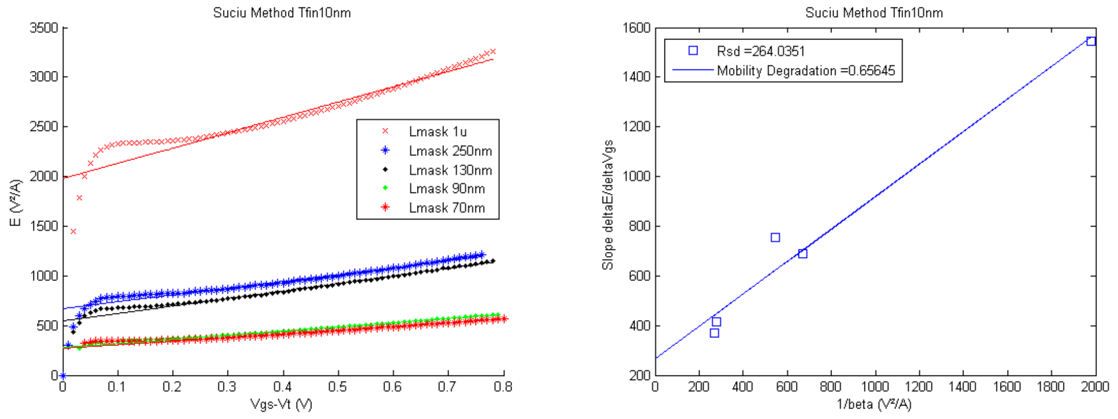

Figure B.1: Extraction of the series resistance for FinFETs with 10nm of fin thickness using the Suciu-Johnston method

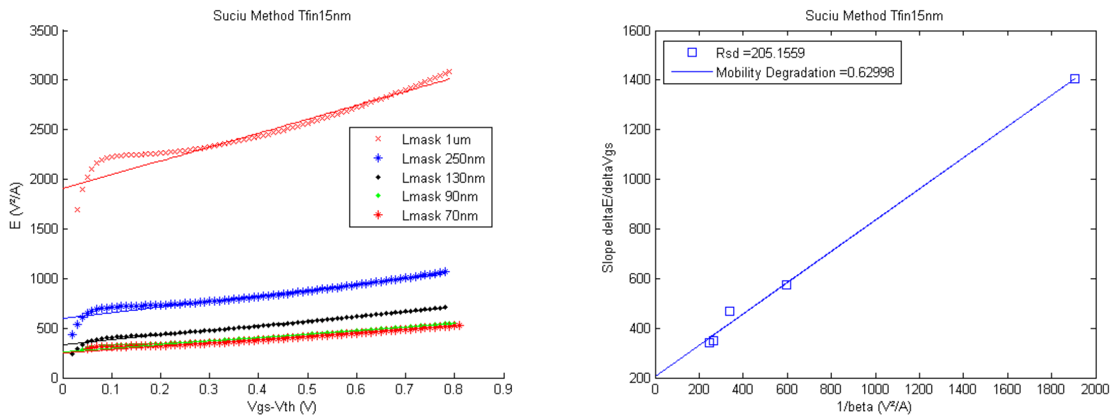

Figure B.2: Extraction of the series resistance for FinFETs with 15nm of fin thickness using the Suciu-Johnston method

B.2 Torres-Torres Method

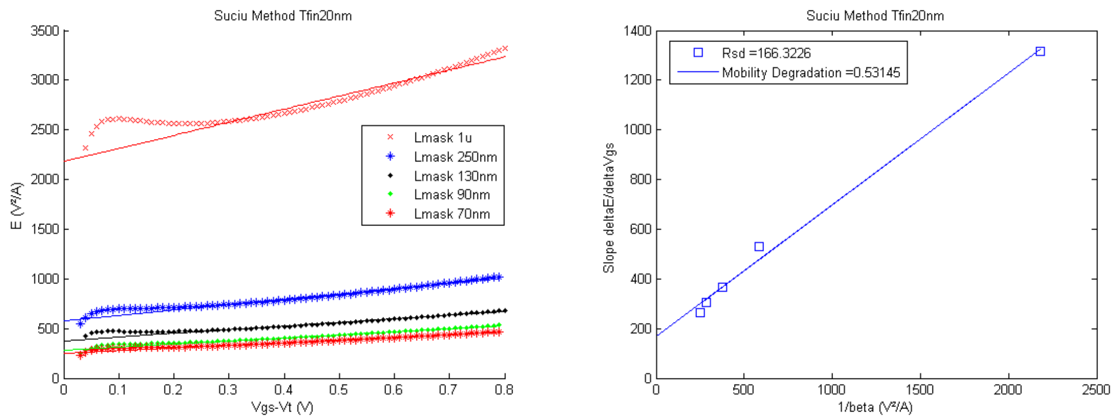

Figure B.3: Extraction of the series resistance for FinFETs with 20nm of fin thickness using the Suciu-Johnston method

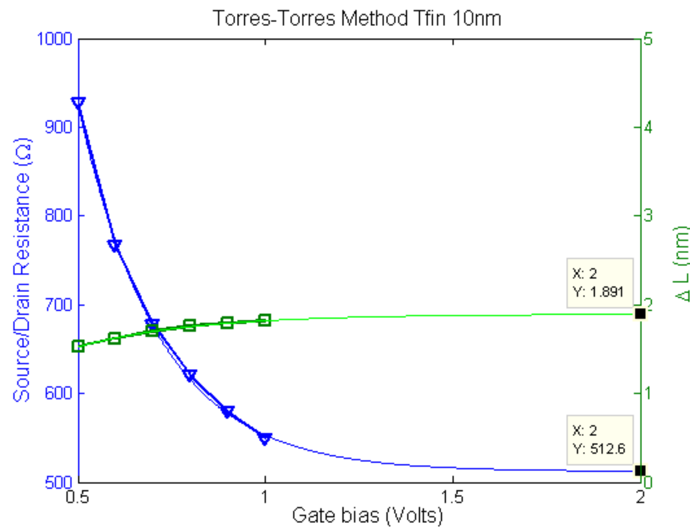

Figure B.4: Extraction of the series resistance for FinFETs with 10nm of fin thickness using the Torres-Torres method, including the variation with gate bias and the extrapolation to higher overdrives.

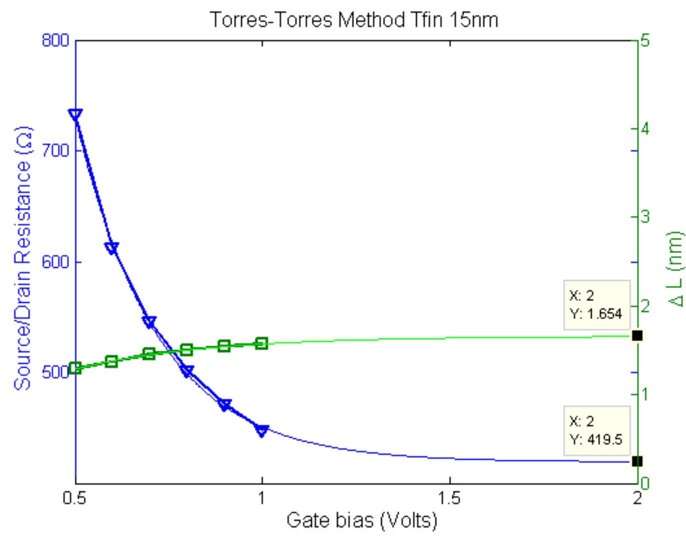

Figure B.5: Extraction of the series resistance for FinFETs with 15nm of fin thickness using the Torres-Torres method, including the variation with gate bias and the extrapolation to higher overdrives.

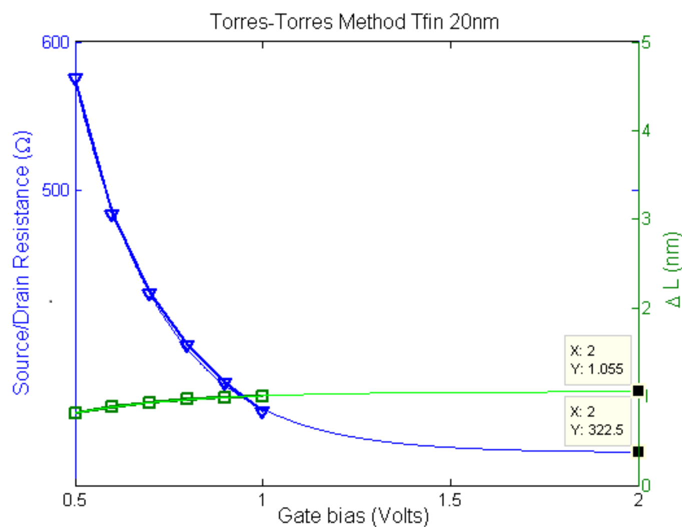

Figure B.6: Extraction of the series resistance for FinFETs with 20nm of fin thickness using the Torres-Torres method, including the variation with gate bias and the extrapolation to higher overdrives.

APPENDIX C BSIM-CMG DEVICE MODELLING

C.1 10nm FinFETs

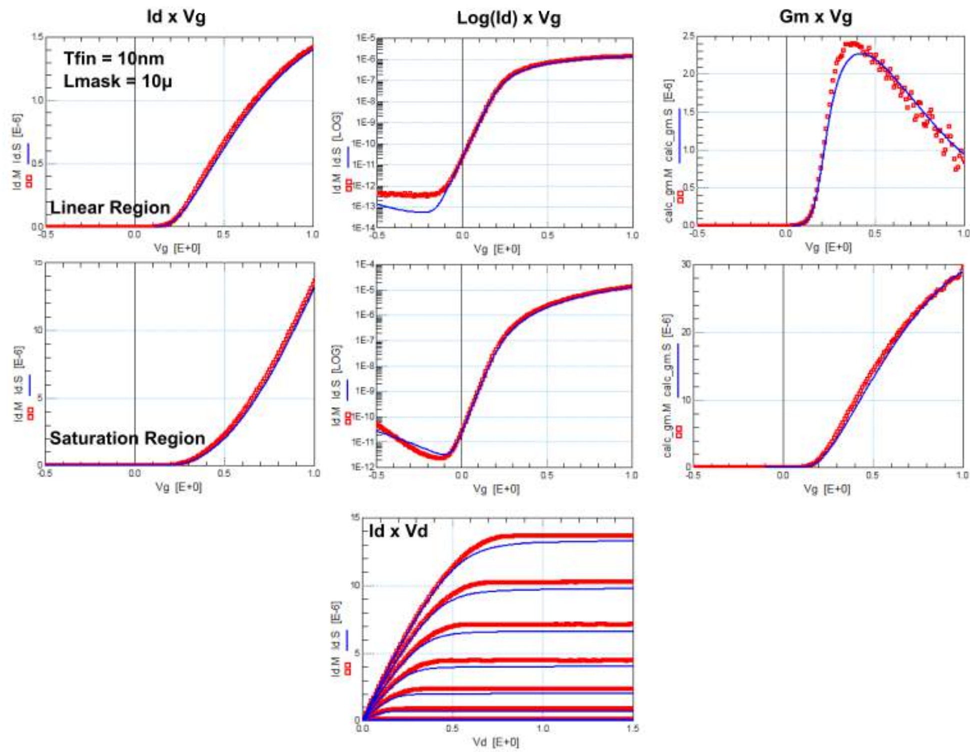

Figure C.1: Modelling of a FinFET with T_{fin} = 10nm and L_{mask} = 10µm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

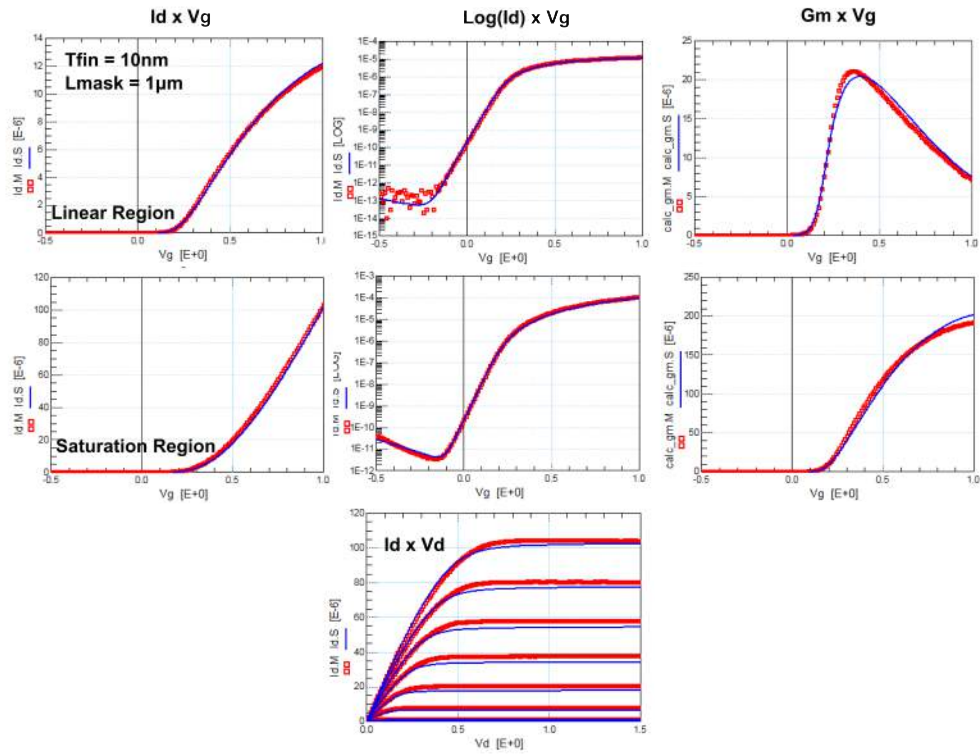

Figure C.2: Modelling of a FinFET with T_{fin} = 10nm and L_{mask} = 1µm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

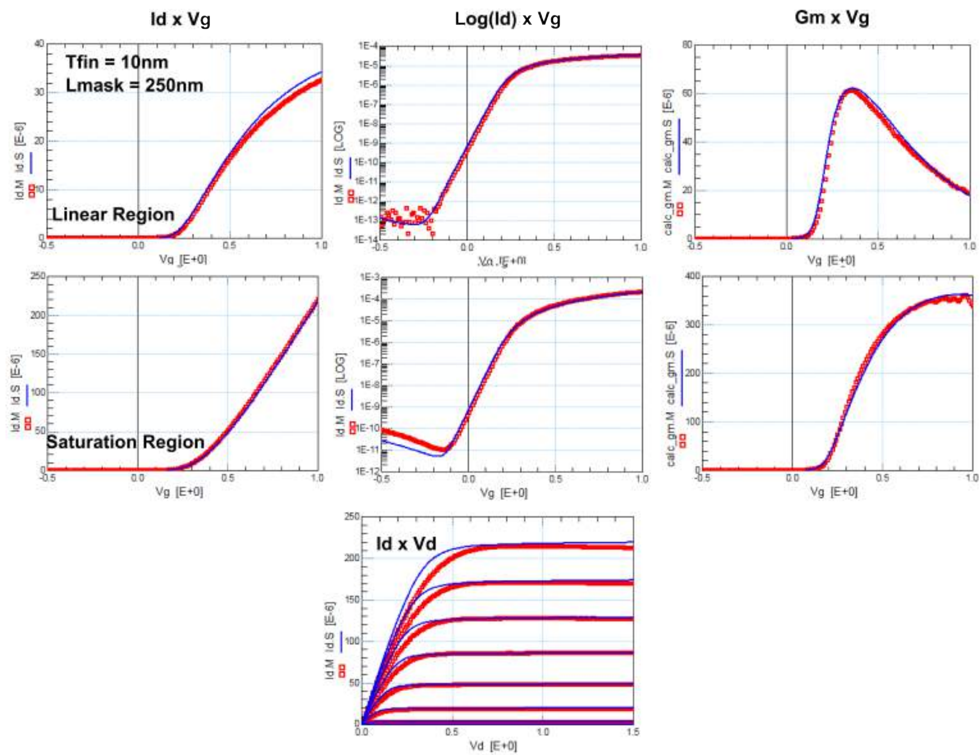

Figure C.3: Modelling of a FinFET with T_{fin} = 10nm and L_{mask} = 250nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

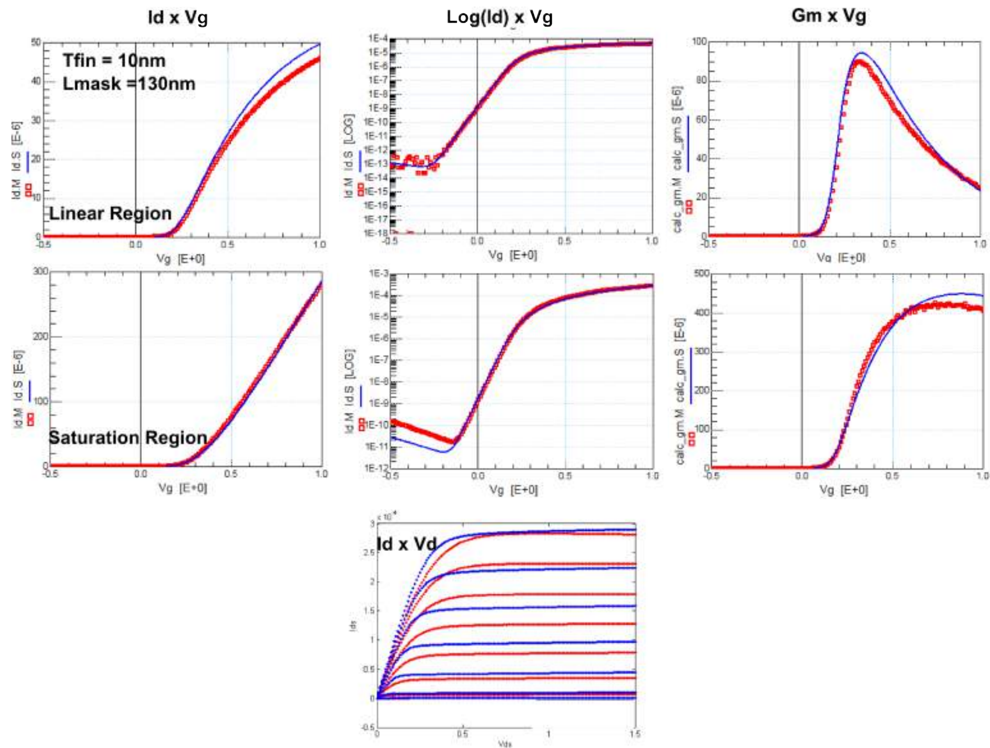

Figure C.4: Modelling of a FinFET with T_{fin} = 10nm and L_{mask} = 130nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

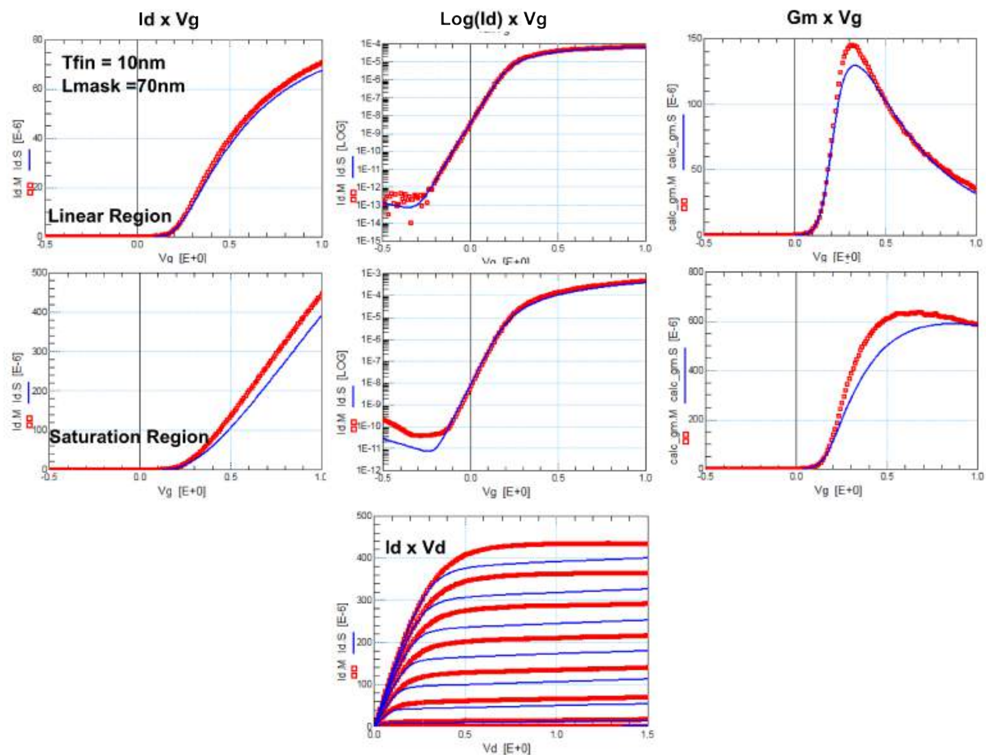

Figure C.5: Modelling of a FinFET with T_{fin} = 10nm and L_{mask} = 70nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

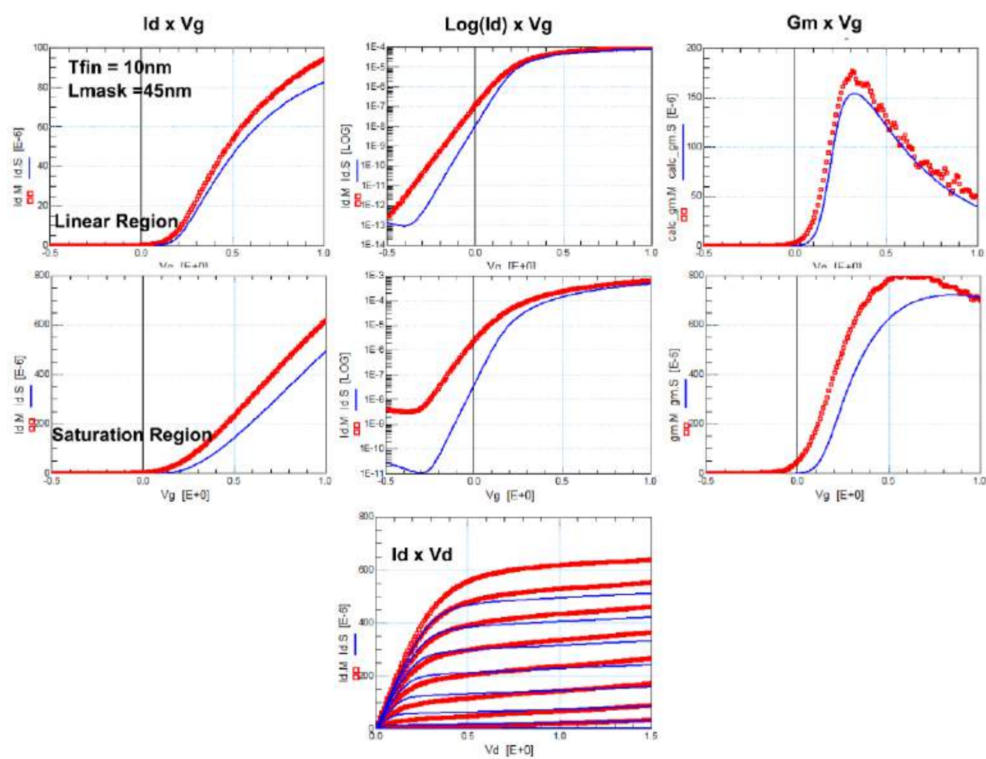

Figure C.6: Modelling of a FinFET with T_{fin} = 10nm and L_{mask} = 45nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

C.2 15nm FinFETs

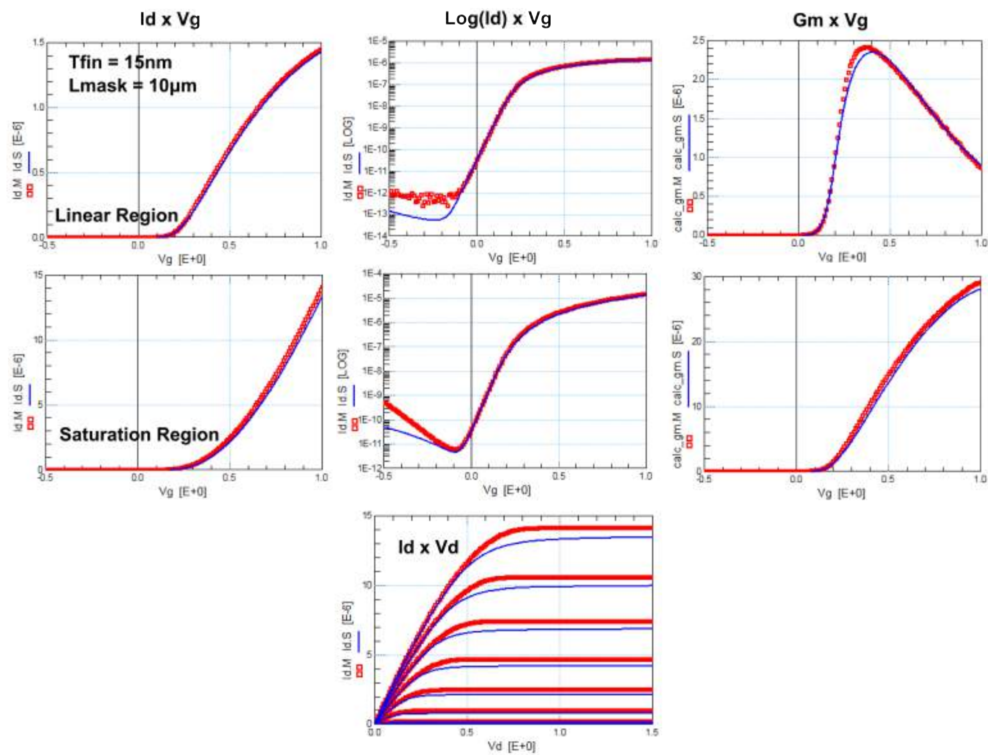

Figure C.7: Modelling of a FinFET with T_{fin} = 15nm and L_{mask} = 10µm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

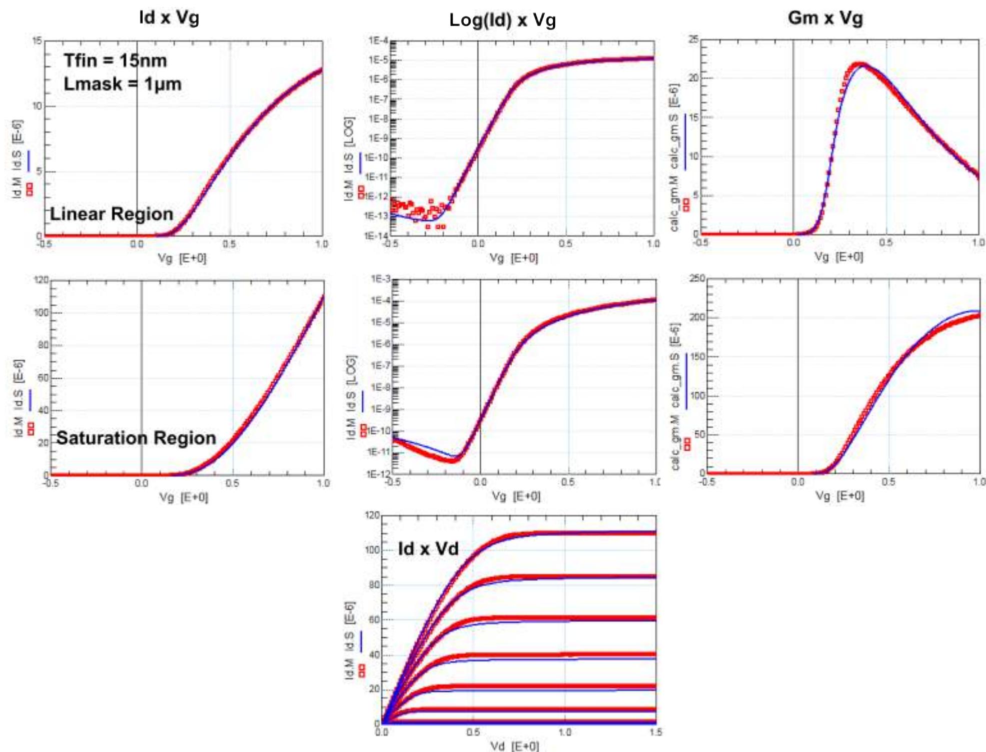

Figure C.8: Modelling of a FinFET with T_{fin} = 15nm and L_{mask} = 1µm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

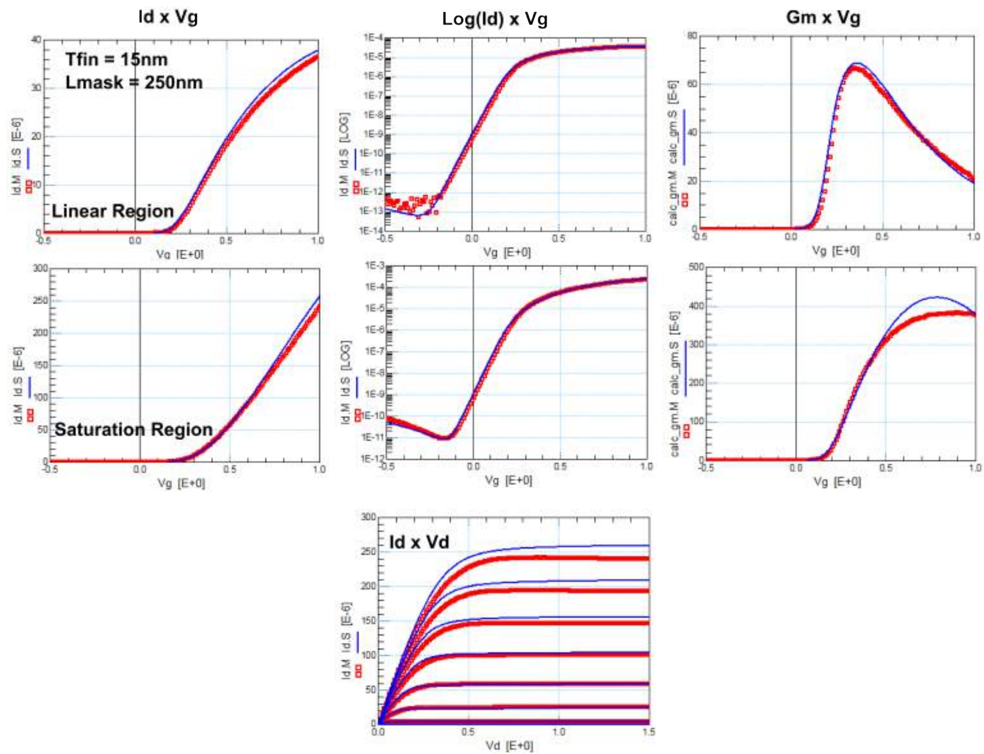

Figure C.9: Modelling of a FinFET with T_{fin} = 15nm and L_{mask} = 250nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

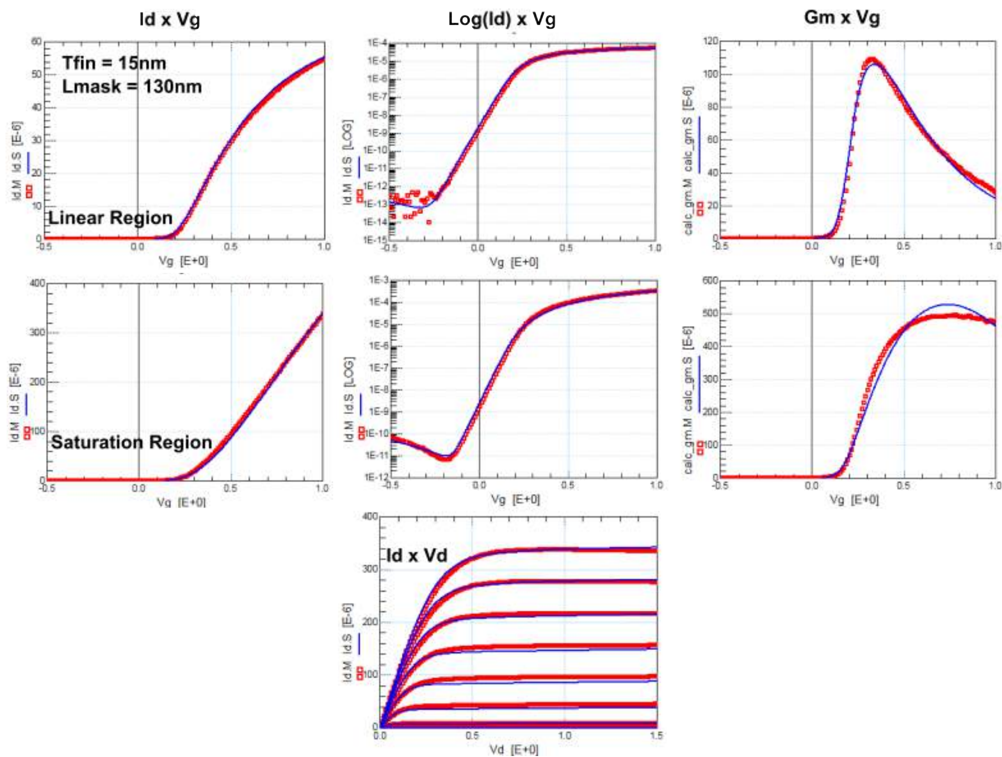

Figure C.10: Modelling of a FinFET with T_{fin} = 15nm and L_{mask} = 130nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

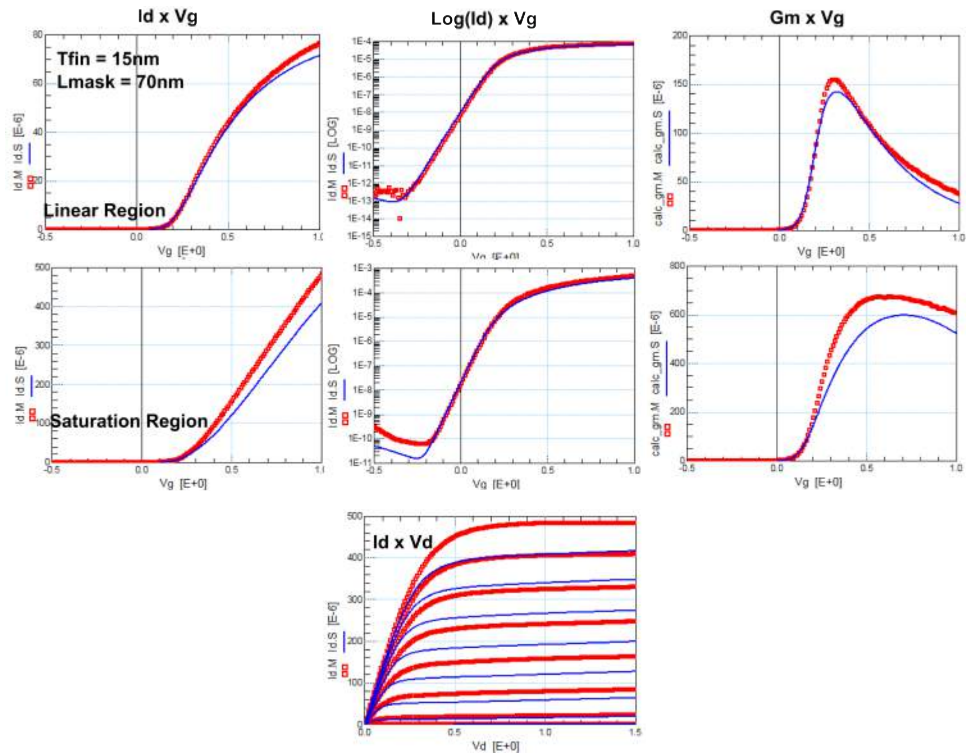

Figure C.11: Modelling of a FinFET with T_{fin} = 15nm and L_{mask} = 70nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

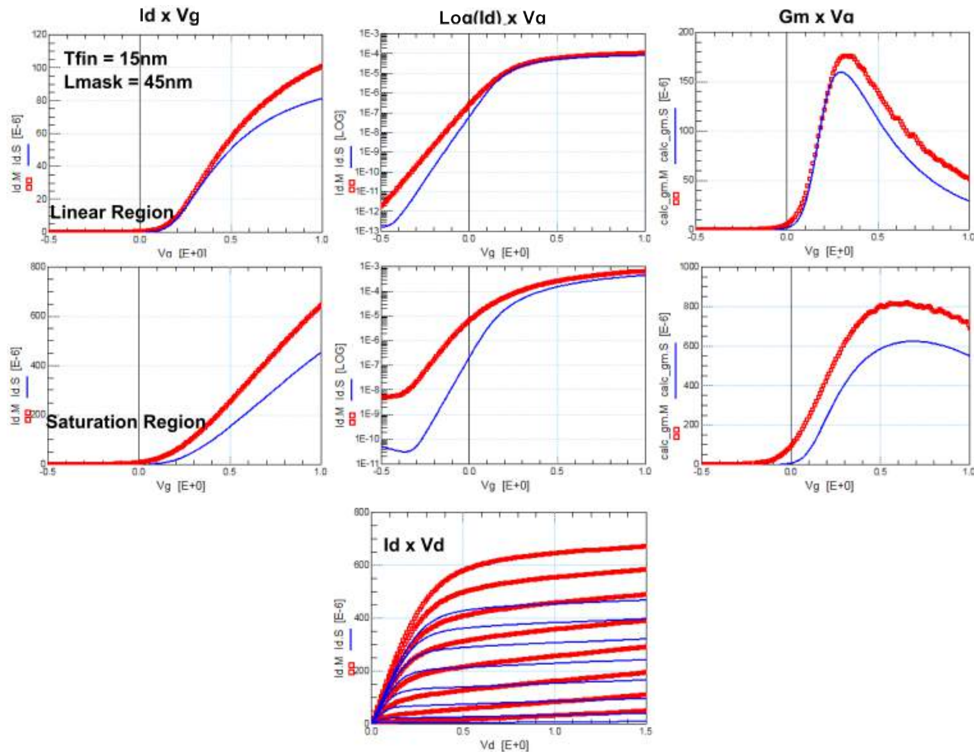

Figure C.12: Modelling of a FinFET with T_{fin} = 15nm and L_{mask} = 45nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

C.3 20nm FinFETs

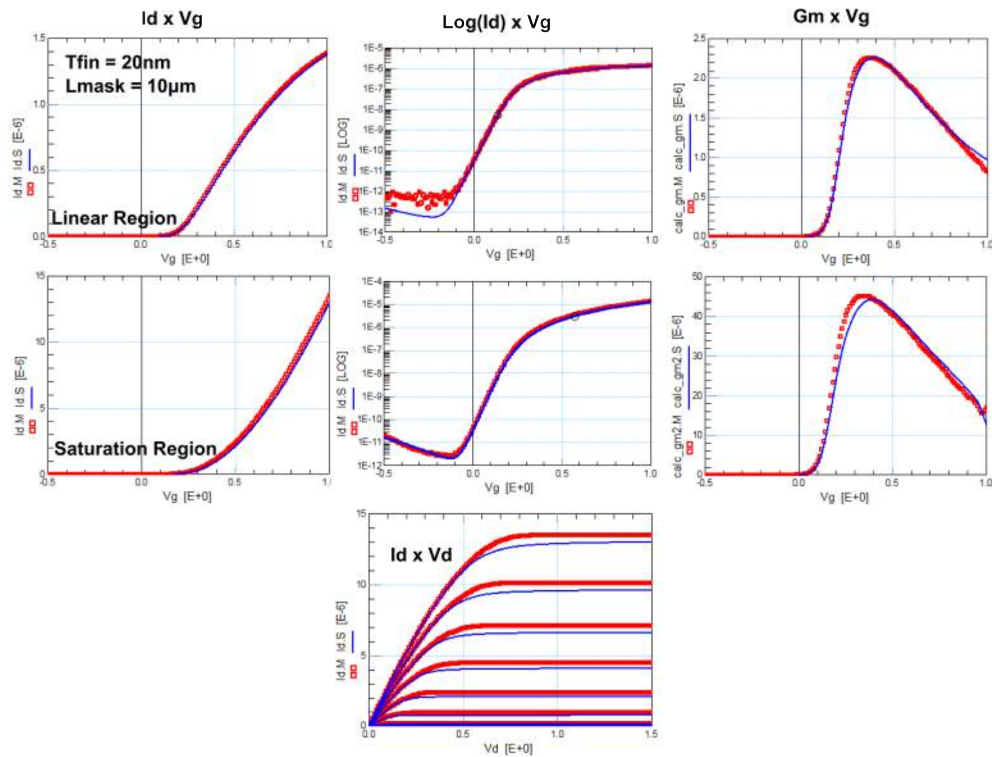

Figure C.13: Modelling of a FinFET with T_{fin} = 20nm and L_{mask} = 10µm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

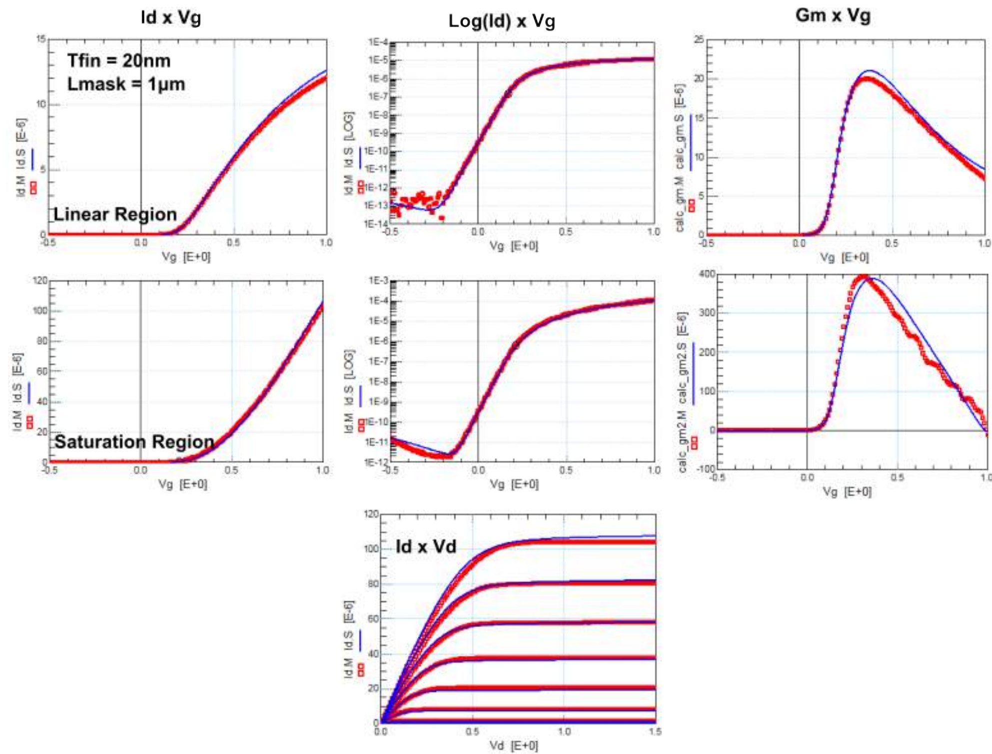

Figure C.14: Modelling of a FinFET with T_{fin} = 20nm and L_{mask} = 1µm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

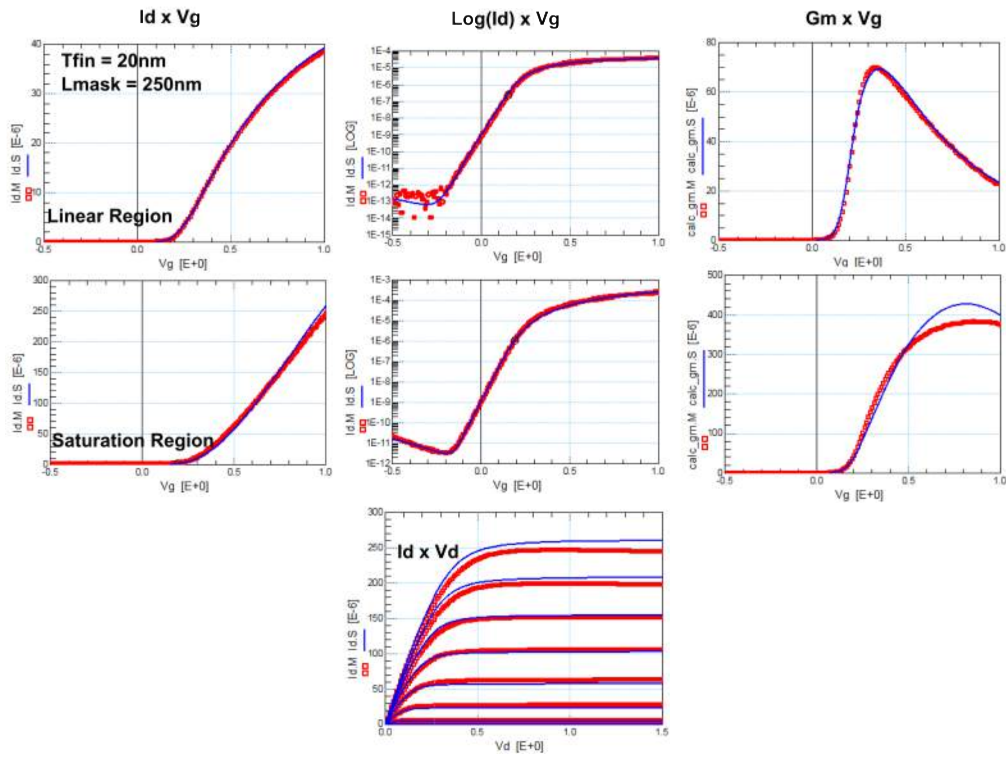

Figure C.15: Modelling of a FinFET with T_{fin} = 20nm and L_{mask} = 250nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

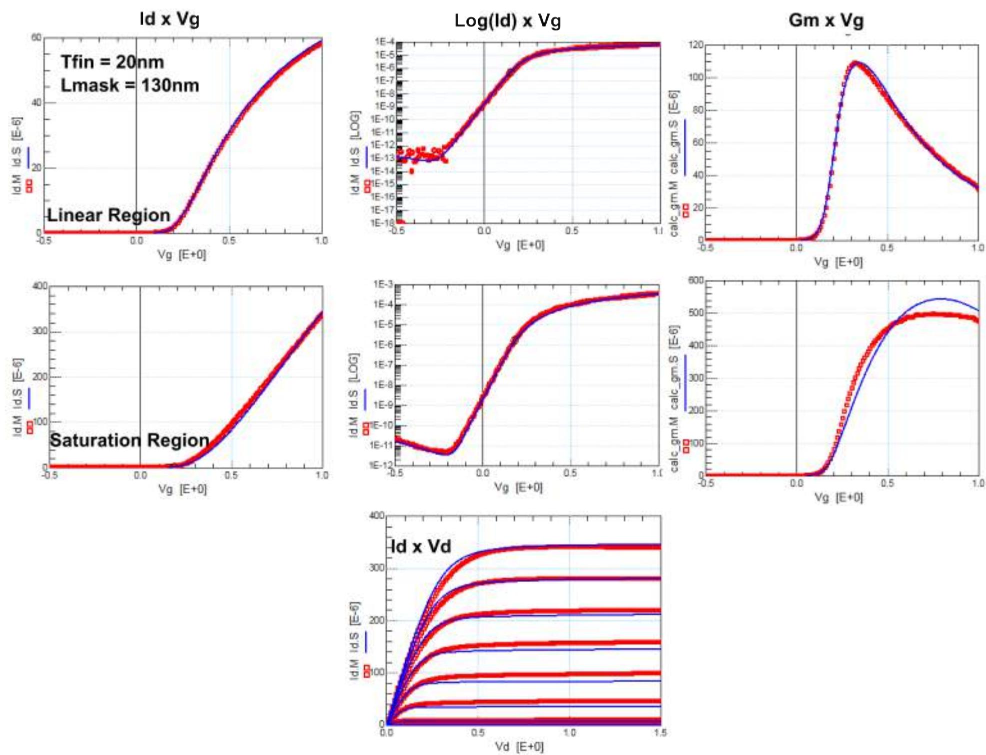

Figure C.16: Modelling of a FinFET with T_{fin} = 20nm and L_{mask} = 130nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

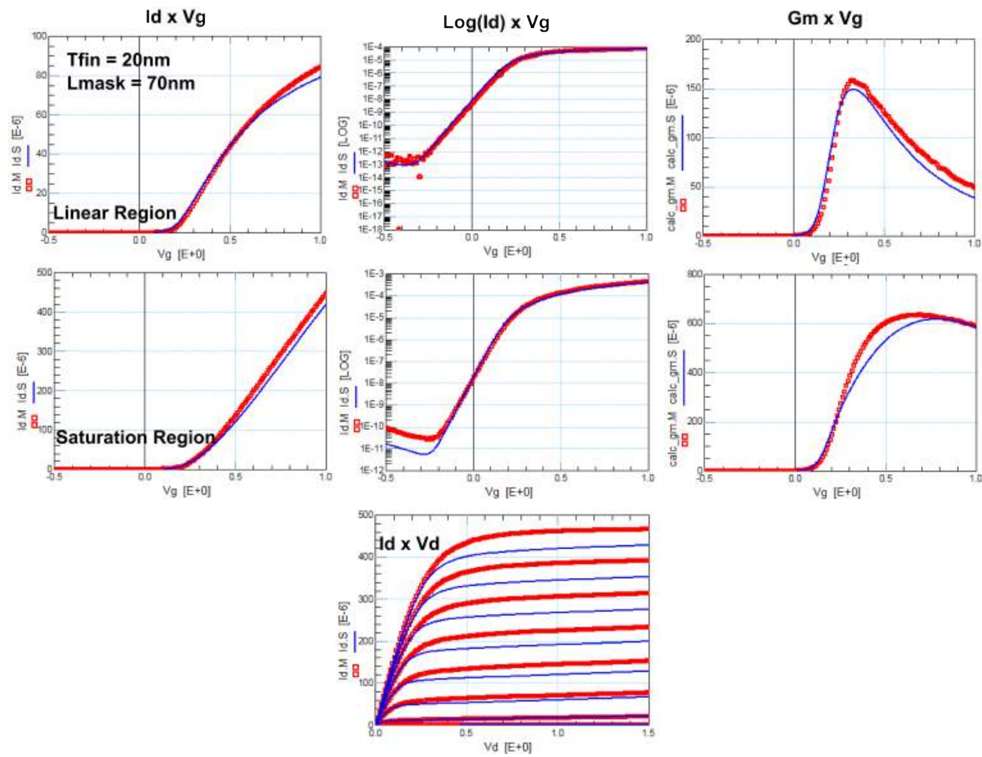

Figure C.17: Modelling of a FinFET with T_{fin} = 20nm and L_{mask} = 70nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.

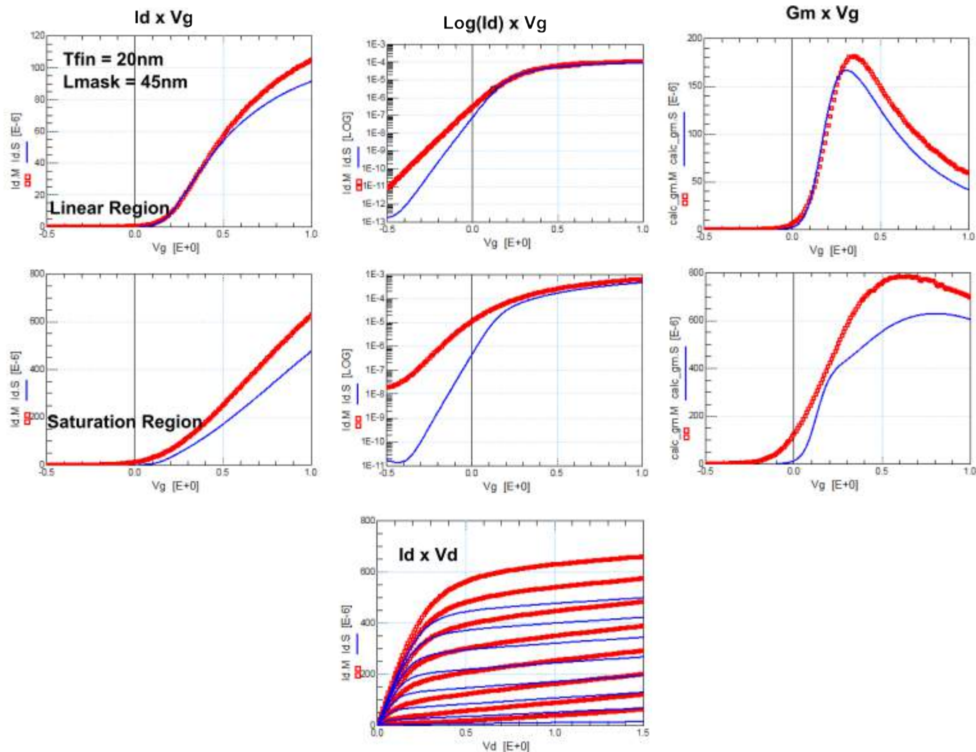

Figure C.18: Modelling of a FinFET with T_{fin} = 20nm and L_{mask} = 45nm in all operation regions. Measured points are the small red squares and simulated data is the solid blue line.