

UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM COMPUTAÇÃO

ADÃO ANTONIO DE SOUZA JUNIOR

**Digital Approach for the Design
of Statistical Analog Data
Acquisition on SoCs**

Thesis presented in partial fulfillment of the
requirements for the degree of Doctor of
Computer Science.

Prof. Dr. Luigi Carro
Advisor

Porto Alegre, julho de 2005.

CIP – CATALOGAÇÃO NA PUBLICAÇÃO

Souza Junior, Adão Antonio de

Digital Approach for the Design of Statistical Data Acquisition on SoCs / Adão Antonio de Souza Junior. – Porto Alegre: Programa de Pós-Graduação em Computação, 2005.

86 f.:il.

Thesis (PhD) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Computação, Porto Alegre, BR – RS, 2005. Advisor: Luigi Carro.

1.ADC. 2. Stochastic quantization. 3.Mixed-signal systems. 4.Design space exploration. 5. Adaptive filtering. 6.Analog test. 7.Fault-tolerance. I. Carro, Luigi. II. Título.

UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL

Reitor: Prof. José Carlos Ferraz Hennemann

Vice-Reitor: Prof. Pedro Cezar Dutra Fonseca

Pró-Reitora de Pós-Graduação: Profa. Valquiria Linck Bassani

Diretor do Instituto de Informática: Prof. Philippe Olivier Alexandre Navaux

Coordenador do PPGC: Prof. Flávio Rech Wagner

Bibliotecária-Chefe do Instituto de Informática: Beatriz Regina Bastos Haro

ACKNOWLEDGEMENTS

First, I wish to thank my parents Adão Antonio de Souza e Rosa Conceição Espindola de Souza, for all their support, unrestricted friendship, dedication and love. I have no doubt that without their caring advices the journey would be much harder. I also must thank my sisters Daya, for being such a good friend, and Jana for having such a huge heart. Also, I must say that in the last two years my life has been turned around, for the best. I am immensely grateful to the woman that made it happen, my love, Rovená.

I certainly want to thank my advisor Professor Luigi Carro, for the many discussions, inspiring suggestions (a.k.a crazy ideas) and for many times believing in me more than myself. I have worked with him since graduation, and I can surely say it has never been boring. Thanks are due to my colleague Marcelo Negreiros, who helped me in many different ways to develop the theme of this thesis and Leticia Guimarães, for cheering things up, whenever one of us gets too grumpy.

There are many people in the Signal Processing Lab (LaPSI), that I also want to acknowledge: the graduation students Thiago Figueiro, Nivea Schuch, Viviane, Davi “Copperfield”, among others, and the master students Josias Mainardi, Erik Schüller, Carla Diniz, and all the other ex-LaPSI warriors with whom I had the pleasure to share the workspace: Maria da Gloria Cataldi Flores, Adriane Parraga, and Osvaldo Betat.

Also I would like to thank Professors Altamiro Susin for always finding a way to make the most unlikely question, which sometimes turns out to have the most rewarding answer; and Professor Adalberto Schuch Jr. for selling me such a good bass guitar. While working through the classes in the first years at the Instituto de Informatica, many people have made me feel at home. I would like to thank André Borin, Erika Cota, Marcio Kreutz, Eric Fabris and Fernanda Lima.

At last I must acknowledge CAPES, for the scholarship grant that supported this research.

TABLE OF CONTENTS

LIST OF ABBREVIATIONS AND ACRONYMS	7
LIST OF FIGURES.....	9
LIST OF TABLES	12
ABSTRACT.....	13
RESUMO.....	14
1 INTRODUCTION: FUTURE CHALLENGES	15
1.1 Mixed-signal and Embedded Systems Design Cycle.....	15
1.2 The Moore’s Law Factor	16
1.3 Trends at Higher Integration Scales.....	17
1.4 System Specification and Design Issues.....	18
1.5 Treating Analog Blocks as a Modeling Problem.....	20
1.6 A Handful of Problems	21
2 STOCHASTIC QUANTIZATION FOR STATISTICS ACQUISITION.....	23
2.1 Highly Digital ADCs Architecture.....	23
2.1.1 Flash Converters.....	23
2.1.2 Stochastic Converters	24
2.1.3 Delta Sigma Converters.....	24
2.1.4 Time-delay Converters	25
2.2 Statistical Sampler Operation.....	26
2.2.1 Hard-limited Sum of Signal and Noise	26
2.2.2 Quasi-static Acquisition	28
2.2.3 Convergence to the Expected Resolution	29
2.2.4 Statistical Sampler and Linearity	30
2.2.5 Non-linear Mapping, Convergence and Linearity	31
2.3 Number of Bits and PSD	34
3 RANDOM SIGNAL GENERATORS	36
3.1 True Random Signal Generator	36
3.2 Chaotic Circuit	36
3.3 Providing Several Uncorrelated Noise Sources.....	36
3.4 Pseudorandom Circuit with Sampling	36
3.5 PDF of a Periodic Signal	36
3.5.1 An Example: Calculating the PDF of a Sinusoidal Signal	41

4 PRACTICAL APPLICATIONS	42
4.1 Bridge Circuit with Differential Acquisition.....	42
4.2 Analog Acquisition with Pseudo-random Generation	44
4.3 Linearization through Non-Uniform Sampling	48
5 UNFOLDING THE DESIGN LANDSCAPE	51
5.1 Redundancy and Performance of ADCs	51
5.2 Parallel Statistical Sampler - PSS.....	52
5.3 Self-test and Fault Tolerance Issues	54
5.3.1 ADC Self-configuration with Pseudorandom Noise.....	55
5.3.2 ADC Self-configuration with Gaussian Noise.....	57
5.4 Generalized Parallel Statistical Sampler - GPSS	58
5.5 Filtering Techniques.....	61
5.5.1 Self-correlation Adaptive Filter Topology	62
5.5.2 Hybrid Topology.....	63
5.6 Practical Applications	64
5.6.1 A PSS with Four Comparators.....	64
5.6.2 Using Adaptive Filtering to Improve SS-ADC Performance	66
6 A COMPARISON WITH OTHER CONVERTERS	68
6.1 Time and Resolution	68
6.2 Area and Resolution.....	70
7 FINAL REMARKS	72
7.1 Application Specific Analog Acquisition - ASAA	72
7.2 Target Applications.....	73
7.2.1 Low Frequency Instrumentation	73
7.2.2 Passive Sensors	73
7.2.3 Analog Test.....	74
7.2.4 Fault-Tolerant Acquisition.....	74
7.2.5 Pattern Processing in Embedded Analog Data Arrays	74
7.3 Hardware Features and Architectures.....	74
7.3.1 Analysis of the Elementary Blocks	75
7.3.2 Parallelism and Reconstruction Models	75
7.3.3 Redundancy and Self-Configuration and the Area/Frequency Tradeoff.....	75
7.3.4 Defining a Complete Path Using Statistical Samplers with more than One Bit.	75
7.4 Modeling Techniques	75
7.5 Original Contributions.....	76
7.6 Open Research Issues.....	77
REFERENCES.....	79
APPENDIX RESUMO DA TESE EM PORTUGUÊS.....	85

LIST OF ABBREVIATIONS AND ACRONYMS

α	Number of independent analog references in a fault-tolerant converter
β	Number of parallel comparators in a PSS
γ	Multilevel or analog reference
$\Phi(v)$	Non-linear function that replicates the behavior of a given statistical sampler
$\Gamma(m)$	Linearization function for a given statistical sampler
$\mu(x)$	Mean value of variable x
$P(x)$	Probability distribution function (PDF) of variable x
p	Pulses in the output of the comparator
m	Output of the moving average with depth N applied over p
s	Output of the subtraction of the reference from the input
v	Analog input to the ADC
AD	Analog to Digital
ADC	Analog to Digital Converter
ANG	Analog Noise Generator
ASAA	Application Specific Analog Acquisition
ASICs	Application Specific Integrated Circuits
BIST	Built In Self Test
CF	Carachteristic Function
CUT	Circuit Under Test
DA	Digital to Analog
DfT	Design for Testability
DFT	Discrete Fourier Transform
DNL	Differential Non-Linearity
DSP	Digital Signal Processing
DUT	Device Under Test
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array

GPSS	Generalized Parallel Statistical Sampler
INL	Integral Non-Linearity
LFSR	Linear Feedback Shift Register
PDF	Probability Distribution Function
PSD	Power Spectral Density
PSS	Parallel Statistical Sampler
RF	Radio Frequency
SNR	Signal to Noise Ratio
SoC	System On a Chip
SS	Statistical Sampler
SS-ADC	Statistical Sampling Analog to Digital Converter
TD-ADC	Time-Delay Analog to Digital Converter

LIST OF FIGURES

Figure 1.1: An hypothetic mixed-signal design process; according to Kundert (2001), a study performed by Collett International in 1997 with 21 design firms, has shown that analog blocks in mixed-signal designs can consume three to seven times the man-hour amount of digital ones; productivity variations can reach fourteen times.	16
Figure 1.2: Resources ratio in a hypothetical mixed-signal system as a function of time, as predicted by ITRS FoMs.....	18
Figure 1.3 : Major challenges for future analog data acquisition within mixed-signal systems.....	20
Figure 1.4 : Compensating ADC non-idealities on the digital domain.....	21
Figure 2.1 : Relationship between properties of v and p for different situations, read text to further explanations. (a) Spectra. (b) Constant values of v and corresponding $\mu(p)$	26
Figure 2.2 : Stochastic quantization as the hard-limited sum of analog signals.....	27
Figure 2.3 : Calculating the relationship between the N-cycles average m of the pulse-stream p and the input value v . Since m is an estimator of $\mu(p)$ one can use it to infer the value of v	29
Figure 2.4 : As the number of averages N increases, error scattering is restricted, allowing an approximation of the input value with a higher resolution.	30
Figure 2.5 : Linearization through non-linear mapping of the output. (a) One compensates the non-ideal behavior of the acquisition in the digital domain after averaging. (b) Given the Φ (gray), the ideal linearization function Γ is defined (black).....	31
Figure 2.6 : Resolution over the dynamic range for a Gaussian reference, plot shows averaging output m and linearized output y . Averaging depth $N = 10$ and $N = 10.000$ cycles.....	32
Figure 2.7 : Averaging/resolution relationship: (a) for uniform noise; (b) for Gaussian noise.	34
Figure 2.8 : Statistical sampler with $N = 128$: (a) a two-tone statistical sampler acquisition using the PSD of the pulse-stream ($S(p)$) using a 105 points – FFT. (b) Slope acquisition with the same sampler and the same number of comparators and averages	35
Figure 3.1 : Thermal noise based, true random signal generator.	36
Figure 3.2 : True random signal generator using the chaotic Chua circuit.	37
Figure 3.3 : Pseudorandom scrambling to generate several noise sources. Signals $si_1, si_2, \dots, si_\beta$ are pulses that are high when the time slot counter reaches the values i_1, i_2, \dots, i_β respectively.....	38

Figure 3.4 : Splitting a single true random noise generator into a series of uncorrelated multilevel sequences. Using this architecture provides more uncorrelated references than a simple delay chain.	38
Figure 3.5 : Sampling a periodic signal to generate multilevel pseudo-random noise... ..	39
Figure 3.6 : Within the analog signal period, any sampling slot can be selected, if each interval have the same probability to be selected (given a uniform distribution for the random sequence i) the resulting output distribution will be determinate by the analog PDF of the reference.....	40
Figure 3.7 : Estimating the PSD for a periodic signal.	40
Figure 3.8 : Periodic signal with highly irregular shaped period.	41
Figure 4.1 : Resistive bridge, with one variable element, v_{REF} is a constant reference. .	42
Figure 4.2 : Differential bridge acquisition setup: the noise source presents a Gaussian distribution.	43
Figure 4.3 : Matching of the points measured with the expected linearized values of m . (a) Shows the typical <i>erf</i> shaped output plot; (b) estimated values of r after linearization.....	45
Figure 4.4 : Setup for the SS-ADC with a pseudorandom reference.....	45
Figure 4.5: The shadowed area represents $P(\gamma)$ for different relations between the time constants for the rise τ_{LH} and fall cycles τ_{HL} of a ref : $\tau_{LH} = \tau_{HL}$ (a), $\tau_{LH} > \tau_{HL}$ (b), $\tau_{LH} < \tau_{HL}$ (c). Parametric variations on the reference generator can be compensated by tuning the digital linearization model.	46
Figure 4.6: Theoretical model and averaged input/output mapping. The model reproduces the expected circuit input/output behavior for each comparator (function $\Phi(v)$) before linearization. (a) $\Phi(v)$ follows a big mismatch between τ_{HL} and τ_{LH} in the reference (60%). (b) $\Phi(v)$ follows non-linearity variations with different values for the generator constants (τ_{HL} and τ_{LH}). .	47
Figure 4.7: Outputs $y = \Gamma(m)$ - the dashed lines show the model outcome for $\pm 10\%$ parametric variations in the references. Solid lines show final outputs after zero subtraction.	48
Figure 4.8: A comparison between the slope acquisition with non-uniform sampling with a roulette function $W(n)$ and using a linearization function $\Gamma(m)$. The gray line shows the output of the non-uniform sampling method and the black the output of the post-linearization method.	50
Figure 5.1: Using redundancy to improve performance in a flash ADC	52
Figure 5.2: Multiple reference offset impact on the average output of each comparator.	53
Figure 5.3: Multiple reference deviation impact on the average output of each comparator.....	54
Figure 5.4: PSS architecture (a) with a single analog reference and pseudo-random scrambling and (b) with separate and uncorrelated analog generators.....	54
Figure 5.5: Complete PSS architecture employing a pseudo-random reference generator.	56
Figure 5.6: Measuring the real parameters of the analog reference to adjust the linearization. (a) Measure T_{HL} . (b) Measure T_{LH}	56
Figure 5.7: Acquisition with variation in the Gaussian reference distribution. (a) shows the outcome before linearization, and (b) after applying the ideal function $\Gamma(m)$	57
Figure 5.8: GPSS architecture: α , β , N , and l are design parameters.	58

Figure 5.9: Matching of the model in a GPSS and simulated results using a single Gaussian reference with standard deviation 0.5 ($\alpha=1$, $\beta=10$, $N=1000$, $l=2$).	62
Figure 5.10: Resolution behavior as a function of the factor of parallelism (β) and the resolution of the CE blocks	60
Figure 5.11: Analog area estimates a function of CE' resolution and β	61
Figure 5.12: Using the adaptive modeling approach to improve SS-ADC.....	64
Figure 5.13: Self-correlation adaptive filter structure.....	65
Figure 5.14: Four parallel comparators acquisition setup (a) two noise sources are turned into four using analog inverters, (b) acquisition uses digital channels of the HP54645D oscilloscope.	65
Figure 5.15: Four comparators acquisition. Each channel generates a different gray erf plot. After subtracting zero and using the linearization function Γ , one has four linear mappings of the input, that added together result the final output (in black). Output resolution matches the theoretical.	65
Figure 5.16: Resolution and number of comparators using Gaussian noise.	66
Figure 6.1: Using a single SS-ADC to acquire multiplexed inputs.....	70
Figure 7.1: Proposed project flow for an application specific analog acquisition design process within mixed-signal systems.....	72
Figure 7.2: Main applications for the proposed system. The gray box in the extreme right marks an area of possible further developments.	73
Figure 7.3: Hardware blocks and feature variation issues.	74
Figure 7.4: Digital modeling techniques: The gray box shows possible future research.	76

LIST OF TABLES

Table 5.1: Single tone results with statistical sampling and adaptive filtering	63
Table 5.2: Two-tone acquisition results as a function of the signal bandwidth.	63
Table 5.3: Hybrid model results, parameter mismatch is assumed as a 20% variation..	64
Table 5.4: Adaptive filter approach result with acquired data	67
Table 6.1: Area and resolution for the ADC architectures.....	70
Table 6.2: Estimated area for an eight bits ADC on .35 μ m CMOS	71

ABSTRACT

With the current demand for mixed-signal SoCs, an increasing number of designers are looking for ADC architectures that can be easily implemented over digital substrates. Since ADC performance is strongly dependent upon physical and electrical features, it gets more difficult for them to benefit from more recent technologies, where these features are more variable. This way, analog signal acquisition is not allowed to follow an evolutionary trend compatible with Moore's Law. In fact, such trend shall get worst, since newer technologies are expected to have more variable characteristics.

Also, for a matter of economy of scale, many times a mixed-signal SoC presents a good amount of idle processing power. In such systems it is advantageous to employ more costly digital signal processing provided that it allows a reduction in the analog area demanded or the use of less expensive analog blocks, able to cope with process variations and uncertainty. Besides the technological concerns, other factors that impact the cost of the design also advise to transfer problems from the analog to the digital domain whenever possible: design automation and self-test requirements, for instance. Recent surveys indicate that the total cost in designer hours for the analog blocks of a mixed-signal system can be up to three times the cost of the digital ones.

This manuscript explores the concept of bottom-up analog acquisition design, using statistical sampling as a way to reduce the analog area demanded in the design of ADCs within mixed-signal systems. More particularly, it investigates the possibility of using digital modeling and digital compensation of non-idealities to ease the design of ADCs. The work is developed around three axes: the definition of target applications, the development of digital compensation algorithms and the exploration of architectural possibilities. New methods and architectures are defined and validated. The main notions behind the proposal are analyzed and it is shown that the approach is feasible, opening new paths of future research.

Keywords: ADC, stochastic quantization, mixed-signal systems, design space exploration, adaptive filtering, analog test, fault tolerance.

Uma Abordagem Digital para o Projeto de Aquisição Estatística de Dados Analógicos em Sistemas Integrados (SoCs)

RESUMO

Com a demanda atual por sistemas integrados híbridos, cada vez mais projetistas buscam arquiteturas de conversores A/D que tenham fácil implementação em tecnologia de processo digital. Como o desempenho de conversores A/D depende fortemente de características elétricas e físicas, se torna difícil para os mesmos tirar proveito integral das tecnologias mais recentes, onde estas características são mais variáveis. Deste modo a aquisição de sinais analógicos fica impossibilitada de seguir uma tendência evolutiva compatível com o caráter exponencial da Lei de Moore. De fato, essa tendência deve se agravar uma vez que as novas tecnologias terão características cada vez mais imprecisas.

Também, por razões de economia de escala, muitas vezes um sistema integrado apresenta uma boa capacidade de processamento ociosa. Nestes sistemas seria vantajoso utilizar um processamento digital mais custoso desde que esse permitisse uma diminuição da área analógica empregada ou o uso de componentes analógicos menos exigentes, compatíveis com variações de processo e incertezas. Pondo de lado as questões envolvendo a tecnologia de integração, outros fatores geradores de custo de projeto também aconselham que se transfiram problemas do domínio analógico para o digital sempre que possível: automação de projeto e a necessidade de auto-teste embarcado, por exemplo. Estudos recentes que apontam um custo em homens-hora para o projeto dos blocos analógicos em um sistema híbrido pode ser até três vezes maior que para os blocos digitais.

Este trabalho explora o conceito de projeto de aquisição analógica de baixo para cima (bottom-up), usando a amostragem de estatísticas (Statistical Sampling) como forma de reduzir os requisitos de área analógica para o projeto de conversores A/D em sistemas híbridos. Em particular se investiga a possibilidade de usar modelagem digital e compensação de não-idealidades para facilitar o projeto de conversores A/D. O trabalho é desenvolvido em três eixos: na definição de aplicações, no desenvolvimento de algoritmos de compensação digital e na exploração de arquiteturas. Novos métodos e arquiteturas são definidos e validados. As noções principais por trás da proposta são devidamente analisadas, demonstrando-se a viabilidade da abordagem e abrindo-se rotas para futura exploração.

Palavras-chave: conversores A/D, quantização estocástica, sistemas híbridos, exploração do espaço de projeto, filtros adaptativos, teste de sistemas analógicos, tolerância a falhas.

1 INTRODUCTION: FUTURE CHALLENGES

Interfacing between analog and digital domains in the context of mixed-signal SoC (Systems on Chip) design is nowadays a topic of extensive investigation. It is very likely that the existing gap between digital processing speeds, and the frequencies of acquisition of available ADCs is not about to narrow in the foreseeable future. In fact, chances are that, for compatible cost requirements, the existing gap will widen (WALDEN, 1999). Reasons for this trend are twofold: the best digital integration technology is always one or two generation ahead of the analog ones, and state-of-the-art digital technologies present intrinsic process variations that are a real challenge to the analog designer.

In this work ADC (Analog to Digital Converter) design is addressed in the context of mixed-signal SoC design. In mixed-signal and embedded applications, available integration technologies, pre-existing project development procedures and test demands, as well as available computational resources can play a major role in reducing the total cost impact of any given ADC architecture (CARRO et al., 2003). In fact, future developments in ADCs will require that several design resources, currently available only for designs in the digital domain, be extended to deal with analog data acquisition as well. To better understand how such a goal can be accomplished, one must first review the current status of ADC design in the mixed-signal and embedded system context and its forthcoming design challenges.

1.1 Mixed-signal and Embedded Systems Design Cycle

Several modern day microelectronic applications require a broad range of components with rather different characteristics. Digital processing blocks, high speed communications, analog blocks and RF circuits are just a few examples of functions that are increasingly integrated into the same die as fabrication processes become more advanced. From consumer electronics to embedded applications, market demands for improved and new products at ever increasing innovation rates have shrunk design and manufacture cycles at the same time that systems become more complex.

To deal with this speeded-up reality, several design innovations have been adopted. Today, products heavily rely on previously designed Intellectual Property (IP) or design cores. In the digital domain new tools to provide automatic synthesis, simulation and verification from high level specifications are in widespread use both for the design of individual cores and to total system design. Fast prototyping techniques allow a shorter time-to-market for totally digital designs, while automatic test procedures and new embedded test features (DfT - Design for Testability, and BIST - Built-In Self Test) allow the use of newer integration technologies with higher yields without compromising total design quality.

The picture for analog blocks is however quite diverse. Automatic generation of analog blocks is heavily based on libraries and can not be automatically updated for each new technology. Prototyping techniques for analog blocks, some research proposals notwithstanding, are still far from providing a general and flexible environment like the digital ones. The same also holds true for test and reliability. Thus a lot of craftsmanship is still required to make mixed-signal prototyping a reality in most SoC designs (ZORIAN; MARINISSEN, 2000).

Taking all this factors together we have a picture like the one shown in figure 1.1. On a real mixed-signal design each step in the design methodology includes different procedures for analog and digital blocks. As every aspect of analog design is more costly than the digital counterpart, one should expect that the productivity gains on the digital design block would in the long run increase the amount of system design taken by the analog blocks (KUNDERT et al, 2000; KUNDERT, 2001; GIELEN; RUTENBAR, 2000). As every ADC circuit is partially analog this would be particularly negative for their employment on mixed-signal applications.

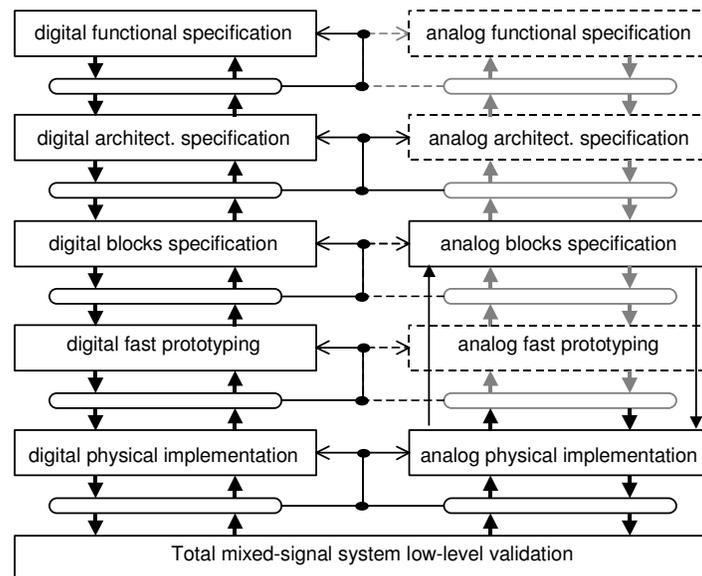


Figure 1.1: An hypothetic mixed-signal design process; according to Kundert (2001), a study performed by Collett International in 1997 with 21 design firms, has shown that analog blocks in mixed-signal designs can consume three to seven times the man-hour amount of digital ones; productivity variations can reach fourteen times.

1.2 The Moore's Law Factor

Analog integration technologies lag behind digital ones because they must be more robust, demand more predictability of their physical and electrical properties and need more geometric features (for instance, one extra layer of poly). The digital design paradigm is at advantage, even with increasingly complex issues to tackle at the deep submicron level.

Computational power is likely to keep pace with the Moore's law for still some time, keeping a steady influx of low-cost digital blocks able to operate at higher switching speeds. At the same time, the higher process variations expected for the technologies to

come will surely impact on the gap between analog and digital technologies, further expanding it. Since analog-to-digital interfacing always relies on some analog components, ADCs will not take full advantage of the latest process, thus being unable to follow an evolution trend compatible with Moore's exponential law.

For economic reasons, many times a System on Chip will have a lot of extra processing power available. Historically this extra computational power has been used to increase system functionalities in many situations (like f.e. smart sensors, control applications or signal processing), replacing or alleviating functions that were traditionally performed in the analog world. Thus, provided that similar conditions are found in the design of ADCs within SoC mixed-signal applications, there is good reason to think it would be better to try the same kind of solution: allocate more digital signal processing resources to allow the use of reduced analog parts, or less demanding ones, compatible with digital process variations and uncertainty.

1.3 Trends at Higher Integration Scales

While exercising in predicting technological future path one is always taking chances. However, a way to keep the pictured scenarios within the bounds of plausibility is to access the so-called industry roadmaps. One of such roadmaps with particular relevance for the subject of ADC design within mixed-signal systems is the ITRS Roadmap (ITRS, 2003). It details the expected evolution trends for the main parameters in integrated circuits, whether they are analog, digital, ADC's, RF or micromechanical, according to industry best informed guesses.

To account for ADC's overall performance evolution trend a single parameter, FoM_{ADC} – Figure of Merit for ADCs – is defined in the scope of ITR'03. FoM_{ADC} follows equation (1.1). Since in ADCs it is always possible to trade resolution for dynamic performance, in this equation the dynamic limits of the ADC (estimated by the minimum between the converter sampling frequency and two times its signal bandwidth) is multiplied by the effective number of quantizing steps (2^{ENOB_0}). Also, the impact of the higher switching speeds in the total power consumption (P) is accounted and enters the equation dividing the figure of merit.

$$FoM_{ADC} = \frac{(2^{ENOB_0}) \times \min(\{f_{sample}\}, \{2 \times ERBW\})}{P} \quad (1.1)$$

According to the ITRS'03, the figure of merit for ADC (FoM_{ADC}) is doubling at every three years, half the digital switching improvement rate. It also points out that major advances in ADC design are required just to keep this rate. Assuming for a while that the FoM can be used as a rough measurement of the amount of system resources available to the designer at any given moment (a not so far-fetched assumption), one ends up with the scenario depicted in figure 1.2.

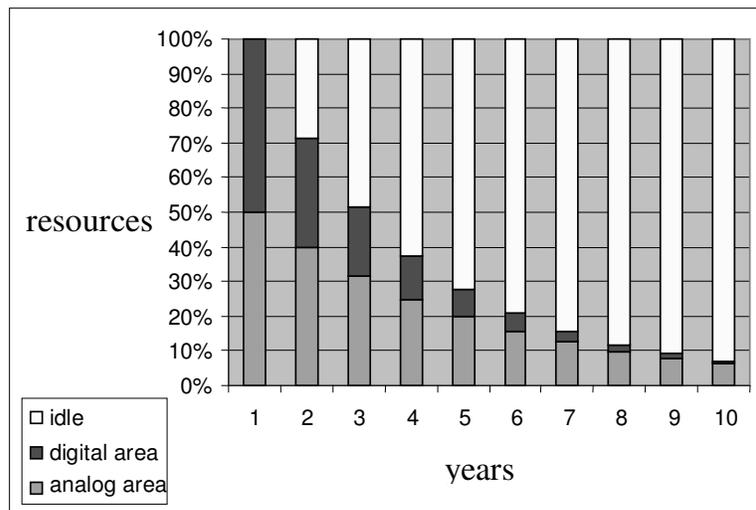


Figure 1.2: Resources ratio in a hypothetical mixed-signal system as a function of time, as predicted by ITRS FoMs.

Starting with an hypothetical application where half the resources were allocate in the digital block, and half in the ADC block, as system integration increases with the arrival of new technologies and system functionality is kept constant, the share of resources taken by the ADC increases. As the trend is kept, one finds that after a decade the ADC alone will respond to 91% of total system resources occupation.

Now, there is one more issue of relevance while addressing the ITRS roadmap: the increase in the yield that is foreseen for new technologies. The performance of ADCs almost always relies, one way or another, on the electrical parameters of the circuit being well-known by the designer. Should mismatches occur, this must be dealt with by component sizing, trimming or calibration (either analog or digital). As analog processing is less favored by the new CMOS processes commonly used by mixed-signal and embedded implementations, and given the restrictions of both sizing, trimming and analog calibration, digital calibration is quite probably to become a mandatory issue for most future embedded ADC applications.

Although all these foreseen trends in integration technology already justify the pursuit for new, highly digital analog acquisition design methodologies, one must also take into consideration other characteristics of current ADC design methods that also impact on the cost and feasibility of mixed-signal and embedded systems. These are issues comprising system specification, design, and reliability

1.4 System Specification and Design Issues

Traditionally, everyone using ADCs tries to reconstruct the analog signal in amplitude and frequency. Using this approach, the resolution of the converter (number of bits) plays a major role. However, for many applications, the digital data the system actually needs is not a full reconstruction of the input signal, but rather a measurement that can express some properties of it. Sometimes, the signal has a low frequency and can be approached by its mean, like in a bridge circuit for instrumentation, for instance.

In many other applications, just the signal statistics are important, applications as analog test and any other circuits that seek to estimate a correlation, signature or grouping from the input signals. For such circuits the information extraction is less demanding in terms of ADC resolution than the total reconstruction of the input.

Another important issue is the growing need of design automation to cope with the growing complexity of the new SoCs. Design automation is much more easily developed in the digital domain (KUNDERT et al, 2000). Some analog blocks for mixed signal integration proposed in the literature have as a strong appealing factor some form of already digital output (LU; LEMKIN; BOSER, 1995; YAMADA et al., 1992; SMITH; HUIJSING, 1989; CHICHOCKI; UNBEHAUEN, 1989; KWON et al., 1999). This is normally done through some kind of clever modification of design that puts the output in an easy to acquire analog form. These are largely *ad hoc* solutions and a general approach to lower analog impact is still lacking.

Then, there is the granularity problem for automatic ADC design: and ADC is a rather complex device, and there are several design choices that must be made in order to determinate the ideal performance of a given architecture. To automate the mixed-signal system design, proposals of automatic architecture selection of ADCs for a given application have already been made (YOO; CHOI; LEE, 2002). Some research settles for delta sigma converters as a largely configurable, general purpose analog acquisition system, and proposes automatic design systems around this architecture (MEDEIRO et al., 1995). However these are top-down approaches, where an already designed ADC structure is selected or parameterized to fit one's purposes. The problem of this approach is that it was already shown that for some applications, even a delta sigma ADC is much larger than the minimum granularity ADC required (NEGREIROS; CARRO; SUSIN, 2002; VUJCIC et al. 1999; TAPANG; SALOMA, 2002).

The third axis of issues comprising the problem of automated analog acquisitions within mixed-signal and embedded systems is the reliability and test axis. One already knows that future ADCs within mixed-signal systems will probably have to endure higher feature variation, work under lower voltage supplies and will take a higher amount of the overall system resources. Under such circumstances, it is even more important that any new design strategy for ADCs addresses the fact that ADC test and ADC fault tolerance will be prominent. Since digital testing is a much more consolidated field of research than analog test, it is also clear that the higher the amount of any ADC that is digital, the easier to test the ADC is. The diagram in figure 1.3 shows the main challenges to deal on future ADCs within mixed-signal systems.

In principle, a much more efficient allocation of the resources on a standard CMOS mixed-signal design would be possible if one could use the smallest possible one-bit converter capable to be implemented on this technology, and then devise a way to improve its performance by digital signal processing techniques and redundancy. A bottom-up design approach based on highly redundant low-cost analog blocks and compensation through DSP modeling could theoretically have several advantages over top-down approaches, on issues such as design automation, application targeting, dealing with CMOS high feature variability, system prototyping, test and fault tolerance of the analog parts.

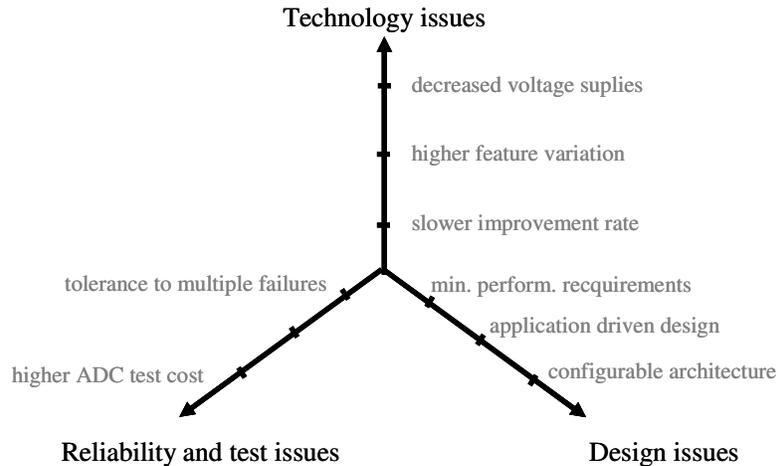


Figure 1.3 : Major challenges for future analog data acquisition within mixed-signal systems.

1.5 Treating Analog Blocks as a Modeling Problem

There is an old quote that goes like: “If someone has a hammer, he will eventually find a nail”. Digital design techniques and digital modeling techniques are quite a powerful hammer, and finding out whether they can be of any use for a given application is many times a worthy pursuit. As computational power becomes available at really low costs, computationally intensive algorithms can be employed to solve problems that traditionally were tackled using special components and materials. To work out a way to transfer analog functions to the digital domain has been a hot topic of research since Moore’s Law reduced the cost of digital chips, and particularly in the last decade (CARRO et al., 2003).

The main approach that allows one to treat an analog problem as a modeling one is based on the concepts of equivalent transfer function and the use of self-calibration properties. The equivalent function is a hypothetical function that fully describes the desired behavior of the designed analog block. Provided that the system possesses a well behaved stimulus generator, it can use the generator in order to determine the real system behavior at a configuration stage, using this knowledge to further compensate the non-idealities. Sometimes the previous knowledge of the signal input statistical properties or of an approximate knowledge of the analog block set-up can further simplify the digital modeling and compensation stage. Figure 1.4 describes the overall proposition.

The present line of research is a conscious attempt to verify whether, and to which extent, it is possible to apply this problem resolution strategy to analog data acquisition in the context of mixed signal and embedded systems. This is proposed as a possible course of research that may be able to fulfill the future challenges that the design of ADCs for mixed-signal systems must face. In the course of this pursuit, many relevant questions are raised, ones that this work hopes to have, at least partially, contributed to answer.

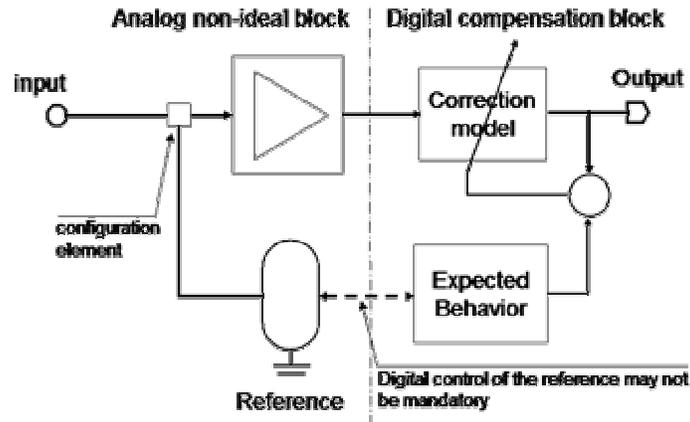


Figure 1.4 : Compensating ADC non-idealities on the digital domain.

1.6 A Handful of Problems

Starting with the above stated goal of turning analog acquisition into a highly digital modeling problem, one must proceed to verify whether this approach addresses the main issues shown in figure 1.3. As stated early, the proposed solution is the use of really small and low cost analog blocks, employing redundancy, self-configuration and digital compensation to fulfill the application specific requirements:

- **Technology issues:** the slower improvement rate of analog technologies is bypassed by defining a mainly digital technology, able to take advantage of the higher switching speeds involved; digital self-calibration together with the possibility to employ highly variable analog blocks is defined as the standard way to overcome the higher feature variations of new technologies. Also, the low cost of the minimum analog blocks will allow massive redundancy and a higher tolerance to soft errors which will take place more often as a consequence of the reduced voltage supplies in the future.
- **Design issues:** provided the analog block is really small, one can build the acquisition system bottom-up, allowing minimum cost for the given set of requirements; this will in its own turn make possible a more application specific analog acquisition design. At the same time, since it does not need demanding analog blocks, the final structure may be easily arranged into a configurable prototyping array, a feature that would make mixed signal prototyping much easier.
- **Reliability issues:** the same features would make analog redundancy much less costly; this together with self-calibration features and digital processing can be combined to provide tolerance to multiple failures and graceful performance degradation, also reducing the foreseen higher ADC test costs.

To make all the above issues possible the first big question to answer is which minimum analog block one should use. Chapter 2 reviews some of the main architectures for ADCs that rely on low cost analog blocks, and explains the chosen one: the digitally compensated statistical sampler. The same chapter also goes on to

explain how the digital modeling strategy can be employed in such architecture. The generation of uncorrelated references for the stochastic acquisition is discussed in chapter 3, while practical applications of these ideas are presented in chapter 4.

The second big issue is whether one can build up onto this idea and which are the limits of performance in the statistical sampling analog acquisition approach. Chapter 5 looks for the answers to this problem, summarizing the research on many strategies that were studied. The aim of this chapter is to provide a set of tools that allow the designer to choose among the many tradeoffs to better fit the analog acquisition block to a given application.

The last and remaining question is how this strategy compares to other currently used solutions for the same set of applications. To answer this question, analog area requirements of the converters thus obtained were compared to other converters in chapter 6.

Chapter 7, gives a draft of the total design process thus defined, summarizes major original contributions of this research, and points to further possibilities in the same line of research.

2 STOCHASTIC QUANTIZATION FOR STATISTICS ACQUISITION

Any ADC design will always use some analog parts. This comes from the fact that no analog signal acquisition can take place without some form of continuous physical variable being compared with a quantization threshold. This is true even for voltage-to-delay and voltage-to-frequency ADCs, only that in such cases the continuous value is quantized using time as the discrete value. To apply the digital modeling approach to analog acquisition one must first review the ADC architectures already proposed in the literature that present minimum analog area overhead and other advantageous properties to be implemented on digital technologies.

These converters were chosen mainly for two reasons: presenting a reduced demand for analog blocks and being representatives of architectures that have played an important role in recent research about automatic ADC design and highly digital ADC design (LOFTI et al., 2003; MEDEIRO et al., 1995). Many ADC architectures in widespread use like successive approximations (PARK et al., 2000) and pipelined conversion (LOFTI et al., 2003) are not fully detailed, since they can be understood as compounded analog structures, and the goal of this research is precisely to minimize the dependence upon analog blocks.

2.1 Highly Digital ADCs Architecture

2.1.1 Flash Converters

The flash converter is many times referred to in the literature as the digital ADC. It is a quite straightforward architecture, where for any required resolution r one employs $(2^r)-1$ comparators with a ladder of analog thresholds. The resulting thermometric output is then digitally converted to a digital scale.

Despite having a very simple structure, flash converters depend on a very high amount of analog area. Smaller flash converters are sometimes combined with dither and averaging to increase their resolutions without the exponential increase in area (AUMALA, 2001; WANNAMAKER, 2003). The analog block is rather simple, but also very demanding. Both comparators and the resistor ladder must have good analog features in order to keep a good analog to digital converting characteristic. To keep the precision on the analog blocks, usually analog calibration or component sizing are required, both being very expensive alternatives.

In a recent paper, Flynn and Bogue (2003) proposed to use low cost analog comparators. The idea was to use redundant low-cost comparators and allow the digital block to select the fittest to the conversion task. In such proposal, however, the resistor

ladder must have a good reliability, since it is also used as the reference for the digital calibration stage. The concept of redundancy of low-cost blocks is rather important, and will be resumed on the discussion about converter performance and parallelism (see chapter 6).

2.1.2 Stochastic Converters

Stochastic quantization is an over sampled process, i.e. a process where the signal sampling frequency is many times higher than the minimum value predicted by Nyquist. On a stochastic ADC, an analog periodic slope signal is compared with the input signal. The outgoing pulse stream is then averaged, resulting in a value that is a good estimate of the input. This approach is already well established for instrumentation applications (VUJICIC et al., 1999; WOLFFENBUTTEL; KURNIAWAN, 1989). In some more recent research the analog reference role is played by a uniformly distributed noise source, which is usually implemented using DA converters (VUJICIC et al., 1999).

The requirement for a particular kind of analog reference (a slope signal or a uniform noise source) is due to the behavior of a comparator when acting as an "area integrator" (WIDROW; KOLLÁR; LIU, 1996) over the probability distributions of functions. As a linear input-output relationship is a mandatory requirement for ADCs, and this kind of analog reference is rather area expensive, the use of stochastic quantization has been very restricted.

More recently, research has been conducted on stochastic quantization using low cost reference sources. For instance, Tapang and Saloma (2002) have shown that a single sinusoidal input, plus low amplitude noise can in theory be used to estimate the main statistical properties of a signal. In a more practical fashion, quantization using a single comparator and a high amplitude non-uniform noise source - an arrangement called Statistical Sampler, has been applied to solve analog acquisition problems where area overhead is a very critical constraint (NEGREIROS; CARRO; SUSIN, 2002).

Being composed by thus a simple comparator and a noise source, the Statistical Sampler is almost the smallest possible block for analog data acquisition. Additionally, its main drawbacks can be treated in the digital domain, what makes it suitable for this research purposes. Given its importance, the statistical sampler is further explained in more detail on section 2.2.

2.1.3 Delta Sigma Converters

Sigma delta converters (TEMES; CANDY, 1990; RITONIEMI; KAREMA; TENHUNEN, 1990) are based on noise reshaping and they oversample the input in order to attain the intended resolution. With a sigma-delta design, resolution and throughput can be traded in a rather straightforward form. These converters also assume the classical additive noise model of quantization as being true, what limits their performance when really high resolutions are required. Solutions to deal with this problem usually involve higher order delta sigma architectures, which are usually more unstable and dependent upon the input signal statistical features. Also, the addition of $\frac{1}{2}$ LSB amplitude noise to the input in order to improve the converter performance is very common design choice.

There is a huge variety of sigma-delta architectures. Despite its many advantages, most of them still take too much analog area, since they always require an analog integrator or a precise multibit DAC in the feedback loop. The flexibility of delta sigma

converters made them the architecture of choice for some recent research aiming at automatic ADC design (MEDEIRO et al., 1995).

A recent paper by JACOMET et al. (2004) uses a simple lossy passive integrator (a RC circuit in fact) in an almost totally digital sigma-delta modulator, whose output bitstream is subsequently sampled by the digital block. The total circuit cost is rather low, however the input is assumed to be a current signal and the circuit works fine for low resolutions. In any applications with a voltage signal a current to voltage circuit must be employed in the input.

The main problem with this circuit is scaling up to higher resolutions. According to the article the loss in the integrator is asymptotically related with the maximum resolution. The paper shows an implementation with four bits, judging by the presented charts, any application around and over eight bits would be very difficult to reach. Also there is no clear path to improve the circuit resolution while keeping at the same time the simplicity in the analog block.

2.1.4 Time-delay Converters

A traditional approach to analog-to-digital conversion is to pass the signal to be digitized through an analog circuit that converts the signal in some form of time-interval representation, which can be easily acquired by the digital block (LU; LEMKIN; BOSER, 1995; YAMADA et al., 1992; SMITH; HUIJSING, 1991). This is the case for double slope-converters (KWON et al. 1999), duty modulation (CICHOCKI; UNBEHAUEN, 1989; BERMAK, 2002), frequency modulation (WATANABE; MIZUNO; MAKINO, 2001; BERMAK, 2002) and, in a broader sense, also for some integrate-and-fire circuits (SARPESHKAR; HERRERA; YOUNG, 2000). All these devices share the same drawback: the need for a robust analog block that can work at high speeds (in FM-based techniques this problem is even harder to solve).

In a recent paper, Watanabe, Mizuno and Makino (2001) proposed a "completely digital" circuit (the delay line converter - DL-ADC) that uses a row of non-linear delay elements in a voltage to frequency modulation setup. The analog block is limited to a line of buffer elements connected in a ring. The input signal is then applied directly to the power source of the buffers. As the difference in the polarization voltage affects the total transition time in each buffer, variations in the ring delay are related to the input voltage. The main limitations of this design are a strong non-linearity and a small dynamic range. Inside the operation range, resolution is not uniform due to the delay element characteristic. To minimize the problem, the authors proposed a further constraint in the dynamic range, although digital linearization could have improved their results. Also, no solution is presented to the problem of temperature drift, which remains to be dealt with in further developments.

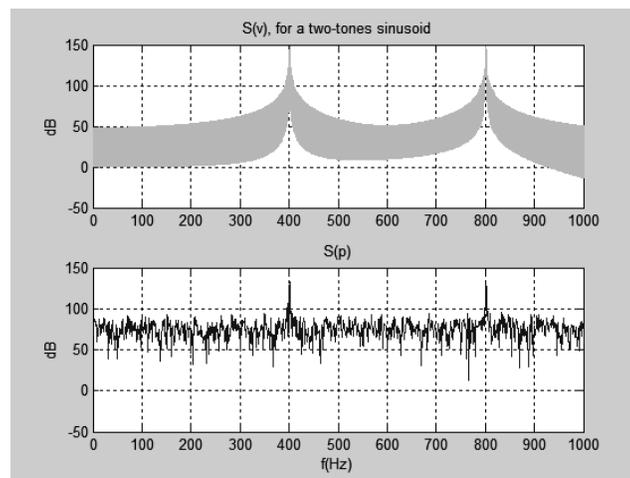
As this approach seemed rather promising, an implementation of the DL-ADC and detailed comparison of its performance to the statistical sampler acquisition was performed (MAINARDI; SOUZA JR.; CARRO, 2004). An important result that was not stressed in the original paper of the DL-ADC is that an analog buffer for the input signal is a mandatory requirement of the architecture. This extra analog area, together with the open issues concerning reliability and temperature drift were considered in the analysis that favored the Statistical Sampler as the best choice to be used as a basic build block for a largely digital ADC.

2.2 Statistical Sampler Operation

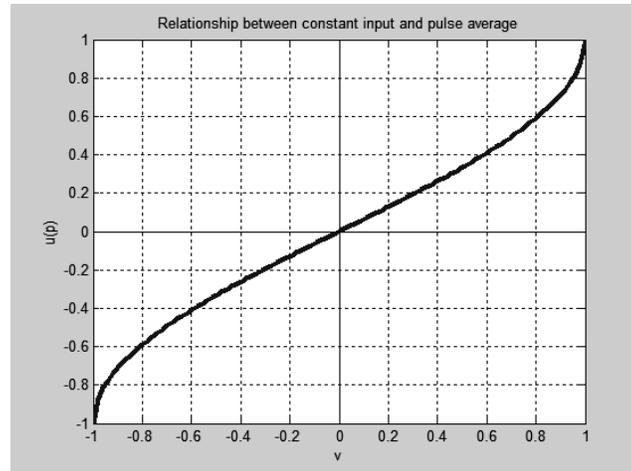
From the previous section it was seen that one of the smallest possible analog to digital acquisition system is composed of a single comparator and a random *dither* centered in zero, used as reference. After analyzing each of the possible low-cost ADC architectures, the statistical sampler was chosen as the most promising analog block to employ in an analog acquisition architecture compensated digitally. In the remaining sections of this chapter the principles of operation of stochastic quantization and its main features are presented, some implementation issues concerning the reference generation are raised and a first digital compensation technique is introduced.

2.2.1 Hard-limited Sum of Signal and Noise

Given a single stochastic quantizer composed by a comparator acting upon an input analog signal v and a band-limited analog reference signal (γ), the output will be a pulse-stream p . Stochastic quantization assumes that the properties of the reference γ are such as one can determinate properties of the input v from measurements performed over the pulse-stream p . Figure 2.1a, shows the frequency analysis performed in the output of a two-tone signal after passing through the statistical sampler: the spectrum of the signal p reflects the spectrum obtained for the input v , in the case γ is a multilevel white noise. The plot in figure 2.1b shows the relationship between a constant value applied to v , and the average of the resulting pulse stream $\mu(p)$, in this case γ is a high-frequency sinusoidal signal.



(a)



(b)

Figure 2.1 : Relationship between properties of v and p for different situations, read text to further explanations. (a) Spectra. (b) Constant values of v and corresponding $\mu(p)$.

To understand how this mapping between v and p properties happens, and hopefully benefit from it, one must keep in mind that when two time-varying signals are compared, the resulting bit-stream is the hard-limited subtraction of the inputs. Figure 2.2 shows the statistical sampler and its equivalent model. The outcome of the hypothetical subtraction is called s , thus the result one gets after passing it through a hard-limiter is the pulse-stream p .

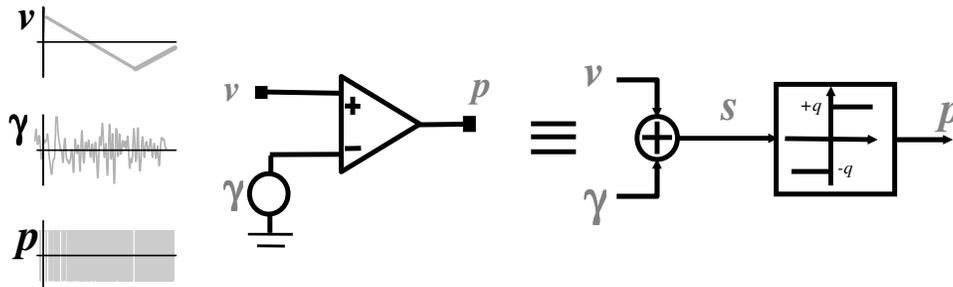


Figure 2.2 : Stochastic quantization as the hard-limited sum of analog signals.

Usually two kinds of references may be employed: γ may be a periodic signal or multilevel noise. In both situations the reference role is to shift the comparison level sweeping the whole dynamic range of v . For this reason, the first property of stochastic quantizer is that the total dynamic range of the converter, $DR(v_{MAX})$, is limited by the dynamic range of the reference ($DR(v_{MAX}) \leq DR(\gamma)$).

Depending on the application one may be interested in getting a high resolution view of v or, assuming v is a periodic signal, one may just want to take a snapshot of some of its relevant spectral features. In the first case one can use a reference much faster than the input; in such situation v may be considered quasi-static and $\mu(p)$ will be used to approximate its value. The second case imposes looser constraints over γ and v , but also presents results which are limited to specific pattern-matching related applications.

While the low-pass quasi-static case is discussed in this section at length, the second case is approached in this work in a more application specific basis: section 2.3 introduces the main ideas and points to the chapters and sections that summarize this discussion. In the remaining parts of this chapter the statistical sampler with pulse-stream averaging is analyzed for resolution, linearity and conversion time.

2.2.2 Quasi-static Acquisition

In the quasi-static situation one is concerned with the measurement of an input that is much slower than the total bandwidth of the reference. Under this condition one can consider v as a constant value and use the average of the pulse-stream $\mu(p)$ to estimate it. In fact, as the averaging will actually take place in the digital domain, one will use an

estimator m ($m = \frac{1}{N} \sum_{n=1}^N p[n] \approx \mu(p(t))$) with averaging depth N , operating over discrete one-bit samples of p ($p[n]$).

Quantization analysis is performed over the PDFs (Probability Distribution Functions) of both signals. When one calculates s by subtracting γ from v , the PDF of $-\gamma$ is actually convolved with the PDF of v . As v may be considered as a constant signal, its PDF will be a Dirac delta centered in this value, and convolving this function with $P(-\gamma)$ one will simply center the distribution $P(-\gamma)$ around v .

Passing s through the hard-limiter would produce a PDF (figure 2.3) with two deltas proportional to areas under the plot $P(s)$ for $s < 0$ and for $s > 0$, A1 and A2 in the figure 2.3. Knowing the probability distribution of p , it is, thus, possible to determine the pulse-stream average $\mu(p)$ as a function of the input v (2.1). For a uniform noise, expression (2.1) can be evaluated, normalized to the interval $[-1, 1]$ and shown to be linear (2.2); in this equation, m_N is m normalized to the interval $[-1, 1]$.

$$\mu(p) = \frac{-q_- \cdot \int_{-\infty}^0 P(s) + q_+ \cdot \int_0^{+\infty} P(s)}{\int_{-\infty}^{+\infty} P(s)} \quad (2.1)$$

$$m \approx \mu(p) = q \cdot \frac{2 \cdot v + 1}{2} \rightarrow m_N \approx \frac{DR(v)}{DR(\gamma)} \cdot v \quad (2.2)$$

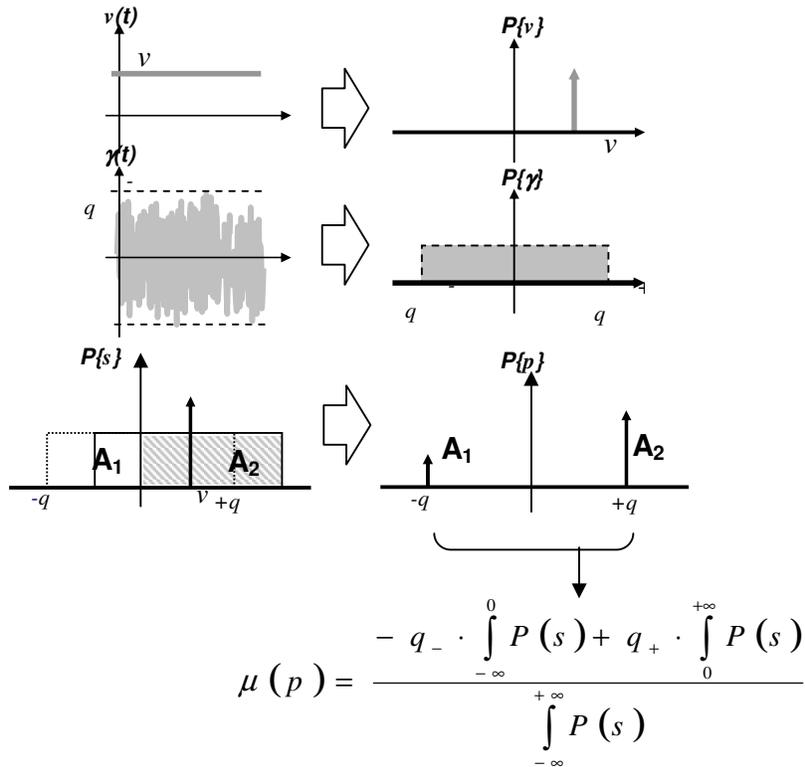


Figure 2.3 : Calculating the relationship between the N-cycles average m of the pulse-stream p and the input value v . Since m is an estimator of $\mu(p)$ one can use it to infer the value of v .

The entire process of derivating expression 2.2 from expression 2.1 is depicted in figure 2.3. The probability of high level in the comparator output will be proportional to the area A_2 under $P\{s\}$. As v increases a greater fraction of the total reference is shifted to the positive side of the $P\{s\}$ plot accordingly. In fact, one sees that

$$q \cdot \int_0^{\infty} P(s) = q \cdot \int_0^{v+1} ds = q \cdot (v+1). \text{ Thus, calculating the probability of a low level in the}$$

omparator and combining the results one ends up with the first part of expression 2.2. Since the resulting m is presented in a positive range ($m \in [0, 1]$), and the input v varies along a symmetric range ($v \in [-\text{DR}(v)/2, +\text{DR}(v)/2]$), and $q = \text{DR}(\gamma)/2$, one can normalize m to get m_N , that will mach the input values. In equation 2.2, $\text{DR}(v)$ is the dynamic range of the input signal and $\text{DR}(\gamma)$, the range of the reference.

Using a reference with any other PDF shape will imply in a non-linear, but well-defined, mapping between $\mu(p)$ and v . Even when this relation is not uniform, the knowledge of its properties may also allow the use of a less costly reference generator block if the pulse averaging stage is followed by a digital linearization process. This issue is further discussed while dealing with the linearity of the statistical sampler.

2.2.3 Convergence to the Expected Resolution

Naturally the average estimator m is itself a stochastic variable related to the averaging depth (N). As N increases $m \rightarrow \mu(p)$, with an uncertainty that can be

estimated. The final uncertainty will be defined for many factors, including the distribution of the reference ($P(\gamma)$). However, one may rely on the Central Limit Theorem [PAP91] to assume that for a high value of N the distribution of m will be normal and centered in $\mu(p)$. Also, as the value of m will be scattered around $\mu(p)$ with this normal distribution, there will be an error $e = \|\mu(p) - m\|$ or uncertainty for each averaged value. Resolution will be determined by the maximum uncertainty allowed for the output.

This approach gives for stochastic quantization a resolution that can be approximated by $r = \frac{1}{2} \cdot \log_2 \left(\frac{N}{k_u} \right)$, where $k_u > 1$ is a constant defined by the shape and relative amplitude of the reference γ . In other words, this means that one can assume the quantization step of a statistical sampler as a number proportional to $\frac{1}{\sqrt{N}}$.

Figure 2.4 shows the idea: for a fixed value of v , m_1 is calculated as a moving average with depth $N_1 = 100$ and m_2 with average depth $N_2 = 1.000$. At the right side of the picture one can see that fitting the measured error distributions one has Gaussian plots matching the expected.

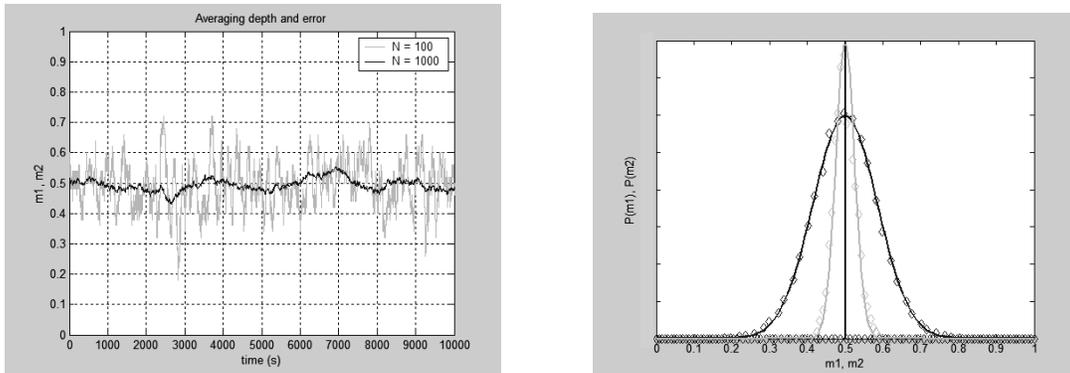


Figure 2.4 : As the number of averages N increases, error scattering is restricted, allowing an approximation of the input value with a higher resolution.

One alternate way to understand the relationship between resolution and the uncertainty of the average estimation is as follows: since the error in stochastic quantization is nearly ideal and has an almost flat spectral characteristic, m will converge to $\mu(p)$ by reducing the total error spectral power.

2.2.4 Statistical Sampler and Linearity

Until now it was possible to show how one can calculate the relationship between the input v and the estimated average of the pulse stream m for a statistical sampler in a quasi-static situation. It was also shown that a uniform reference guarantees a linear relationship for the sampler, and that using this average to approximate the input v one has a resolution that is proportional to $\frac{1}{\sqrt{N}}$.

However, a uniform noise distribution is not as easy to design as many others (for instance a Gaussian distribution) and may not be practical. If the reference distribution

$P(\gamma)$ is well-known, the same procedure that was employed to a uniform reference can now be applied for any other non-uniform PDF.

If, for instance, $P(\gamma)$ is Gaussian, one ends up with the relationship described on equation (2.3), where erf is the error function of the normal distribution (2.3).

$$erf(v) = \frac{1}{\sqrt{2\pi}} \cdot \int_{-\infty}^v \exp\left(-\frac{t^2}{2}\right) \cdot dt \quad (2.3)$$

In the remaining of this document, this function that maps the input value to the average of the pulse stream will be identified as the Greek capital letter Φ . Thus, for the above mentioned case with a Gaussian reference equation (2.4) holds.

$$\Phi(v) = \frac{DR(v)}{DR(\gamma)} \cdot erf(v) \quad (2.4)$$

When using references with non-uniform PDFs, and whenever a linear characteristic is required for the stochastic converter, one will have to resort to a digital linearization block (which behavior is described by the function Γ) following the averaging. It is important to note that the ideal characteristic for this linearization block will be the inverse function of Φ (i.e. $\Gamma(v) \equiv \Phi(v)^{-1}$). Figure 2.5 illustrates the linearization block and its desired characteristic for the statistical sampler with a Gaussian reference.

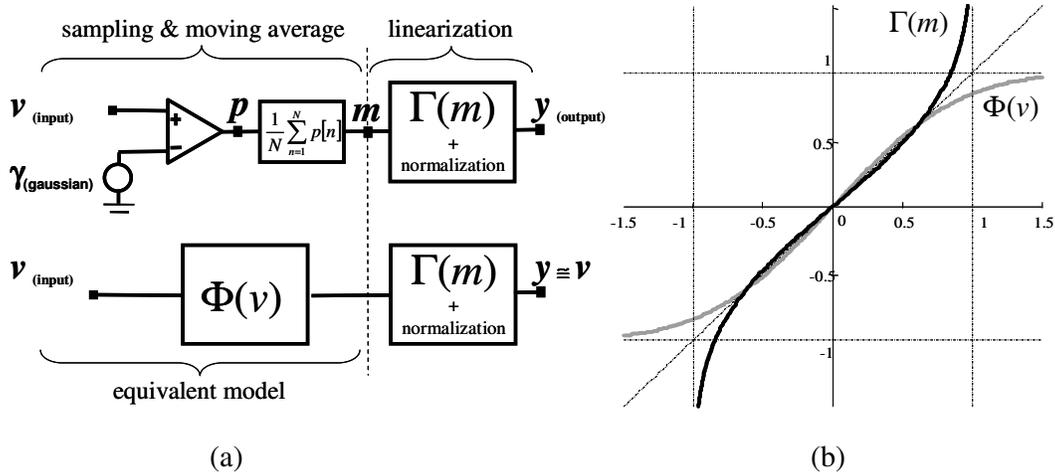


Figure 2.5 : Linearization through non-linear mapping of the output. (a) One compensates the non-ideal behavior of the acquisition in the digital domain after averaging. (b) Given the Φ (gray), the ideal linearization function Γ is defined (black).

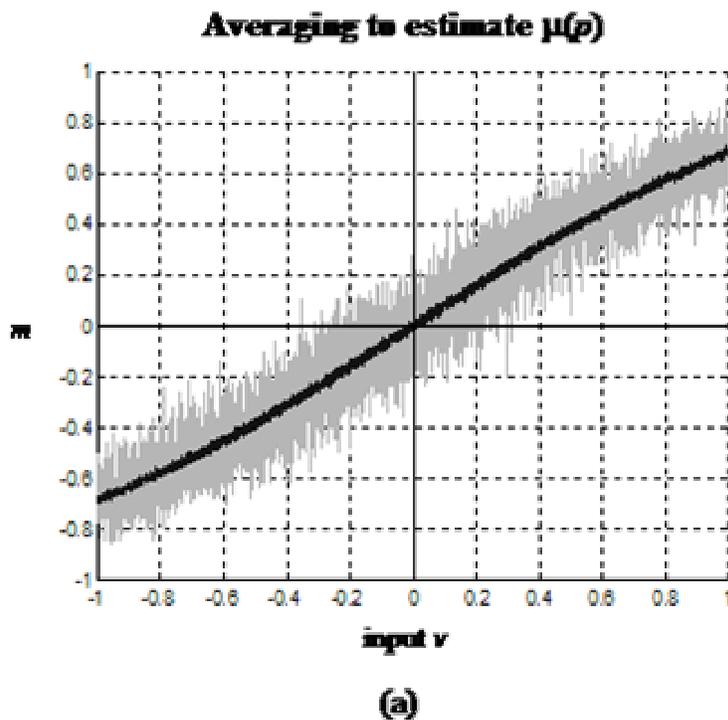
2.2.5 Non-linear Mapping, Convergence and Linearity

For non uniform reference distributions, Γ is a non linear mapping, and this may impact on the convergence for the desired resolution. Keeping the same example of a reference with Gaussian distribution, one has an ideal linearization function Γ that is asymptotic near ± 1 (figure 2.5b). This means that any input that is too close to the

dynamic range fringes will have its uncertainty amplified by the difference in the gain represented by the non-linearity of the linearization function Γ .

A higher gain in the periphery of the DR (Dynamic Range) also means that one needs more estimates (N) to guarantee the same dispersion of the output. The reason for that behavior in the case of the Gaussian reference is simple: any input at the margins of the distribution will be “reached” by γ fewer times than if it was located in the center of the distribution. That implies that fewer transitions in the pulse-stream output are available to be averaged over, and, as a consequence, convergence to the expected resolution will take more averaging cycles. As the number of averages N is fixed for the whole dynamic range, resolution at the fringes turns out to be lower.

Figure 2.6 shows the output of the statistical sampler with Gaussian reference before and after linearization.



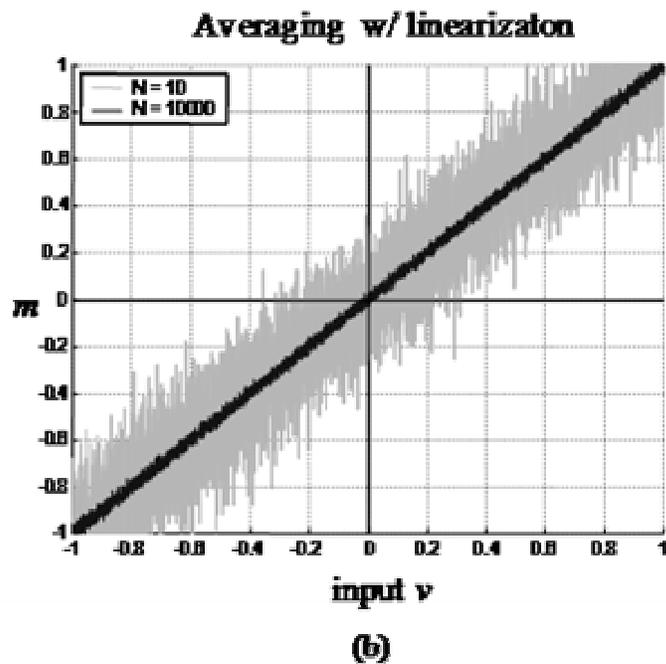


Figure 2.6 : Resolution over the dynamic range for a Gaussian reference, plot shows averaging output m and linearized output y . Averaging depth $N = 10$ and $N = 10.000$ cycles.

Contrary to other ADCs, such as the flash converter architecture, the statistical sampler does not have a discrete evolution in the number of bits. Resolution is a continuous function of N and $P(\gamma)$. As the error will be normally distributed, one should define a maximum number of error standard deviations admitted to estimate the total system resolution. This number will define the size of the quantization step (usually symbolized by q in the literature).

Of course, this arbitrary choice of how many error deviations correspond to q presents its own tradeoff: if the number of deviations concealed in q is not high enough many acquired samples will have a lower resolution than expected. On the other side, if q is much higher than the error standard deviation, the statistical sampler may take too much time for a single conversion in an application where a few samples with lower precision would not be a problem.

In figure 2.7 it is possible to see the number of averages (N) required for a given resolution using different numbers of error standard deviations. The central line in both plots corresponds to $q = 2 \times \sigma_e$, where σ_e is the standard deviation in the error distribution. Whenever it is not specified otherwise every resolution plot in this work assumes this condition.

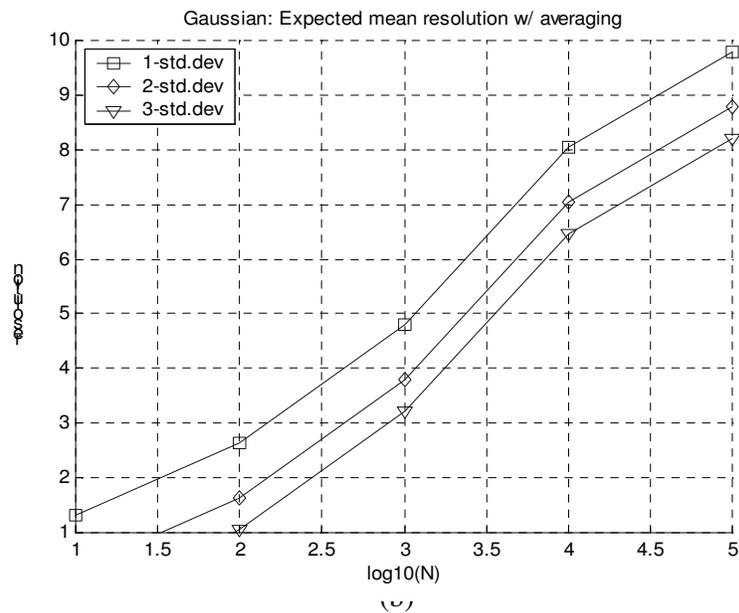
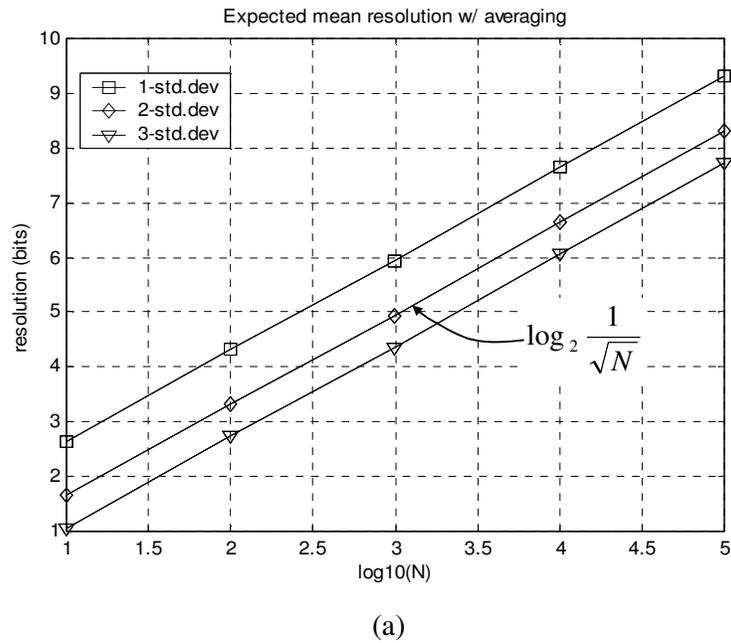


Figure 2.7 : Averaging/resolution relationship: (a) for uniform noise; (b) for Gaussian noise.

2.3 Number of Bits and PSD

All the analysis performed until now was limited to the quasi-static situation, where the reference maximum frequency is many times the maximum frequency of the signal. In this case a low-pass averaging process is employed to estimate $\mu(p)$. An alternative approach to statistical sampling is to perform data acquisition directly in the frequency

domain: instead of averaging, the Power Spectral Density (PSD) of p is directly estimated and any higher level application operates over it.

Working directly over the pulse stream may be useful when one is concerned with a very narrow band signal operating on well defined frequencies, or when the application seeks only to determinate a spectral signature of the signal. The estimation of the PSD already involves averaging of the Fourier transform, similarly many other algorithms have built-in features that already reduce the spectral noise power. For such cases, the Effective Number of Bits (ENOB) is directly calculated over the PSD, using the relationships among ENOB, THD (Total Harmonic Distortion), SNR (Signal to Noise Ratio) and SINAD (Signal to Noise and Distortion Ratio).

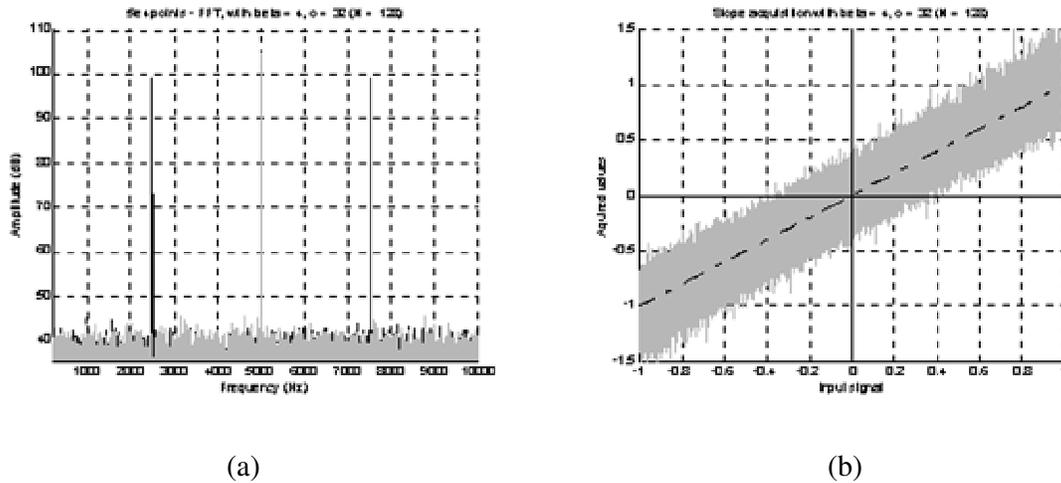


Figure 2.8 : Statistical sampler with $N = 128$: (a) a two-tone statistical sampler acquisition using the PSD of the pulse-stream ($S(p)$) using a 105 points – FFT. (b) Slope acquisition with the same sampler and the same number of comparators and averages

Figure 2.8 shows the main idea: the same statistical sampler using a uniform reference and with a low averaging depth is employed: (a) to acquire a two-tone signal; (b) to read an input slope. From the slope acquisition one can see how the system is still highly noisy, thus providing a reconstructed resolution very low ($r_{aq} \approx 2$ bits) and does not represent a very high constraint on the stochastic quantization process. However, if one is concerned only with the relationship between the peaks in the spectrum, this data can be directly processed to obtain a FFT with a much higher resolution (≈ 8 bits) with just a cost in latency. This way, the stochastic acquisition allows us to use the knowledge of the system application to minimize the analog cost of the acquisition blocks. Also, if a full reconstruction of the signal (instead of a FFT) was necessary using the same circuit to reach 8 bits, it would take about 100.000 averages in the statistical sampler with a single comparator to keep discretization noise within three standard deviations.

3 RANDOM SIGNAL GENERATORS

The former chapter has made it clear that analog values can be acquired using a single comparator and a reference multilevel noise. It was also shown that the addition of high levels of noise to this system allows small one-bit ADCs followed by digital averaging to achieve higher resolutions. Although most electrical systems already have an amount of noise that can help the statistical sampler, the usual signal dynamic range will need noise references with rather higher amplitudes.

In this chapter, while studying how to improve the SS-ADC performance with parallelism, it will be shown that sometimes several uncorrelated noise sources are necessary. While obtaining a single noise source may be easy, the noise generation circuits may prove expensive if one is employed for each of the required references. This section is thus devoted to study how to design several uncorrelated analog random signal generators on chip using minimum noise generator cost, and how the different architectures may be suited to use in a statistical sampling acquisition environment.

3.1 True Random Signal Generator

One of the advantages of the statistical sampling approach to analog acquisition is the low cost involved in designing a simple noise source. One of the most usual ways to do it is using a component with a high thermal noise characteristic (usually a Zener diode, but sometimes a resistor with a high value) and further amplifying it. Figure 3.1 shows the basic topology (HOLMAN; CONNELLY; DOWLATABADI, 1997).

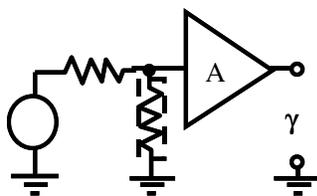


Figure 3.1 : Thermal noise based, true random signal generator.

These circuits generally provide an almost Gaussian irregular output distribution that must be previously completely characterized so that one can define the output linearization strategy. Also, one can use a really high amplification in order to fit just an almost uniform slice of the distribution over the entire input dynamic range.

The main disadvantage of true random signal generators is the requirement of special analog components of difficult implementation on standard digital CMOS technologies. As for a parallel acquisition where several uncorrelated noise sources are

required, when using this kind of generator one of the techniques described in section 3.3 should be used.

3.2 Chaotic Circuit

Another analog approach to generate the random references is to use a circuit with a chaotic dynamic that can be parameterized to exhibit the desired noise characteristic. One such circuit that can provide analog noise with both almost uniform and almost Gaussian (depending upon circuit parameters) distributions is the Chua circuit depicted in figure 3.2 (ANDÓ; GRAZIANI, 2000).

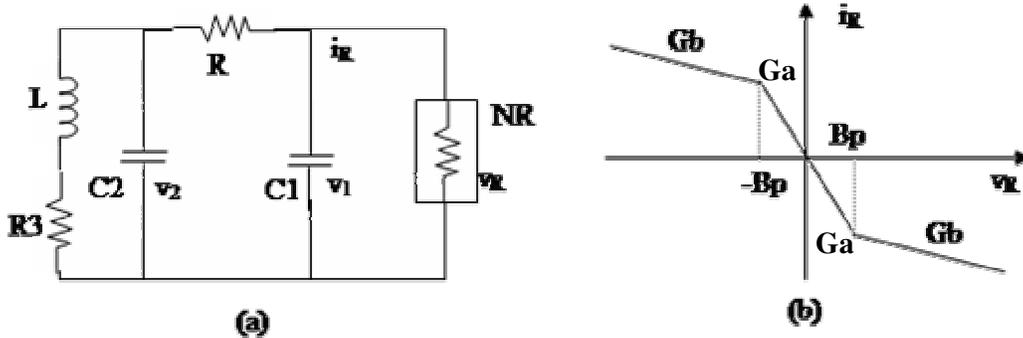


Figure 3.2 : True random signal generator using the chaotic Chua circuit.

The circuit is composed by five linear elements (resistors, capacitors and one inductor) and a single non-linear resistive element represented by NR , which follows the input-output characteristic given in 3.2b. The circuit parameters are given by the set of equations (3.1).

$$a_0 \equiv \frac{C_2}{C_1} \quad b_0 \equiv \frac{R^2 C_2}{L} \quad k \equiv \frac{1}{RC_2} \quad m_0 \equiv RG_a + 1 \quad m_1 \equiv RG_b + 1 \quad (3.1)$$

By changing the values of a_0 , b_0 , k , m_0 and m_1 , rather different dynamic behavior are exhibited by the voltages measured over the capacitors C_1 and C_2 . According to Andó and Graziani (2000), the set of parameters $a_0 = 9.6$; $b_0 = 15.2$; $k = 1$, $m_0 = -0.1428571$, $m_1 = 0.2857142$ makes the circuit a Gaussian noise generator, while for the parameters $a_0 = 9$; $b_0 = 14.2$; $k = 1$, $m_0 = -0.1428571$, $m_1 = 0.2857142$ its PDF is almost uniform. In both cases the distributions match the desired ones 95% of the time.

Although the Chua circuit offers a rather nice possibility of generating noise with almost uniform distributions, it repeats the same flaws of the thermal noise circuits, with one additional problem: the high sensitivity of the circuit parameters makes its correct design and operation a rather difficult task.

3.3 Providing Several Uncorrelated Noise Sources

Since a true uncorrelated noise source is characterized by the temporal independence of its successive samplings, several uncorrelated noise sources can be provided by multiplexing a single noise source in time. To accomplish this one can use a sample-and-hold delay chain where each analog memory element could be treated as a separate random source.

To improve the results one can use a digital pseudorandom number generator to scramble the sampling intervals in the sample-and-hold elements. In this technique a number of sample-and-hold elements β is allowed to sample the original signal at a given instant (out of L possible sampling intervals), determined by the pseudo-random variable (i , see figures 3.3 and 3.4).

The technique works as follows: inside a time interval T , a number of time slots L numbered $[1, L]$ is defined. For each of the demanded generator outputs, a pseudo-random number i (also in the interval $[1, L]$) is generated in the digital block at each time interval T . Then every sample and hold circuit uses its own value for i in order to define the number of the time slot where it will be triggered. It is important to note that the pseudo-random number sequences are digitally generated and must be uncorrelated to guarantee the independence of the values of γ_n .

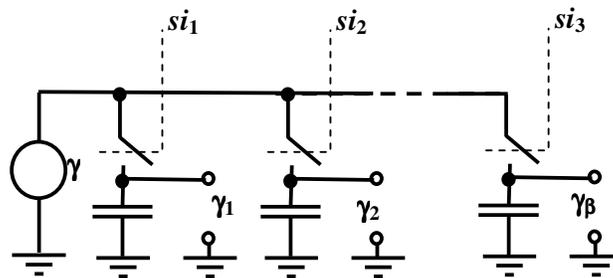


Figure 3.3 : Pseudorandom scrambling to generate several noise sources. Signals $s_{i_1}, s_{i_2}, \dots, s_{i_\beta}$ are pulses that are high when the time slot counter reaches the values i_1, i_2, \dots, i_β respectively.

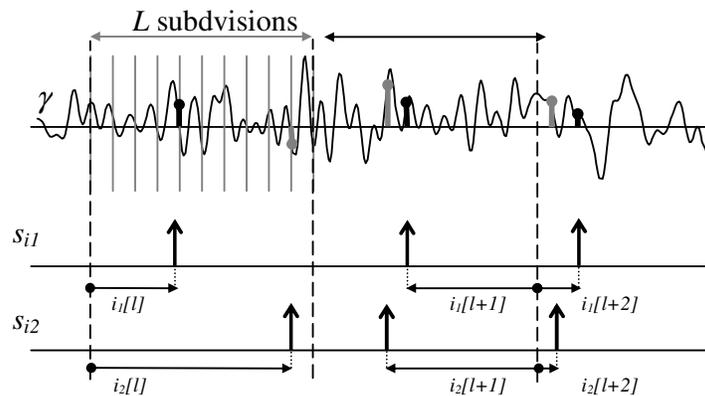


Figure 3.4 : Splitting a single true random noise generator into a series of uncorrelated multilevel sequences.

3.4 Pseudorandom Circuit with Sampling

A low cost way to implement multilevel noise generator (in fact pseudo-random generators) is using the same sample and hold structure explained in section 3.3 and substituting the original noise generator γ for a simple analog periodic signal a_{ref} . This analog signal must be adjusted such as its period is an integer multiple of the period T (in figure 3.5 the periodic signal is a charge discharge waveform), since a_{ref} will be sampled at random intervals (i) within its period T . Thus, in such architecture the problem of producing β multilevel analog references γ_n is reduced to the digital

generation of β uncorrelated sampling sequences ($i_1 \dots \beta$). This same structure was proposed in previous papers (FLORES et al, 2002) and one integrated circuit with this generator was already designed envisioning analog test applications (FLORES et al., 2003).

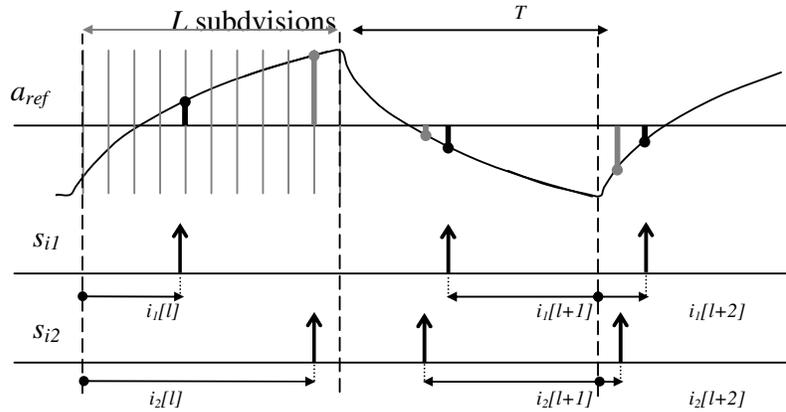


Figure 3.5 : Sampling a periodic signal to generate multilevel pseudo-random noise.

Some caution is advised when employing the pseudo-random generator. Randomizing the sampling time is important in order to produce a good output spectrum. If L , the number of time slots within a single period is too low, output PDF will be severely quantized. Also, if one uses the rise and fall transitions of a_{ref} the output noise spectrum may present a high component at the frequency $f = \frac{1}{2T}$. To prevent this last problem, rise and fall time intervals must use symmetrical indexing schemes (see figure 3.5).

Provided that the behavior of a_{ref} in time is approximately known, one can calculate the output PDF of the generated signals γ_n . In fact, if the random sampling signals (i_n) have a uniform probability distribution, in the long run each time slot will be selected the same number of times. For a slope analog signal a_{ref} , this setup generates a uniform output distribution (P_U in figure 3.6). However, figure 3.6 shows that if the reference is not linear (in the example it is the low-to-high transition of a charge-discharge plot) the output

It is possible to show that, to calculate the output PDF one must evaluate for each monotonic section of the signal a_{ref} the derivative of its inverse function. Afterwards, the expressions obtained will be weighted by the ratio of the time this section takes related to the signal period. Determinate this distribution will be important when one seeks to estimate the equivalent model ($\Phi(v)$) of the statistical sampler to define the linearization model ($\Gamma(m)$). In the next section, the issue of how to calculate the PDF of a given periodic function is explained at length, while in the following chapter throughout the applications, this technique is applied to estimate the ideal linearization function for statistical sampler based ADC (SS-ADCs) with different shapes of reference reference generated (in the figure P γ) will also not be evenly distributed.

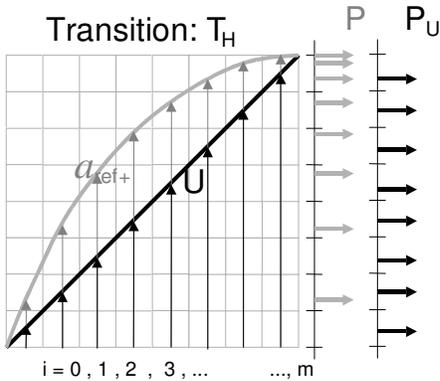


Figure 3.6 : Within the analog signal period, any sampling slot can be selected, if each interval has the same probability to be selected (given a uniform distribution for the random sequence i) the resulting output distribution will be determined by the analog PDF of the reference.

3.5 PDF of a Periodic Signal

When discussing the above mentioned generator behavior, it is important to understand the consequences of the analog reference a_{ref} shape in the final distribution $P(\gamma)$. If the pseudorandom number distribution $P(i)$ is uniform, the distribution of the generator output will follow the distribution of the analog reference ($P(\gamma) \rightarrow P(a_{ref})$). The question then, becomes how to calculate $P(a_{ref})$, for any given periodic reference employed.

Given any periodic signal s discretized in both time and amplitude, its probability distribution function, $P(s)$, is proportional to the number of times (let's call it h) the signal is found within a given interval of values Δy , assuming one samples this signal in Δx intervals (figure 3.7)

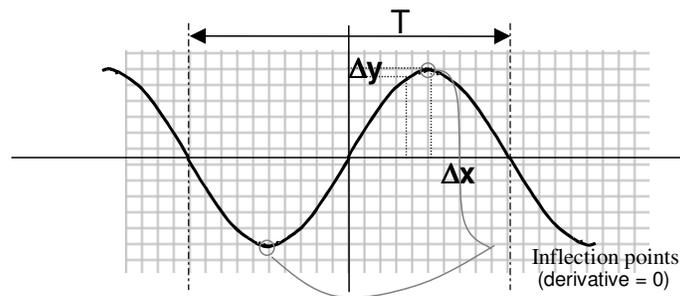


Figure 3.7 : Estimating the PDF for a periodic signal.

For any monotonic periodic analog signal with a frequency F , this will happen F times in any unitary period of time. In fact, the number h for every interval Δx will be given by the ratio between Δx and Δy ($\Delta x/\Delta y$). Generalizing for the time continuous situation where both deltas go to zero one has expression (3.2)

$$p(y) = f \cdot \left| \frac{dx}{dy} \right| = f \cdot \left| \frac{d(y^{-1})}{dy} \right| \quad (3.2)$$

This expression, however, can only be applied to monotonic and invertible functions. As any useful periodic signal is not monotonic, it is necessary to expand this result for an arbitrary waveform. This can be accomplished by decomposing the original signal in several monotonic intervals (by splitting the period in the signal inflection points, where its derivative is zero). As the total number of times any Δy will be visited is the sum of the partial results for each interval λ_n (figure 3.8) the final PDF can be calculated weighting each result by the ratio between the time each interval takes (λ_n) and the total period T (equation 3.3).

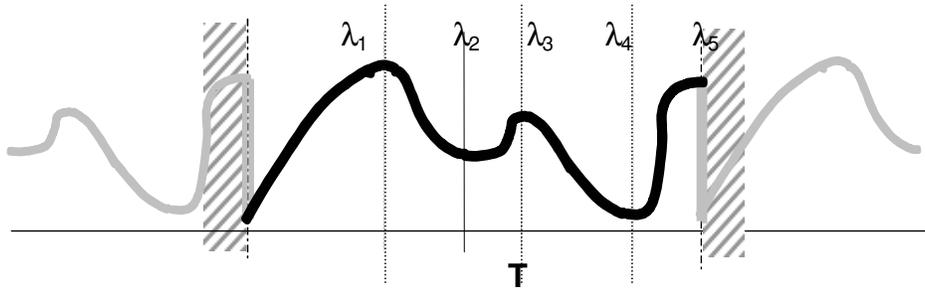


Figure 3.8 : Periodic signal with highly irregular shaped period.

$$p(y) = f \cdot \left[\frac{\lambda_1}{T} \cdot \left| \frac{dy_1^{-1}}{dy} \right| + \frac{\lambda_2}{T} \cdot \left| \frac{dy_2^{-1}}{dy} \right| + \frac{\lambda_3}{T} \cdot \left| \frac{dy_3^{-1}}{dy} \right| + \frac{\lambda_4}{T} \cdot \left| \frac{dy_4^{-1}}{dy} \right| + \frac{\lambda_5}{T} \cdot \left| \frac{dy_5^{-1}}{dy} \right| \right] \quad (3.3)$$

3.5.1 An Example: Calculating the PDF of a Sinusoidal Signal

To show how equation (3.3) is employed its application for a simple sinusoidal signal described by equation $y = \sin(2\pi \cdot f)$, within a unitary period $[0, 2\pi]$, is shown in the sequence. One can see that there will be two inflection points (at $\pi/2$ and $3\pi/2$). This gives equation (3.4).

$$P(y) = \left(\frac{1}{4} \cdot \left| \frac{-1}{\frac{\partial y}{\partial x}} \right|_{[0 \dots \pi/2]} + \frac{1}{2} \cdot \left| \frac{-1}{\frac{\partial y}{\partial x}} \right|_{[\pi/2 \dots 3\pi/2]} + \frac{1}{4} \cdot \left| \frac{-1}{\frac{\partial y}{\partial x}} \right|_{[3\pi/2 \dots 2\pi]} \right) \quad (3.4)$$

Calculating the derivative of $y = \sin(2\pi \cdot f)$, using the theorem of the derivative of the inverse function, and substituting $\cos(2\pi \cdot f)$ by $\sqrt{1 - \sin(2\pi \cdot f)^2}$, one gets the well-

$$P(y) = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{1 - y^2}} .$$

known result

4 PRACTICAL APPLICATIONS

To acquire experience with the *SS-ADC* and better define its application range as an analog to digital converter, some practical implementations were made. First, differential data acquisition was performed on a bridge circuit using Gaussian noise. After this, the same approach was used to perform linearization in a statistical sampler using the above proposed pseudo-random multilevel noise generator. Finally, in the third application, a different idea was implemented, in this case the digital control circuit for the pseudo-random generator was modified in order to achieve a more uniform noise distribution and, as a consequence, to define a linear acquisition plot.

4.1 Bridge Circuit with Differential Acquisition

Bridge circuits are applied in instrumentation and measurement whenever one has to determine a resistance or impedance absolute or variation values. Such topologies are used both in balanced mode, where a known impedance variation is used to estimate the impedance of an unknown element, and in an unbalanced configuration, where the element variation can be estimated by the voltage output of the bridge.

Figure 4.1 shows a typical resistive bridge with a single variable element working on unbalanced mode. A reference $v_{REF}(t)$ is applied, the sensor input to be estimated is given by $r(t)$, where $r(t) = \Delta R(t)/2R$. The bridge output is calculated by the average of the pulse streams (p_1, p_2) difference.

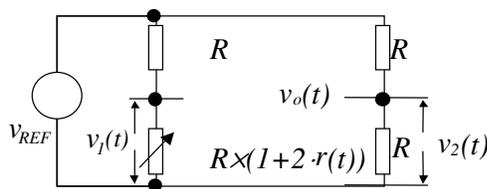


Figure 4.1 : Resistive bridge, with one variable element, v_{REF} is a constant reference.

Input resistor variations were manually adjusted for several values in a differential range going from $r = -0.1$ to $r = +0.1$. Reference to the bridge uses a simple power source (with $V_{REF} = \pm 7V$, with measured noise level of $V_{noise} \approx 40mV$). It has a slow drift, due to heating, making the reference signal oscillate $\pm 10mV$ in an interval of several minutes.

Figure 4.2 displays the acquisition setup. For practical reasons the circuit used as reference was a Gaussian noise (with standard deviation, $\sigma = 0.25$, normalized to the nominal generator amplitude) obtained from a signal generator (HP33120A) and band

limited using a second order low-pass filter ($F_c = 350\text{kHz}$, $\text{Gain} = 4$). Maximum noise amplitude was restricted to nearly $4V$ in the comparators inputs. To quantize such signal two *LM311* were used to compare the reference with the values of v_1 and v_2 . Data was acquired using an oscilloscope at a maximum sampling frequency $F_O = 500\text{Ms/s}$ (HP54645D). Output linearization employed an expression $\Gamma(m)$, like the one explained for Gaussian references in chapter 2.

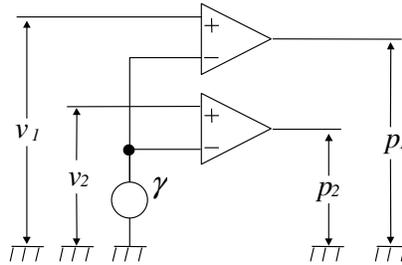
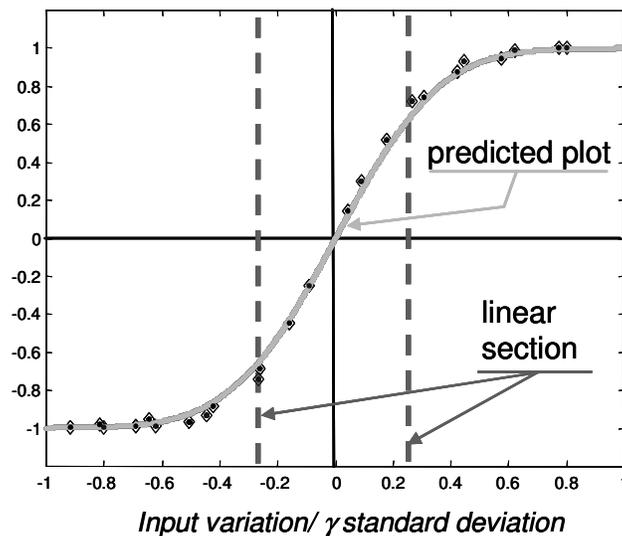


Figure 4.2 : Differential bridge acquisition setup: the noise source presents a Gaussian distribution.

Since the equivalent model $\Phi(v)$ for the SS-ADC using a Gaussian function saturates when v is near $\pm 3\sigma$, one must observe two things: (i) signal range must be restricted (in another words the amplitude of the reference γ must be higher than the dynamic range of v_1 and v_2); (ii) as predicted one should expect lower resolution at the fringes of the dynamic range.

$$m = \frac{1}{N} \sum_{n=1}^N (p_1[n] - p_2[n])$$



(a)

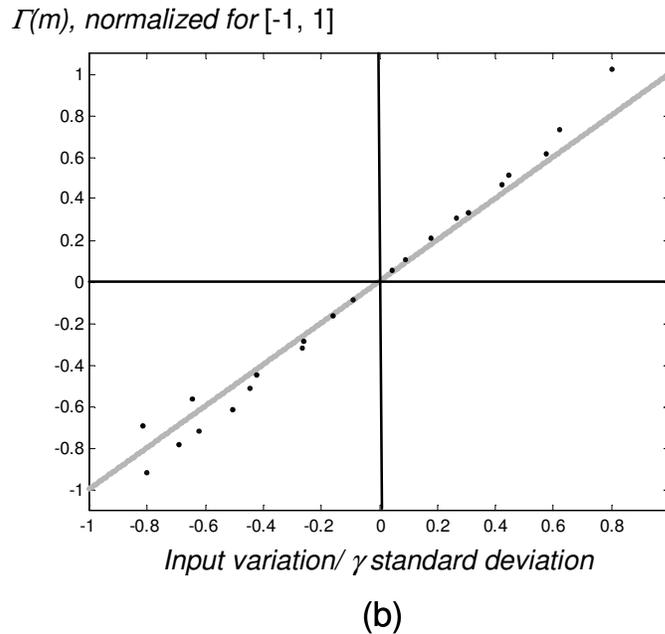


Figure 4.3 : Matching of the points measured with the expected linearized values of m . (a) Shows the typical *erf* shaped output plot; (b) estimated values of r after linearization.

$$m = \frac{1}{N} \sum_{n=1}^N (p_1[n] - p_2[n])$$

In figure 4.3a one sees that measured values for m agree with the expected *erf*-like characteristic of $\Phi(v)$. Figure 4.3b shows the same points after processed by the ideal $\Gamma(m)$ i.e. the reconstruction model adjusted to the design parameters of the converter without tuning to compensate for variations on the implementation. One can see that the scattering of the measured points are in good agreement with the variations expected for the averaging depth employed. Also, as the x-axis is shown normalized by the standard deviation it is easy to see that with input values restricted to the range $[-\frac{1}{4} \cdot \sigma, +\frac{1}{4} \cdot \sigma]$, $\Gamma(m)$ can be fitted by a linear function.

4.2 Analog Acquisition with Pseudo-random Generation

The second application is pretty much similar to the previous one. The idea here is again the acquisition of data with a single comparator and a stochastic multilevel reference. The main difference is in the reference generator: instead of a Gaussian generator, a simple pseudorandom source, like the one explained in section 3.4 was employed. Sample and hold circuits were interposed between the generator and the comparator. Two sampling pseudorandom sequences i_1 and i_2 were provided by digital LFSRs implemented in an Altera UP1 prototyping board. An oscilloscope with four digital inputs was employed to acquire the data. The complete circuit is depicted in figure 4.4. In this diagram n_{VI} stands for the number of valid inputs, obtained after the datapath fault detection stage. The control block uses this number to determinate both the minimum averaging depth (N) in order to achieve the desired resolution and the error margins (ϵ) in each comparator employed for online fault detection.

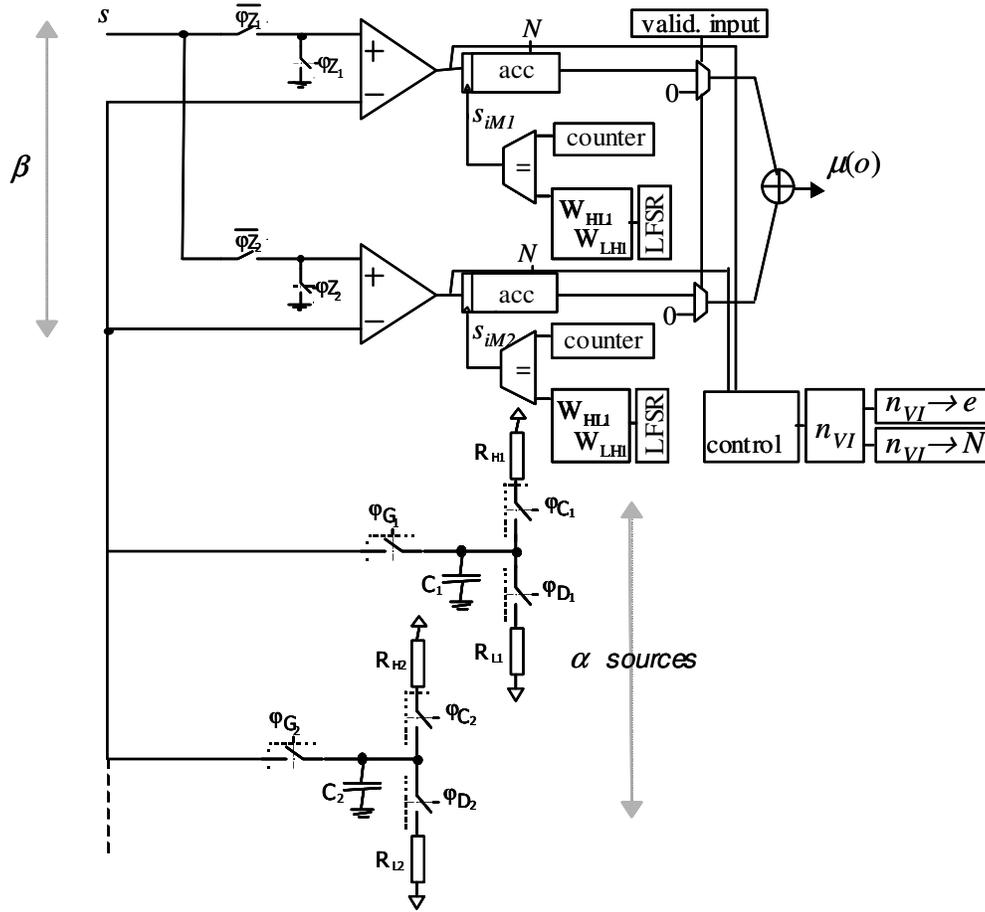


Figure 4.4 : Setup for the SS-ADC with a pseudorandom reference.

In order to determine the equivalent model of the SS-ADC it is necessary to determine the distribution of the reference signal (γ). In this case, the analog reference is generated by a charge-discharge circuit, whose behavior is described by normalized equation (4.1).

$$a_{ref}(t) = \begin{cases} 2 \cdot \left[-1 + \exp\left(-t/\tau_{LH}\right) \right] + a_H, & t \in [0, T_{ref}/2] \\ 2 \cdot \left[+1 - \exp\left(-t/\tau_{HL}\right) \right] - a_L, & t \in [T_{ref}/2, T_{ref}] \end{cases} \quad (4.1)$$

Thus, applying the method described in section 3.5.1, one calculates the expected output PDF as given by equation (3.8). Where $u_I[a, b]$ is a step window with value $u_I[a, b] = 1$ for $y \in [a, b]$, and $u_I[a, b] = 0$ for the remaining values of y .

$$P(\gamma) = \begin{cases} \left[\left(\frac{\tau_{LH}}{y+1} \right) - \left(\frac{\tau_{HL}}{\alpha_1 - y} \right) \right] \cdot u_1[-\kappa_1, 1] + A_1 \cdot u_0[+1], & \tau_{LH} > \tau_{HL} \\ \left[\left(\frac{\tau_{LH}}{y + \alpha_2} \right) - \left(\frac{\tau_{HL}}{1 - y} \right) \right] \cdot u_1[1, -\kappa_2] + A_2 \cdot u_0[-1], & \tau_{LH} < \tau_{HL} \end{cases} \quad (4.2)$$

In equation (4.2), $u_0[a]$ denotes one unitary impulse located in a . For $P(\gamma)$ this impulse is related to the area of the graph that is "cut out" by the saturation. The constants κ_1 , κ_2 , α_1 , α_2 , A_1 , A_2 , are determined by the values of τ_{HL} and τ_{LH} . This relationship can be more clearly understood in the figure 4.5.

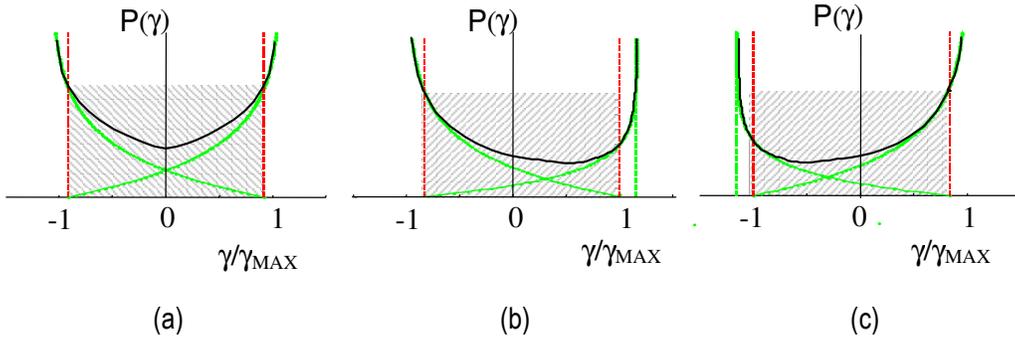


Figure 4.5: The shadowed area represents $P(\gamma)$ for different relations between the time constants for the rise τ_{LH} and fall cycles τ_{HL} of aref : $\tau_{LH} = \tau_{HL}$ (a), $\tau_{LH} > \tau_{HL}$ (b), $\tau_{LH} < \tau_{HL}$ (c). Parametric variations on the reference generator can be compensated by tuning the digital linearization model.

Applying the same procedure described in section 2.2.5 to equation (4.2) one determines the equivalent model of this SS-ADC ($\Phi(v)$), and as a consequence defines the mapping equation $\Gamma(m)$. Figure 4.6 shows the matching between the theoretical model and the output of a slope acquisition.

The most important thing to note about $\Phi(v)$ is that, once the real parameters of the circuit are determined, one can change the linearization model accordingly. The circuit feature variation range defines the maximum non-linearity at the output. The function $\Gamma(m)$ can be used to linearize the outputs in the same fashion that was shown for outputs of statistical sampling with Gaussian noise in the chapter 2. Figure 4.7 shows Γ applied to the outputs shown in figure 4.6a.

For the linearization of the measured data, initially RC timing data was acquired and used to fine-tune $\Gamma(m)$. Afterwards, while working with fault-tolerance, a simple procedure based on counting the time taken for each low-to-high and high-to-low transition was developed. This procedure is further explained in section 5.3.

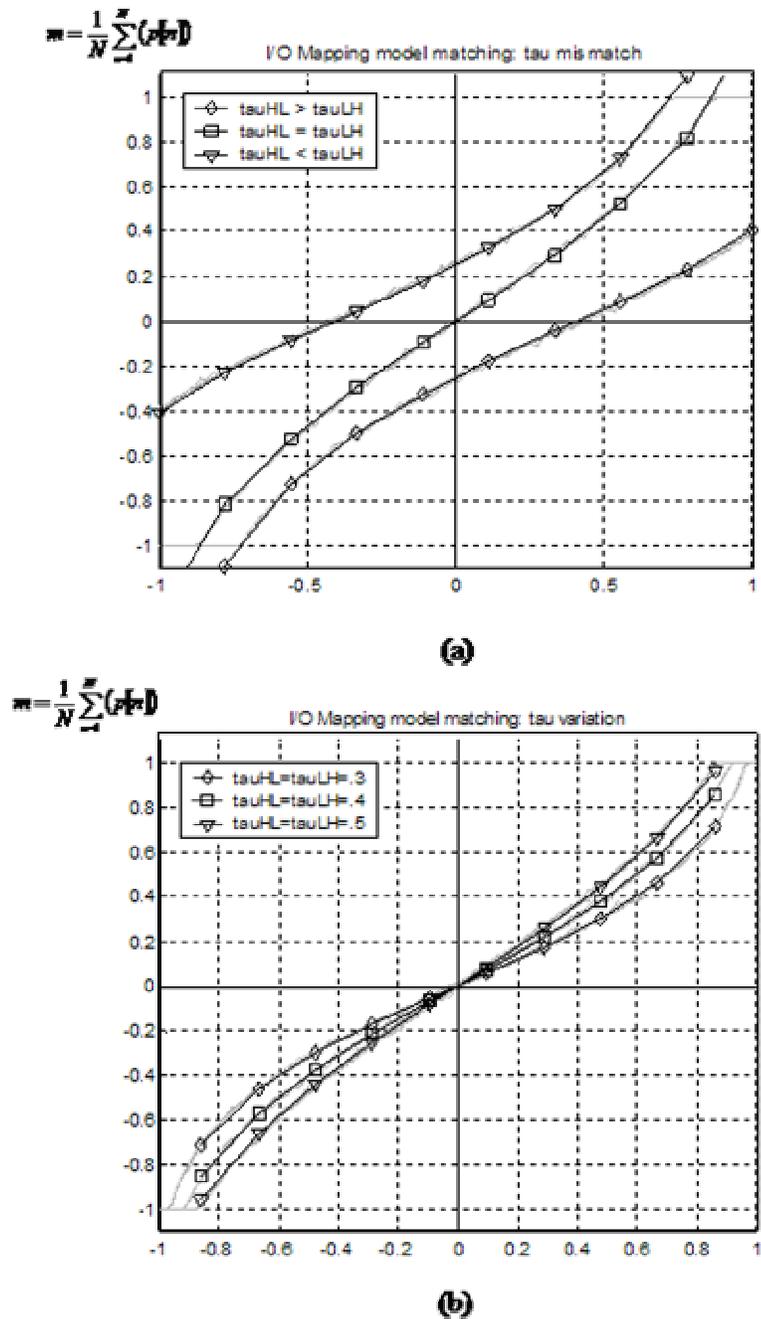


Figure 4.6: Theoretical model and averaged input/output mapping. The model reproduces the expected circuit input/output behavior for each comparator (function $\Phi(v)$) before linearization. (a) $\Phi(v)$ follows a big mismatch between τ_{HL} and τ_{LH} in the reference (60%). (b) $\Phi(v)$ follows non-linearity variations with different values for the generator constants (τ_{HL} and τ_{LH}).

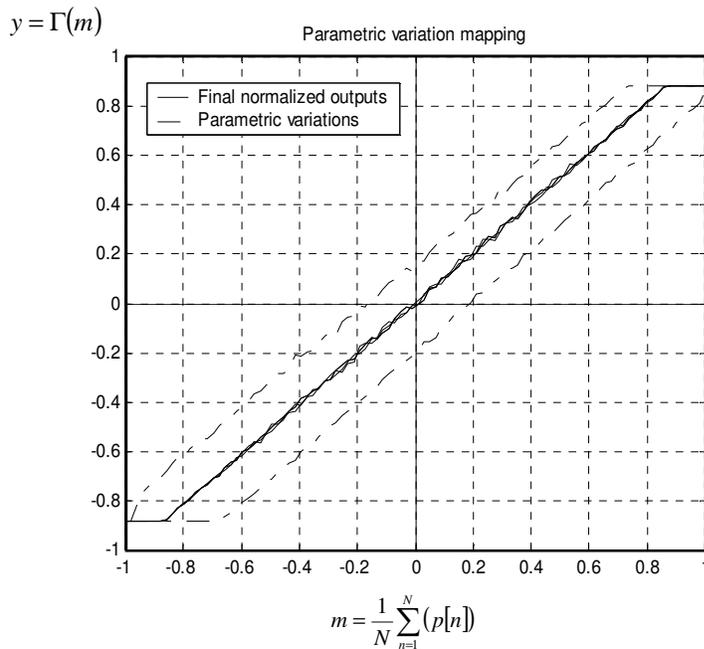


Figure 4.7: Outputs $y = \Gamma(m)$ - the dashed lines show the model outcome for $\pm 10\%$ parametric variations in the references. Solid lines show final outputs after zero subtraction.

4.3 Linearization through Non-Uniform Sampling

The use of a pseudorandom analog signal generator opens up another approach to make the digital compensation of the non-linearity's in the mapping $\Phi(v)$ between the input v and m (where m is our best estimation for $\mu(p)$ within the sampling interval T). The modeling strategy that have been used consists in defining a mapping function $\Gamma(m)$, such as $\Gamma(m) = \Phi(v)^{-1}$ and use it to post-process the averaging results.

Now, since the random sequence that determines the sampling intervals in the pseudorandom reference generator is under the control of a digital random number generator, one can change this algorithm in order to guarantee that the output of our generator will have a uniform distribution. Since a uniform distribution provides a linear mapping between system first order statistics, the SS-ADC non-linearity will be kept at lower values. This section shows how this can be achieved using a modified pseudorandom number sequence i_m with a non-uniform distribution adequately chosen to compensate for the characteristics of the periodic analog signal a_{ref} .

From section 3.5 one knows that each monotonic section of a_{ref} contributes to $P(\gamma)$ with a term that is proportional to derivative of the inverse of the function describing a_{ref} in that section. In other words, assuming a_{ref} is the charge-discharge circuit, there will be a part of the $P(\gamma)$ that is due to the high-to-low transition ($P_{HL}(\gamma)$) and another part that is proportional to the low-to-high transition ($P_{LH}(\gamma)$). If f_{LH} and f_{HL} are functions that

describe the behavior of a_{ref} during the transitions, it is known that

$$P_{HL}(\gamma) \propto \left\| \frac{\partial(f_{HL}^{-1})}{\partial t} \right\|,$$

and

$$P_{LH}(\gamma) \propto \left\| \frac{\partial(f_{LH}^{-1})}{\partial t} \right\|.$$

As the digital portion of the SS-ADC controls the switches of the sample and hold block and also triggers the transitions of the charge-discharge circuit, it is possible to define a digital block W such as $i_m = W(i)$ for each of the monotonic sections of a_{ref} . Once this is realized it is just a matter of performing a couple of algebraic operations to

determine $W_{HL}(i)$ and $W_{LH}(i)$. In fact,

$$P_{HL}(\gamma) \propto \left\| \frac{1}{\partial(f_{HL})}{\partial t} \right\|,$$

and, after uniformization one

has

$$P_{HL}(\gamma) \propto \left\| \frac{1}{\partial(f_{HL}(W_{HL}(i)))}{\partial t} \right\|,$$

where the derivative in the denominator must be made equal to the unity.

Using a roulette-like algorithm where each time-slice n (out of L time slices) has the probability to be selected determined by equation (4.3) one can map a uniform selection sequence i , to a non-uniform random number sequence i_m which will generate a uniform distribution in γ .

$$i_m[n] = \begin{cases} 2 \cdot \exp\left(-t/\tau_{LH}\right) & , n \in [1, N_i/2) \\ 2 \cdot \exp\left(-t/\tau_{HL}\right) & , n \in [N_i/2, N_i] \end{cases} \quad (4.3)$$

Figure 4.8 compares the results of analog signal acquisition using both the linearization model and the non-uniform sampling in the generator. It can be seen that although for this particular set of parameters output resolution was better for the non-uniform sampling method over most of the input range, non-uniform sampling in the generator was not able to deal with the extreme non-linearity on the fringes of the dynamic range.

Using this approach has the advantage of requiring a less demanding digital block, once average post-processing is not-required. However, this technique has a flaw: when L is too small, and the time constant (τ_{LH} or τ_{HL}) is high, the resulting reference γ will not have the desired flat PDF. For a high L sampling interval T must be several hundred times the clock period. Since the statistical sampler is an over-sampling converter this further constraint on the reference noise bandwidth restricts the applications of the converter, to very-low frequency instruments.

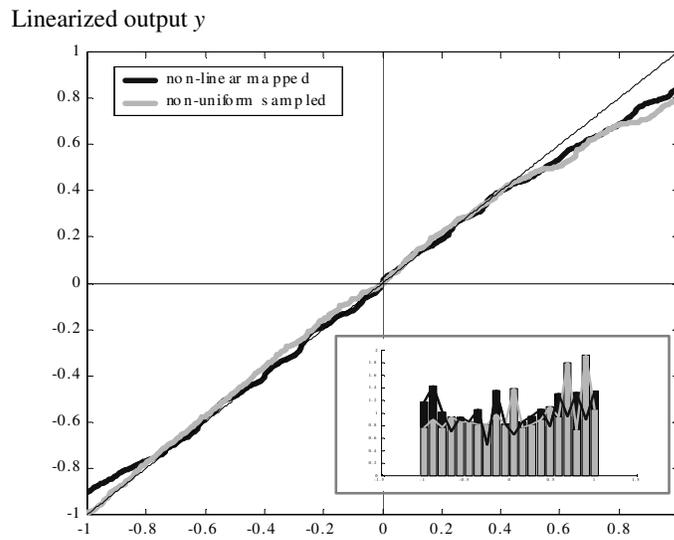


Figure 4.8: A comparison between the slope acquisition with non-uniform sampling with a roulette function $W(n)$ and using a linearization function $\Gamma(m)$. The gray line shows the output of the non-uniform sampling method and the black the output of the post-linearization method.

5 UNFOLDING THE DESIGN LANDSCAPE

The aim of the previous chapters was to show how analog signal statistics can be acquired using a very simple analog block composed of comparators and multilevel noise sources. It was also shown that a well known, albeit usually nonlinear relationship can be established between the statistics of the input analog signal v , and the statistics of the resulting bitstream p . Moreover, the dependency of this relationship upon the shape of the Probability Distribution Function of the employed reference noise γ was demonstrated and quantified for a couple of cases. It was also possible to delineate the main drawbacks of stochastic quantization in general, and the statistical sampler setup in particular.

It is clear that, for any expected resolution r , the statistical sampler will require an averaging depth N that grows exponentially with this resolution. As the averaging depth increases, the maximum operation frequency of the analog input decreases in the inverse proportion. That makes the resolution/ bandwidth ratio of a single statistical sampler rather unfavorable. It is that limitation that raises questions on whether one could build upon this basic block increasing the relationship between resolution and bandwidth.

This chapter focuses on investigating a set of tools that allows one to achieve a better performance within the framework of statistical sampling. Of course, any improvement over the original circuit will have a cost in area, but the question one wants to deal with is whether this improvement is reached in a way that keeps the circuit able to fulfill its proposed goals, i.e. it can be achieved using low cost analog blocks, and treating non-idealities in the digital domain. To accomplish this goal, two other important tools are employed: self-configuration and redundancy.

5.1 Redundancy and Performance of ADCs

The first important notion behind this chapter is that one can use redundancy of analog blocks to improve the ratio between the performance and analog area required for a given comparator based ADC. The concept was introduced by Flynn and Bogue (2003), and afterwards fully developed in another paper (FLYNN; DONOVAN; SATLER, 2003).

In any traditional flash ADC the input is compared with several values of ascending trip voltages. In this situation, comparator mismatch and offset will cause the comparison thresholds to vary. This variation will impact on the ADC linearity and total performance. To keep offset under acceptable values analog matching methods must be used. For small low cost comparators this variation can lead even to a non-monotonic characteristic in the ADC. As comparators designed on digital CMOS technology suffer

from higher electrical feature variations that are inherent to the digital technologies, ADCs implemented with such comparators will surely require the employment of parameter matching methods, i.e. device sizing, offset nulling, averaging and trimming.

In this setup, redundancy comes in as a way to provide several comparators per comparison threshold. As the system provides an input reference, the best comparator per code is selected in a self-configuration stage. The main point is that using self-configuration to select the best comparator per code it is possible to reduce the total amount of analog area for a given performance. In fact, provided self-calibration is present, using better and larger comparators can be more expensive than employing the same area to design redundant small ones. Figure 5.1 adds further detail to the overview of the Flynn's architecture.

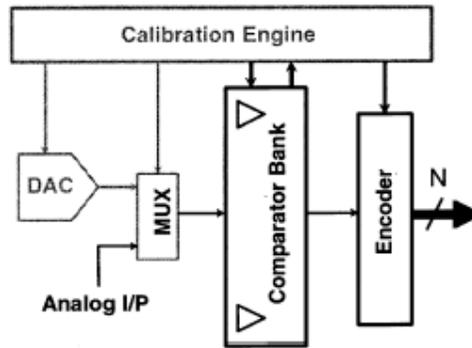


Figure 5.1: Using redundancy to improve performance in a flash ADC (FLYNN; BOGUE, 2003).

Although originally developed to flash converters, this idea is particularly interesting to be applied to the statistical sampler for several reasons. First, statistical sampling is already a process based on comparison with an external reference which is a requirement to self configuration of redundant blocks. Also, as it will be more thoroughly explained in the next section, one can add redundant parallel comparators to decrease the averaging depth N required to achieve a resolution in the SS-ADC. During this process, pruning of the worst inputs can be easily accomplished also in the digital domain.

5.2 Parallel Statistical Sampler - PSS

As it was seen in chapter 2, since the resolution is directly proportional to the square

$$r = \log_2 \left(\frac{\sqrt{N}}{k_u} \right)$$

root of N , (in fact,) it is possible to quantify the tradeoff between resolution and maximum averaging depth in a given SS-ADC. A higher value for N will mean a higher resolution, but at the same time a possible lower maximum input frequency. This tradeoff is summarized on equations 5.1 and 5.2.

$$r = \frac{1}{2} \log_2 \left(\frac{N}{k_u} \right) \quad (5.1)$$

$$F_{MAX} = \frac{F_{SAMP}}{2 \cdot N} \quad (5.2)$$

Starting with these relations it is possible to devise that a rather intuitive way to improve the relationship between resolution and maximum input signal frequency is using several (say a number β) statistical samplers in parallel to acquire the same inputs, combining the results in the digital domain. Assuming in each comparator this analog input uses a noise source with the same distribution and that these sources are uncorrelated to each other, and defining M as the total number of averages including the totalization of the parallel comparator outputs ($M = N \cdot \beta$) one will have that the same equations can be rewritten as shown in 5.3 and 5.4.

$$r = \frac{1}{2} \log_2 \left(\frac{N \cdot \beta}{k_p} \right) = \frac{1}{2} \log_2 \left(\frac{M}{k_p} \right) \quad (5.3)$$

$$F_{MAX} = \frac{F_{SAMP}}{2 \cdot N} \quad (5.4)$$

The redundancy factor β can thus be used to better fit the system requirements. To make this relationship hold true the references for each of the β comparators ($\gamma_1 \dots \gamma_\beta$) must keep the same PDFs. Now, it is clear that using multiple analog noise sources this will not be true, the same for different comparators, since high variations in the offsets will impact in the bias values for the output bitstreams of each comparator ($p_1 \dots p_\beta$). Figure 5.2 shows the impact of bias variations in the reference for the acquisition of the same input using Gaussian noise. In this plot, the input v is a single slope sweeping the dynamic range, also $m_1 \dots m_\beta$ are the outputs after averaging the bitstreams of each comparator ($m_j = \overline{p_j}$).

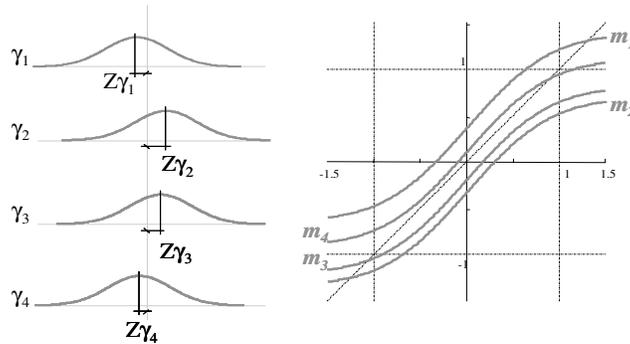


Figure 5.2: Multiple reference offset impact on the average output of each comparator.

Figure 5.3 shows the effect of variations in the standard deviation of the Gaussian reference. This could happen for instance when several independent analog noise sources are employed. Both situations will have different impacts of the PSS architecture.

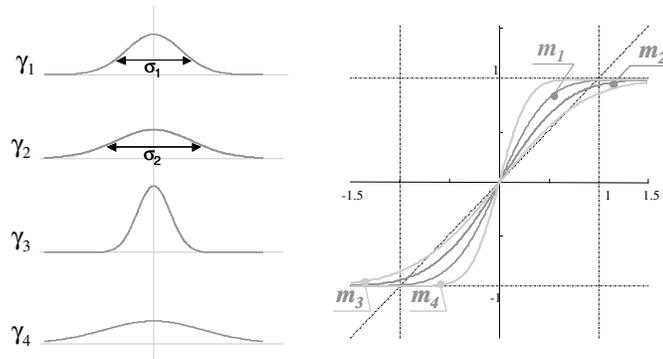


Figure 5.3: Multiple reference deviation impact on the average output of each comparator.

From chapter 3 one knows that there are alternatives that allow one to use a single analog reference in order to provide several uncorrelated multilevel noise sources. Using the proposed reference random samplers (whether using Gaussian random or a periodic signal as the original analog source) one will end up with a situation that is pretty similar to the one depicted in figure 5.1, main variations between outputs will be due to bias in the comparators. In this situation, and assuming the analog reference is well characterized, a calibration stage is only required to determine zero in each of the comparators.

If more than one analog reference (say a number α of references) is employed, the output averages can not be directly added. In this situation since input-output relationship for the outcomes of each source will be different, linearization must take place in every comparator using the known parameters of each of the analog sources. Figure 5.4 compares both setups.

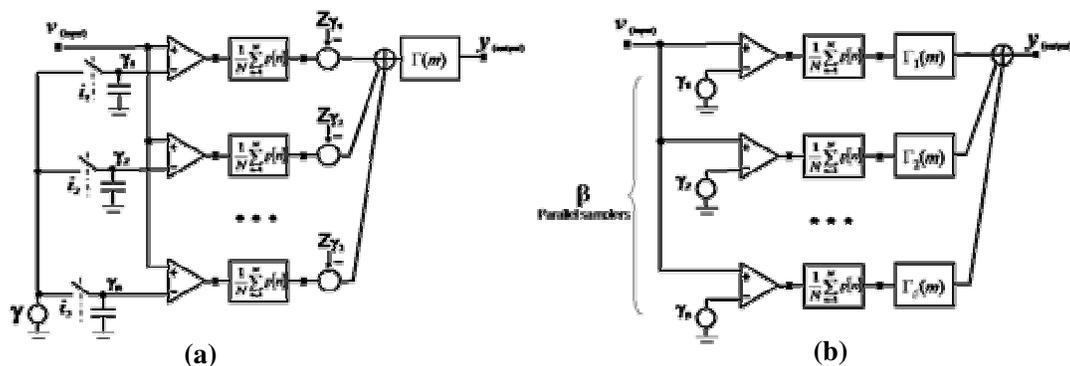


Figure 5.4: PSS architecture (a) with a single analog reference and pseudo-random scrambling and (b) with separate and uncorrelated analog generators.

5.3 Self-test and Fault Tolerance Issues

If either architecture is employed (with a single source and scrambling or with multiple analog sources or a mix of both), there will remain the problem of determining the statistical parameters of the noise source, since these parameters will impact in the

linearization blocks $T_{n=1..β}$. There are at least three ways this problem can be approached:

1. One can try to guarantee the properties of the ADC by designing an analog reference with low parameter mismatch. Since this will only be required for the analog source and low-cost comparators can be used (with zero-setting), the area overhead will not be too high and linearization functions will be preset;
2. One can provide the ADC with the means to self-tune both generators and offsets. This approach will require at least two precise voltage references. This again is feasible since its cost is much lower than a single resistor ladder for a two-bits flash comparator. In this situation parameters of the linearization functions are set using the data thus gathered;
3. One can use the linearization functions preset for the design parameters, assuming that there will remain a non linearity in the output and using some adaptive post-processing to deal with it. This approach may be valid for specific applications where a dynamic reference signal is already available.

The first two situations are covered below for SS-ADCs using pseudo-random noise and Gaussian noise. The remaining is partially addressed by the discussion over filtering techniques on section 5.5. A very important consequence of the redundant parallelism the SS-ADC presents is its natural ability to deal with applications where a fault-tolerant analog acquisition with graceful degradation of performance is required. This application is further developed in section 5.6.2.

5.3.1 ADC Self-configuration with Pseudorandom Noise

A PSS implementation with pseudo-random noise generators and a leaky integrator is depicted in figure 5.5. First step at the configuration stage is to verify the interconnection network. The redundancy of the configuration allows two types of measures that can be taken to deal with an error in the analog acquisition paths: (i) to discard an analog reference or, (ii) to discard a comparator.

For every α reference generator (using the switches ϕ_{Gi}), one sets the output to either +Vcc or -Vcc (with ϕ_{Ci} and ϕ_{Di}). Zero switches (ϕ_{Zi}) are grounded, and, toggling the generator output, one verifies the outcome of the comparators. Stuck-at faults on the generator switches or components will be detected in all the comparator outputs, faults in each comparator switches will be detected only in that comparator output. The references and comparators that survive this step are marked as active, the remaining are discarded.

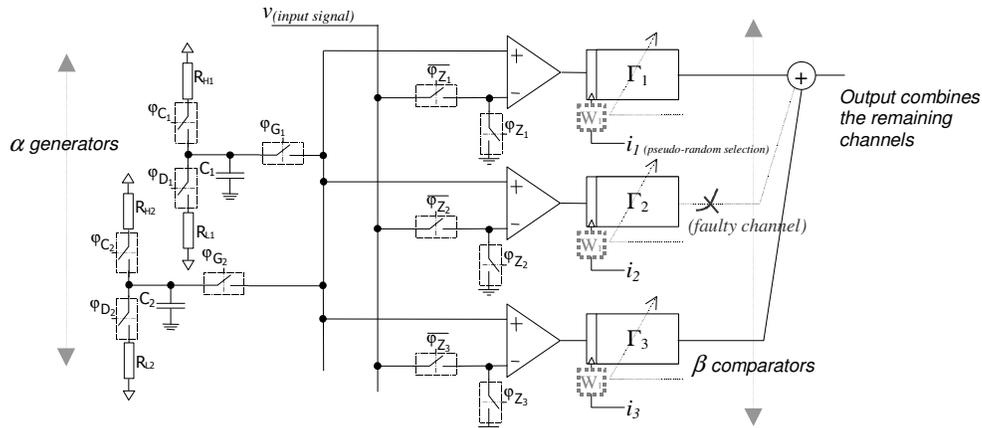


Figure 5.5: Complete PSS architecture employing a pseudo-random reference generator.

To characterize the analog generators and adapt the digital reconstruction models, one must only keep track of the number of clock cycles that takes each comparator output transition (figure 5.6). This procedure can be repeated several times for a better characterization.

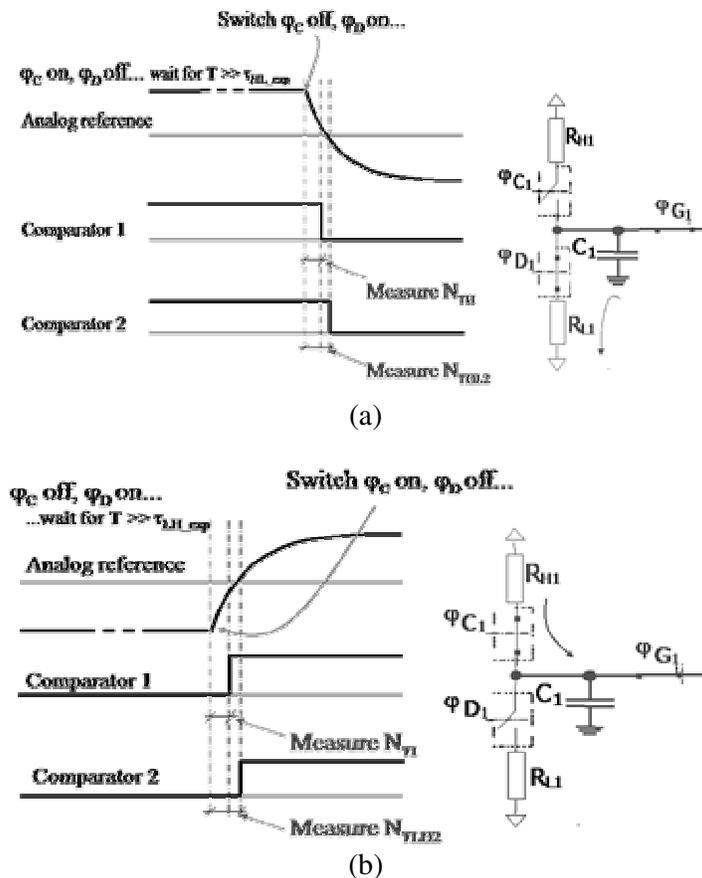


Figure 5.6: Measuring the real parameters of the analog reference to adjust the linearization. (a) Measure T_{HL} . (b) Measure T_{LH} .

If any output fails to change state within the maximum expected time range, it is assigned as not working and let aside at the operation stage. If one wants to keep non-linear error at the lowest possible value, the allowed variation for the time constants will

be very limited. Using the measured generator parameters to set the digital linearization block, parametric variation in the generators is permitted to reasonable degree.

Once the values for τ_{LH} and τ_{HL} are determined, the device adjusts T_{ref} such as it matches two times the larger transition interval. Both low-to-high and high-to-low transitions are set to take $T_{ref}/2$. At this point, online transition values are set for each of the enabled input channels and the charge switches begin acquisition regime ($\varphi_{Ci, i=1..α}$, $\varphi_{Di, i=1..α}$). Using this parameter setup, input offset value is determined for every active channel. This is done by grounding the inputs (using switches ($\varphi_{Zi, i=1..β}$), and calculating the output average obtained in each comparator.

5.3.2 ADC Self-configuration with Gaussian Noise

Given the prevalence of Gaussian noise sources among the many available circuits, it worth mentioning how the main configuration steps could be applied to statistical samplers with Gaussian shaped references. In fact, since the determination of the offset can employ the same procedure already described to pseudo-random references and any Gaussian shape can be characterized by just two parameters (standard deviation and mean), one will only have to define a reasonable way to estimate the standard deviation of the source.

Assuming one has two precise reference thresholds t_{R1} and t_{R2} , it would be useful to know how the measured values of these references (y_{R1} and y_{R2}) can be used to estimate the generator parameters. Figure 5.7a shows the output plot for the statistical sampler with an ideal Gaussian generator and for one with different deviation and not zero centered distribution. Input is a slope signal. Plot 5.7b shows the outcome after linearization. One can see how the reference points are reflected. In fact it can be shown that variations in the standard deviation will change the output slope angle with the x-axis, while variations in the distribution center will just shift the output in the y-axis.

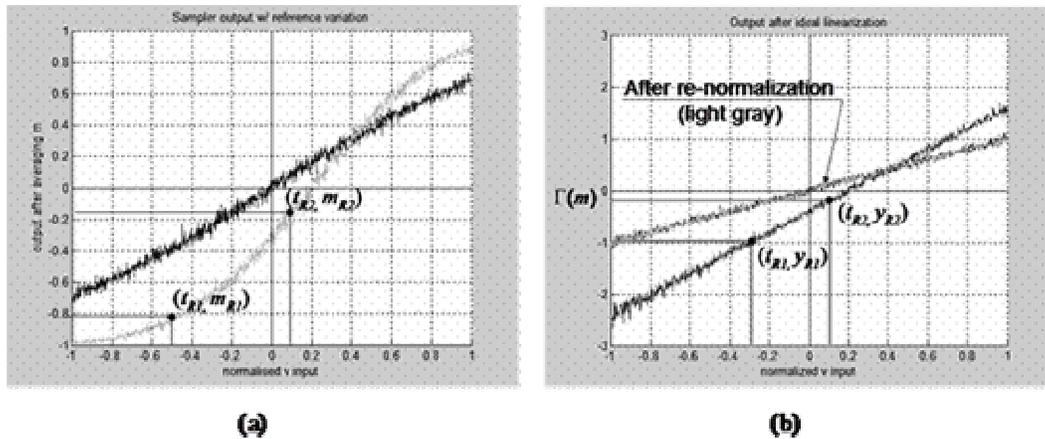


Figure 5.7: Acquisition with variation in the Gaussian reference distribution. (a) shows the outcome before linearization, and (b) after applying the ideal function $\Gamma(m)$.

Given this, adjusting the linearization function in such situations becomes just a matter of re-normalizing the output plot using the two known points as a reference. In a self-configuration stage the input is set to each of the reference values and acquired. After this the acquired values are used to adjust $\Gamma(m)$. The light-gray plot in figure 5.7b shows the matching of the output after renormalization.

The same considerations regarding the resolution of the initial acquisition of the reference points must be emphasized: one should preferably use one of the reference points near the center of the input dynamic range, while the other would be at the fringes, but preferably within range of one-third of the expected standard deviation. This would put both of them in a region where acquisition have a better relationship between resolutions and required averaging depth (N).

5.4 Generalized Parallel Statistical Sampler - GPSS

Once the basic operation of the PSS is well understood and its main advantages are known, one clear question that comes to mind is whether the same approach could be employed using comparison elements (CEs) with a higher number of bits, and whether there would be any advantage to it.

Figure 5.8 shows a generalized topology with an arbitrary number β of comparison elements, each of them with a number l of different voltage thresholds. Analog reference γ is added to the input value by means of passive resistor circuit. The comparison element (CE block) follows a mid-raising characteristic for easy compatibility with the one bit comparator case and is implemented through resistor ladder and l comparators.

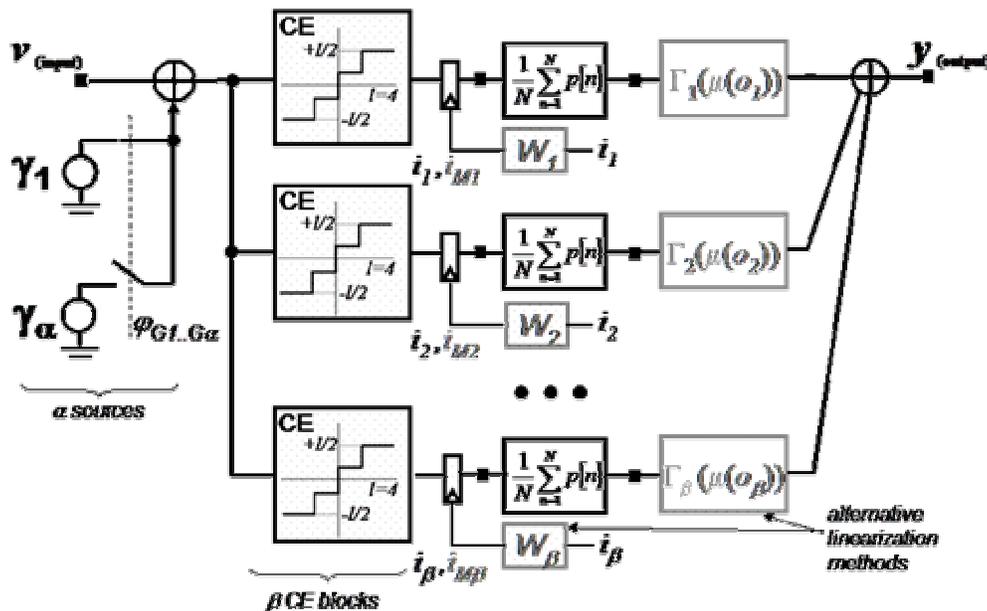


Figure 5.8: GPSS architecture: α , β , N , and l are design parameters.

Although a single analog reference is required for the circuit to perform an acquisition, due to its low-cost, a total of α reference generators may be present. Inside the CE, each of the l comparators have its own output p_n , the combination of this comparator outputs generates the total output of the CE block (called o). For each of comparator output $p_{n=-l/2, \dots, -2, -1, +1, +2, +l/2}$, the probability distribution of the output $P(p_n)$ can be calculated using the same approach used in chapter 2. However, in order to estimate the output average of each CE block, one must first determine the conditional probability of each output symbol $P(o | (n-q \leq o < n+(q+1)))$ and use expression (5.5).

$$\mu(o) = \sum_{n=-l/2}^{n=+l/2} n \cdot [P(o|_{o \geq n \cdot q}) - P(o|_{o \geq (n+1) \cdot q})] \quad (5.5)$$

Equation 5.5, can be developed applying quantization analysis over $P(o)$. In fact, if s is the output of the addition of the analog input v and the reference γ ($s = (v - \gamma)$), one

$$P(o|_{n \cdot q \leq o < (n+1) \cdot q}) = \left\{ - \int_{(n+1)q}^{\infty} [P(s) \cdot \partial s] + \int_{n \cdot q}^{\infty} [P(s) \cdot \partial s] \right\}$$

knows that

To proceed one assumes that $t_{-l/2}, \dots, t_{-1}, t_1, \dots, t_{+l/2}$, are the voltage thresholds of comparison for each of the comparators, for a ideal regular resistor ladder $t_n = (n \cdot DR(v))/m$, where $DR(v)_{MAX}$ is maximum dynamic range of the analog input v .

$$F(x) = \int_x^{\infty} [P(s) \cdot \delta s]$$

In this situation, if one defines $F(x)$, for the central symbols one can say that the equation $P(o = n \cdot q) = P(o|_{n \cdot q \leq o < (n+1) \cdot q}) = F(s + t_n) - F(s + t_{n+1})$ holds, while for the superior and inferior limits the probability distribution is given by $P\left(o \geq \pm \frac{l}{2} \cdot q\right) = F\left(s + t_{\pm l/2}\right)$. As the average of the output ($\mu(o)$) will be given by the sum of the probabilities of each output symbol weighted by the value of the symbol, one is able to determine its algebraic expression.

As an example figure 5.9 shows the average output results for an acquisition with a two-bit CE, using references with Gaussian shaped PDFs and the matching to the expected average based on the statistical sampling model. The employed algebraic expression assumes a uniform resistor ladder in the CEs.

Once the main elements of analysis to the GPSS are in their place, total system performance and cost can be evaluated as functions of the design parameters (α , β , N , l , and for GPSS with pseudo-random references, τ_{HL} and τ_{HL}). The first element that has an impact over the output resolution is the generator non-linearity. As it was seen before, the non-uniformity in the generator PDF is reflected in the acquisition for any number of bits per comparison element, even for the single bit blocks of the PSS. However, for multi-bit CEs total non-linearity is even higher at the dynamic range fringes, where there are higher gains. A consequence of the non-linearity is the variation of the maximum resolution over the dynamic range

One can evaluate the dynamic behavior of the GPSS circuit applying a two-tone signal to the input. Using this procedure, figure 5.10 shows resolution as a function of over-sampling employing the GPSS circuit with different number of bits in the CEs.

Multi-bit CEs increase total resolution at the cost of a decreased linear dynamic range. Two other issues must be considered: the total analog area cost and the inherent fault-tolerance and process insensitivity. It is possible to have a simple estimate of the area cost taking the minimum number of transistors required by each one of the architectures. Figure 5.11 shows this parameter as a function of β and CE's resolution. The two highlighted lines show the topologies that take eight and twelve comparators.

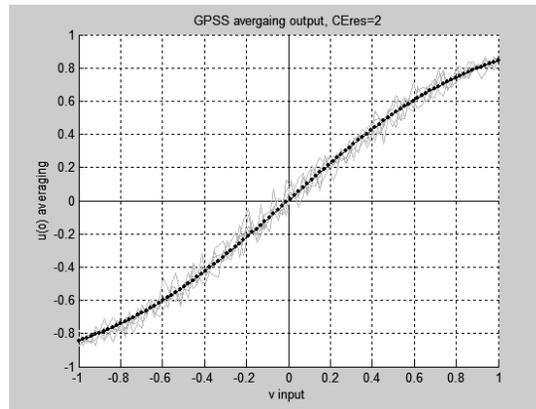


Figure 5.9: Matching of the model in a GPSS and simulated results using a single Gaussian reference with standard deviation 0.5 ($\alpha=1$, $\beta=10$, $N=1000$, $l=2$).

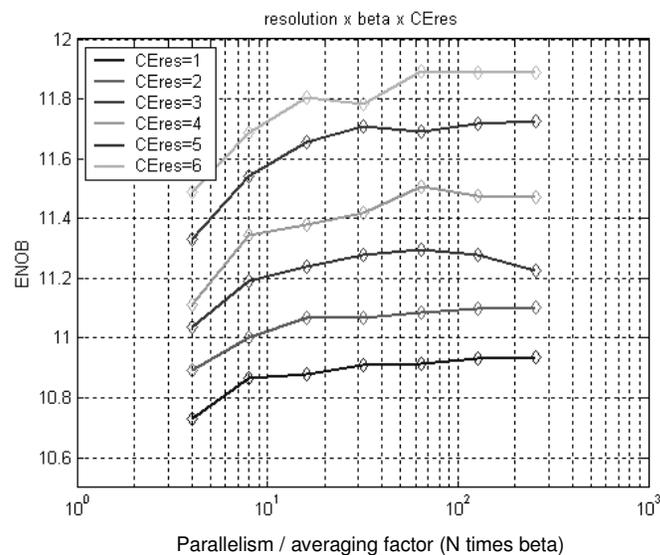


Figure 5.10: Resolution behavior as a function of the factor of parallelism/ averaging ($\beta \times N$) and the resolution of the CE blocks

Assuming a formal tool is designed using this architecture as a reference, it would be rather easy for a designer to explore the design landscape by working the architecture parameters (mainly α , β , CE resolution and N). For instance, applications for tolerance to multiple fault scenarios may require CEs with a lower resolution and higher values of the parameter β , while multi-bit CEs can help applications where the input signal has a higher frequency. Also, as reference variations are dealt by digital modeling, a tradeoff between analog reference source area and the required number of independent sources (α) can be established as a function of the technology employed and the allowed degree of redundancy.

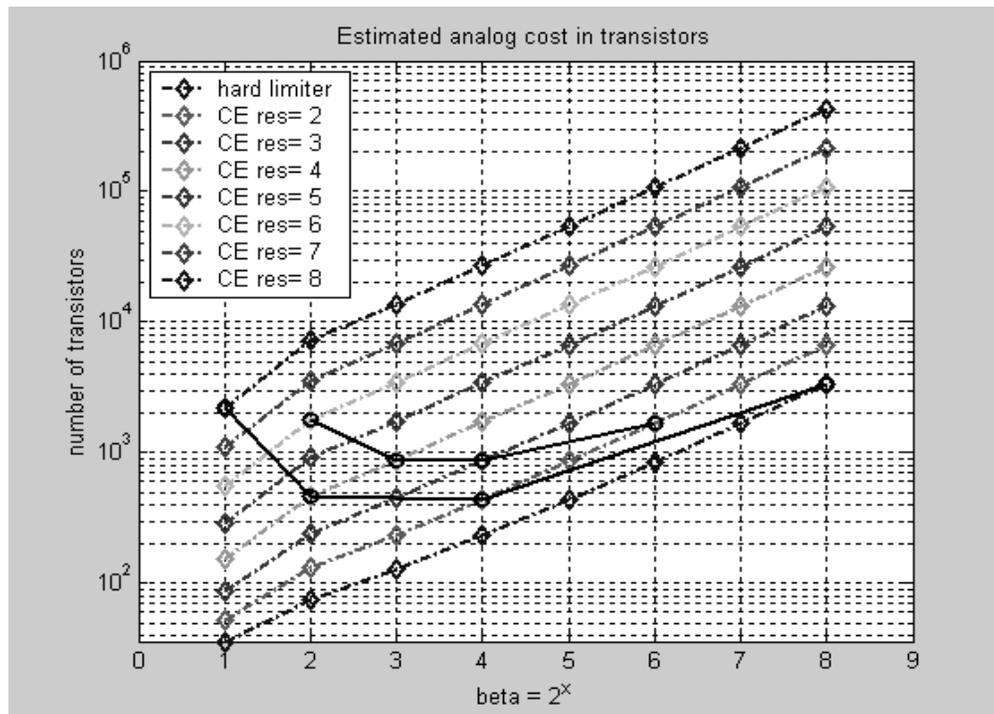


Figure 5.11: Analog area estimates a function of CE resolution and β .

In fact, since ADC self-test is increasingly an important issue in mixed-signal applications, most systems will have to bear some kind of analog reference generator overhead. This is another issue that this line of research have shown: by incorporating the generator, looking for the least costly alternatives for both reference generation and acquisition, and using the digital resources available in most modern SoCs, one ends up with a rather versatile analog acquisition environment. One that is amenable to integration into an ADC design automation tool, have low sensitivity to process variation and can withstand multiple faults.

5.5 Filtering Techniques

The third approach to deal with non-idealities in the analog design blocks is the use of adaptive processing (and particularly adaptive filtering techniques). The core idea here is to use the digitally available data and controls in an adaptive configuration in order to improve SS-ADC performance. From our basic topology one can see that the only window to the analog world that the SS-ADC device possesses is the output bitstreams of the parallel comparators. At the same time, the only digital control output is the random sampling sequence used in the configuration with the pseudo-random generator (Figure 5.12). One must note that while using real noise generators the sampling sequence will also exist but by definition its values will be uncorrelated to the random reference noise levels applied to the comparators and thus can not be used in any control loop.

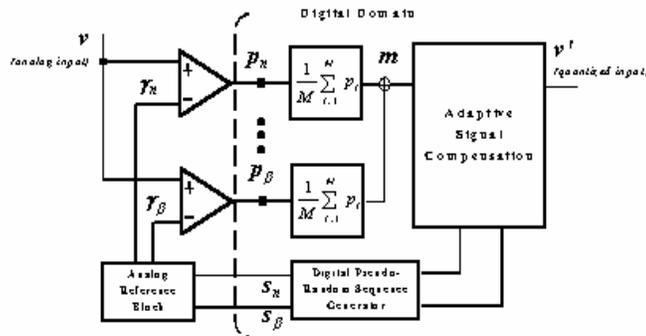


Figure 5.12: Using the adaptive modeling approach to improve SS-ADC.

Two architectures were used in order to test the capabilities of an adaptive filtering block to improve the acquisition performance for a two-tone acquisition application:

1. A self-correlation based architecture to reduce quantization noise and increase resolution, without the need for a configuration reference;
2. A hybrid approach where a pre-linearization is performed by changing the sampling probability in the digital block of the generator using information from the ideal system behavior before the application of the adaptive filter

Another strategy trying to take advantage of the control loop provided by the pseudorandom sampling sequence was also employed, but was not able to show any results. The advantage of these two strategies is that they do not require an external dynamic input generator in order to self-configure. In fact with the availability of an external reference (even a single well-defined sinusoidal signal) several other adaptive architectures would be available. This section will explain both architectures while section 5.6.3 will review the results from a practical setup.

5.5.1 Self-correlation Adaptive Filter Topology

As it was previously explained, the statistical sampler increases resolution by the reduction of output noise levels. A SS-ADC with low averaging in the output will necessarily present a very high level of noise. One first approach to reduce this noise, and thus increase output resolution on a periodic two-tone signal is to use self-correlation delay filter architecture. In this setup the input to the filter and the reference signal are the same bit-stream taken with delay from the input line (figure 5.13).

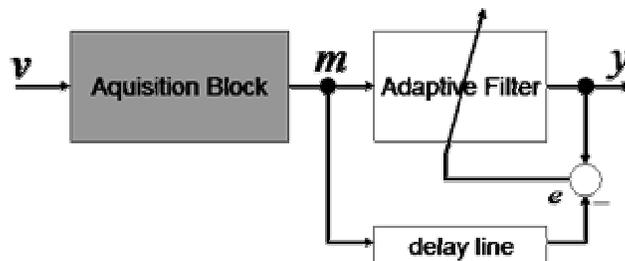


Figure 5.13: Self-correlation adaptive filter structure.

The idea behind this architecture is that the signal will be preserved, since it keeps a strong correlation between samples. At the same time noise is uncorrelated and after the

filtering it will be strongly reduced. Table 5.1 shows the main results of a single tone acquisition with this architecture. The data was pre-processed by averaging with N taps. Results are around three bits higher in resolution, while non-linearity's also show a strong improvement. With post-processing, one can see that it is possible to achieve ENOBs over eight bits. In the same circuit without compensation statistical sampler resolution is about four bits ($ENOB \approx 4$) due to averaging of the bitstream with $N = 40$.

Table 5.1: Single tone results with statistical sampling and adaptive filtering

Time constants	Acquisition performance improvement	
	<i>ENOB</i>	<i>SINAD</i> (dB)
$\tau_{LH} = .3, \tau_{HL} = .4$	7.2503	45.4071
$\tau_{LH} = .4, \tau_{HL} = .4$	8.4898	52.8686
$\tau_{LH} = .4, \tau_{HL} = .5$	7.1555	44.8362

Table 5.2 show the results in the same configuration for a two-tone acquisition. The table displays only the increase in performance due to adaptive filtering. For instance, the upper leftmost improvement result is +3.3187, the total ENOB in this situation is actually 7.362.

Table 5.2: Two-tone acquisition results as a function of the signal bandwidth.

$\tau_{LH} = .32,$ $\tau_{HL} = .32.$	Parameter variation (Δ)		
	<i>F1 @ 0.2kHz</i>	<i>F1 @ 0.7kHz</i>	<i>F1 @ 1.2kHz</i>
	<i>F2 @ 0.7kHz</i>	<i>F2 @ 1.2kHz</i>	<i>F2 @ 1.7kHz</i>
ENOB	+3.3187	+2.6585	+2.0404
SINAD (dB)	+19.9789	+16.0040	+12.2833
THD (dB)	-24.2950	-31.858	-33.793

5.5.2 Hybrid Topology

In the second approach, one uses the previous knowledge about the ideal behavior of our generator to produce a more linear acquisition before subjecting the output bit-stream to the adaptive filter. As the self-correlation filter is not able to deal properly with non-linearity, the idea here is to shape the distribution of the random number generator i in our pseudo-random reference γ in a way that makes the PDF of γ closer to a uniform shape. The pre-uniformization procedure is the same described in detail in section 4.3. It takes advantage of the existence of a well-defined relationship between the probability distribution of the generator and the distribution of the pseudo-random sampling sequences (i). Following the described procedure, two mapping tables are defined with the values of the expected functions W_{LH} and W_{HL} in relation to i . The new sampling sequence i_m is then used to determine the sampling instants in the pseudorandom reference generator.

Since this shaping should be made considering the design values of τ_{LH} and τ_{HL} and a variation between these values and the real parameters on the implemented generator is expected, it is clear that the real resulting output will still be partially distorted, although with much lower values of total harmonic distortion. After this step the same adaptive filter topology explained in section 5.5.1 is then used to increase the total system resolution. Table 5.3 summarizes the results using this approach.

Table 5.3: Hybrid model results, parameter mismatch is assumed as a 20% variation

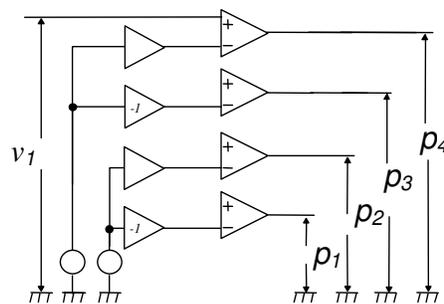
$\tau_{LH} = .32,$ $\tau_{HL} = .32.$	Parameter variation (Δ)		
	<i>F1 @ 0.2kHz</i> <i>F2 @.0.7kHz</i>	<i>F1 @ 0.7kHz</i> <i>F2 @ 1.2kHz</i>	<i>F1 @1.2kHz</i> <i>F2 @1.7kHz</i>
ENOB	+3.7984	+3.1155	+2.9207
SINAD (dB)	+22.9166	+18.996	+15.3943
THD (dB)	-29.4030	-36.233	-37.1787

5.6 Practical Applications

As a way to validate the proposed methods some practical applications were implemented. In the following sub-sections the PSS approach and the filtering post-processing techniques were implemented using prototyping boards and their results were matched to the expected.

5.6.1 A PSS with Four Comparators

To implement a simple PSS-ADC four uncorrelated references were required. Two HP33120A were employed to generate the uncorrelated noise reference. These two Gaussian noise signals were then turned into four using analog inversion in the LM311 inputs. The same simple operational amplifiers were used in every channel and no care was taken to minimize offset contributions in the analog blocks (figure 5.14).



(a)

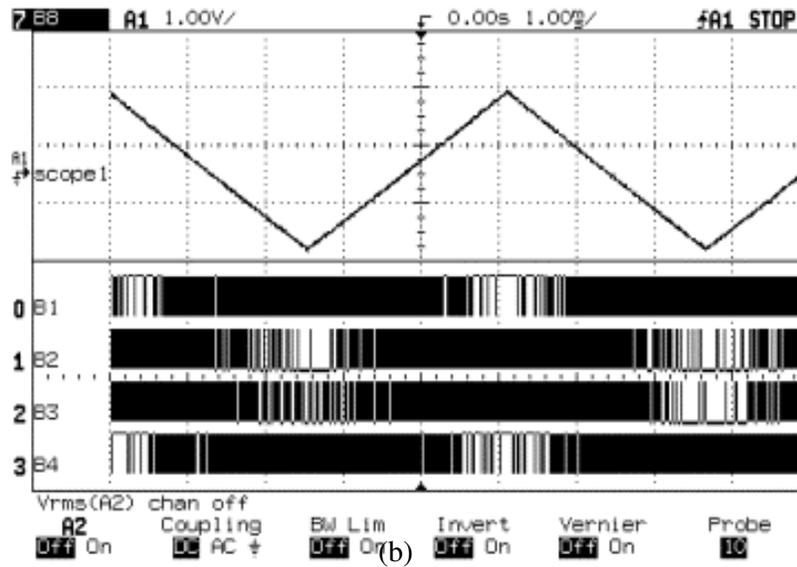


Figure 5.14: Four parallel comparators acquisition setup (a) two noise sources are turned into four using analog inverters, (b) acquisition uses digital channels of the HP54645D oscilloscope.

From the mapping relationship for Gaussian noise it is easy to note that a difference in the offset of each channel will lead to a shift in the y -axis for the output erf plots. For this reason it was assumed that the acquisition should take a previous self-calibrating stage in order to determine the channel offsets. This was easily accomplished by grounding the input signal v and proceeding with a first four-channel zero acquisition. Values thus determined were directly used to compensate the acquired values of each input on the operation stage. The output of each channel was afterwards added together to provide a resolution compatible with a single channel acquisition using four times more averages in the bit-stream. Figure 5.15 shows the acquired results.

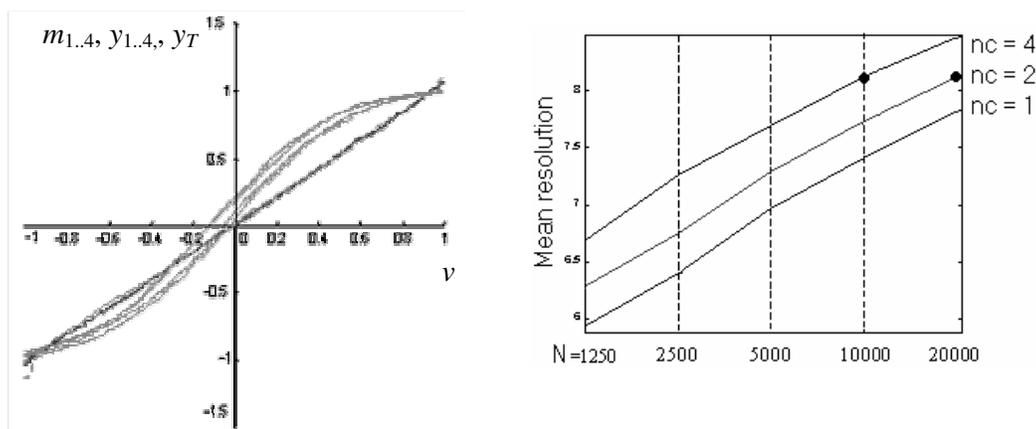


Figure 5.15: Four comparators acquisition. Each channel generates a different gray erf plot. After subtracting zero and using the linearization function Γ , one has four linear mappings of the input, that added together result the final output (in black). Output resolution matches the theoretical.

As the convergence to a given resolution r in this circuit is very slow and related to the averaging window N of the bit-stream ($r \propto \log_2 \sqrt{N}$), using several parallel comparators with different noise references allows a better dynamic performance of the acquisition ($r \propto \log_2 \sqrt{\beta \cdot N}$ for β parallel comparators). Figure 5.16 summarizes this tradeoff between parallelism and averaging in the total resolution for Gaussian noise acquisition (assuming that the quantization step equals the output scattering within two standard deviations).

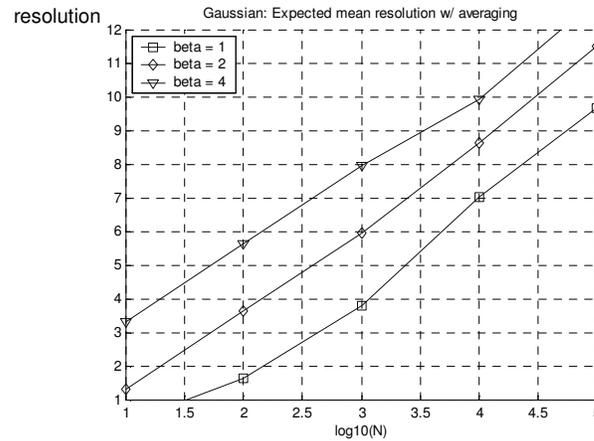


Figure 5.16: Resolution and number of comparators using Gaussian noise.

5.6.2 Using Adaptive Filtering to Improve SS-ADC Performance

A prototype of the analog acquisition system was designed. Analog blocks were assembled with standard discrete components. Four LM311 comparators performed the acquisition, and data was gathered using the digital channels of a HP54645 oscilloscope.

Reference used a pseudo-random generator. The digital control of the generator (including uniform sampling mapping for the hybrid approach) was described using VHDL and synthesized using EPLD prototyping boards. Reference sampling frequency was set to 200kHz. Each generator semi-cycle was divided into 256 time-slices ($L = 256$) selected through the lower bits of a 14-taps LFSR (Linear Feedback Shift Register) pseudo-random generator. Different γ s were generated using LFSRs with different seeds. In a similar fashion to which was done in section 5.6.1 these two pseudo-random signals were transformed into four with analog inversion in order to provide four parallel references. Uniformization functions (W_{HL} and W_{LH}) for both pseudo-random signals were fixed and also hard-coded in the generator VHDL.

Four sets of signals were acquired: one (1kHz) and two-tones (.9KHz and 1.1KHz) signals with a simple non-uniform generator and with a digitally uniformized generator (for the hybrid approach). Also, to configure the adaptive block a grounded input acquisition was performed using both kinds of generator. The results of the adaptive filter strategies using the acquired data are summarized in table 5.4.

Table 5.4: Adaptive filter approach result with acquired data

Measurement	Parameter variation (Δ)	
	<i>ENOB gain</i>	<i>SINAD gain</i>
1 - tone, simple	+3.0365	+18.2798
2 - tones, simple	+2.0594	+12.3978
1 - tone, hybrid	+3.7811	+22.7625

6 A COMPARISON WITH OTHER CONVERTERS

Beginning with the declared aim of applying a digital modeling and compensation approach to analog data acquisition this work has explored the possibilities of using different combinations of statistical sampler blocks with digital linearization methods. In the previous chapters, the principles behind the SS-ADC were explained and some practical measurements were performed. One important question still remains open: how does this approach perform when compared to other ADC architectures, and more important, is the proposed approach capable of taking better advantage of the Moore's Law than the others?

Two other architectures will be approached: the flash converter and the successive approximations converter. To proceed with this comparison, the statistical sampler and its parallel variations will be evaluated in terms of number of conversion cycles and total area for a given resolution. As the area parameter is subject to great variation with architectural choices, the impact of self-configuration, redundancy and cost of individual analog blocks will also be analyzed. Also, starting with these area considerations a projection of area cost trends will be made based on the ITRS Roadmap (ITRS, 2003).

6.1 Time and Resolution

The faster of the architectures is the flash ADC. Since it is a straightforward implementation that takes 2^{r-1} comparators for a resolution r , it will proceed with one conversion per cycle, and its conversion time will only be limited by the delay in the critical path of comparison + decoding (which is usually dominated by the switching speed in the comparators). In fact, the exponential cost of the flash architecture for higher resolutions implies that in most of the applications smaller resolution ADC are combined in some way. The most widely used of these setups is the pipelined-flash (which is sometimes referred as simply the pipelined ADC).

If one employs a pipelined-flash design, the conversion path is divided into several pipeline stages (n_p), each of these composed by a flash AD with smaller resolution (r_p), a DA converter, a sample and hold circuit and (for every stage after the first) signal amplification. In such circuits every acquisition takes n_p cycles for a total resolution of $r = n_p \times r_p$, however as up to n_p conversions can be performed at once, the total throughput reaches one conversion per cycle. The total conversion time is then defined by the slower of the pipeline stages. As with the pipeline full the DA operates in parallel with the AD, once again the usual limiting factor is the delay in the comparator blocks.

A successive approximations converter (also known as SAR-ADC, where SAR stands for Successive Approximation Register) uses a single comparator, sample and hold and a DA. The main idea is to proceed searching for the right digital value using a bisection algorithm. Beginning with half the total input range, at each cycle the reference to the AD is increased or decreased by half the preceding guess until the total resolution is achieved. The conversion process takes r cycles to reach resolution r . Total speed is limited by the path formed by the comparator delay plus the DA delay.

Usually the DA in the SAR-ADC is implemented through a capacitive C-2C circuit (BASU; LEE; MA, 1998; KANG; CHEN; CHUEH, 1989) - sometimes a resistive circuit is also employed - and its non-idealities are the main constraint imposed on the SAR converter performance. Capacitor mismatch leads to loss of acquisition linearity and even loss of monotonicity, thus must be avoided. Since this mismatch is typically inversely proportional to the unitary capacitor size this size can not be made arbitrarily small to increase acquisition speed. Also, this DA unit corresponds to most of the total converter area.

As an example a 10bits SAR-ADC implemented over $.35\mu\text{m}$ CMOS (BASU; LEE; MA, 1998), took 4mm^2 , of which 3.6mm^2 were taken only by the capacitors (interconnection wires not included) and presented a throughput of 10Msamples/s. In the same circuit the sole comparator employed was capable of working up to 200Msamples/s imposing a very small area penalty. Using the same architecture one can calculate that in the same technology for eight bits converter DA area would be around $900\mu\text{m}^2$. This area, in a conservative estimation, is enough to fit up to two hundred additional comparators plus their interconnection wire and a reference generator for a PSS-ADC ($27\mu\text{m}^2$) in the same technology. As a rough estimation, using $\beta=200$ and $N = 20$, one would match the same resolution and throughput. It is important to note that, although the high number of comparators may suggest that a flash architecture would also be feasible, that is not true since the flash architecture demands additional area for the reference ladder and additional analog procedures for mismatch control.

In the SS-ADC resolution depends logarithmically of the product between the averaging depth (N) and the number of comparators (β). One more time, the delay of a single cycle is determined by the operation of the comparators. Also, the averaging imposes latency on the acquisition, it acts like a filter process setting an upper limit to the input signal in a manner that resembles the operation of a sigma-delta converter. After the initial latency, the averaging window slides and assimilates a new transition each cycle. In the same situation, a sigma delta would have its total throughput decreased to accommodate the integration delay (for this reason sigma delta ADCs usually provide two different values for throughput: total throughput and effective multiplexed throughput). Figure 6.1 shows how to multiplex the input signal to a statistical sampler, in this situation the ADC throughput will only be divided between the quantity of analog input channels.

When compared to the other architectures, the SS-ADC takes the higher number of comparison cycles to begin with. As an example, a SAR converter with eight bits, would take only eight cycles to acquire any new input. To reach this resolution a SS-ADC with a single comparator would require at least $N=4.000$. After the initial latency a new value is generated at each cycle. The main advantage comes because it is possible to operate the SS-ADC at the typically higher digital switching speeds of comparator blocks, while SAR-ADCs are limited by the DA chain.

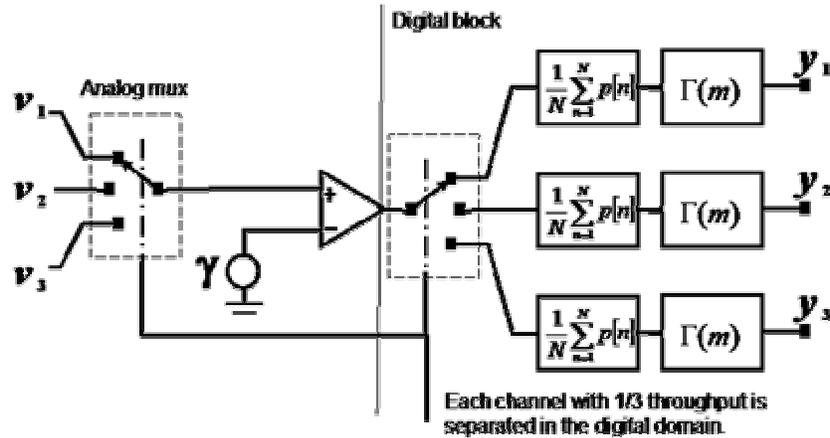


Figure 6.1: Using a single SS-ADC to acquire multiplexed inputs.

Comparing a flash ADC with a PSS-ADC, using eight comparators, in order to reach eight bits the flash ADC would take 255 comparators, or at least three stages with three bits each in a pipelined arrangement (normally more stages are used since some bits are reserved for fault prevention). In this situation, the total latency for the PSS-ADC would be of a thousand cycles against a total conversion time of three cycles for the pipelined-flash. In this situation the PSS is only at advantage if the simplicity of its architecture allows one to fit more parallel low cost comparators in the same total area of the flash ADC.

6.2 Area and Resolution

To compare the total area the architectures take it would be necessary first to determine the cost of the main blocks in each of the ADCs. This task is not very simple, since total area of these analog blocks varies widely depending on the features each designer adds to his project. As a simplification, table 6.1 summarizes the main factors that go in the cost composition for every one of the ADCs as a function of the target resolution. The table assumes one is using the pseudo-random reference generator in the PSS.

Table 6.1: Area and resolution for the ADC architectures

Architecture	Area composition
SAR	$A_{S\&H} + (2^{r-1}) \times A_{DA} + A_{comp}$
Flash	$(2^{r-1}) \times (A_{ref} + A_{comp})$
	$m \times (A_{S\&H} + (2^{r-1}) \times A_{DA} + 2^{r/m} \times A_{comp})$
PSS	$A_{gen} + \beta \times (A_{S\&H} + A_{comp})$

One notes that for $\beta=1$ the SS-ADC is clearly the smallest (in fact in this situation even the sample and hold circuits are not required). The above mentioned table is valid as a first approximation of the relationship between the areas taken by each application.

Using the same example of the former section: an eight bits converter implemented over .35 μm CMOS it is possible to estimate the total area taken by the three different architectures. Area of the Flash ADC was estimated based on Guilherme et al. (2001) and the area expressions listed in table 6.1. Data is summarized in table 6.2.

Table 6.2: Estimated area for an eight bits ADC on .35 μm CMOS

Architecture	Estimated area
SAR	$\sim 1\text{mm}^2$
Flash	$\sim 5\text{mm}^2$
PSS	$800\mu\text{m}^2\text{-}2\text{mm}^2$

In fact there is another important issue to take into account: the quality of the comparator required by each architecture is not the same. For instance, both SAR and Flash are very sensitive to variations in the comparator characteristics (SAR additionally is sensitive to variations in the DA block also), on the other hand the PSS bear easily variations in the comparator offset and in the generator distribution. Here it is important to remember the discussion on how to use redundancy together with self-configuration to increase the total system performance. Architectures that can not easily take advantage of such self-configuration based strategies will have increasingly higher difficulties to accommodate newer, more variable technologies.

7 FINAL REMARKS

7.1 Application Specific Analog Acquisition - ASAA

The main proposal of this work was to explore a possible path to define a highly digital applications specific analog acquisition (ASAA) design process. The long term goal is to define an environment where starting from a high level definition of the final application, one would be able to select the smallest acquisition architecture to fulfill the system requirements. Ideally such system would allow the designer to make a top-down specification of the application in terms of the application description and not low-level parameters such as resolution and bandwidth. At the same time the system would be able to build the total ADC architecture bottom-up, using the minimum available analog resources to fulfill the specified requirements.

The approach taken was based on statistical acquisition and digital compensation of non-idealities. The analog blocks should be small and capable to be implemented on digital technology, while feature variability issues would be dealt by using better digital compensation modules, self-configuration and redundancy. This would make possible to reduce the costs associated with the analog design flow, from specification and technology migration to prototyping and test.

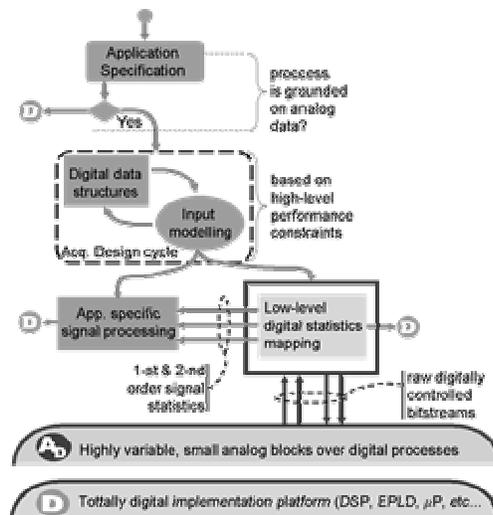


Figure 7.1: Proposed project flow for an application specific analog acquisition design process within mixed-signal systems.

Ideally, this system would be embedded as part of a mixed-signal design environment. Once it is detected that a high level description of the system relies on analog data, the ASAA design path (figure 7.1) is activated

An iterative process would allow the designer to separate the application specific input processing (such as spectral evaluation or analog array pattern identification algorithms) from the remaining digital processing blocks. Given the application and technology constraints, the palette of low-level digital statistics acquisition blocks would be defined. This step allows some simplifications in the digital modeling domain to have a positive influence by loosening the constraints in the ASAA block. A simple example of this would be any application where one seeks to define a spectral signature of a given input, as it was seen on chapter 2.

All the work in this research can be divided on three main axis: application, architectures and digital modeling. The latter two are the core of the research, the first of them was the stage when the minimum acquisition block was defined, characterized and tested, and the second when several algorithms and topologies were evaluated in order to make available a repertoire of composition strategies that the design environment could in the future use to build the applications. The application axis was developed simultaneously with the other two, and consists in the identification of the main applications that could benefit from the performed research.

7.2 Target Applications

Defining possible target applications for this approach and testing the performance of our acquisition techniques performing these applications is rather relevant in order to verify the generality of the statistical sampling based methodology as well as its particularities and limitations. Figure 7.2 shows the main applications targeted for the statistical acquisition of analog data.

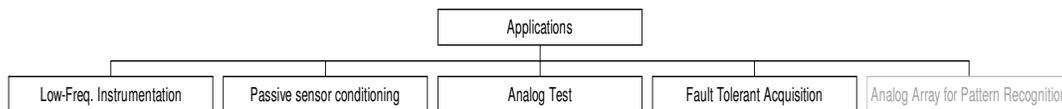


Figure 7.2: Main applications for the proposed system. The gray box in the extreme right marks an area of possible further developments.

7.2.1 Low Frequency Instrumentation

The statistical sampler is an over-sampled converter and thus it is particularly able to take advantage of the really high gaps between digital switching speeds and analog signal frequencies. This is exactly the case for many applications in low-frequency instrumentation, as it was shown in several works. In fact, higher frequencies can be achieved through redundant parallelism and a smart identification of particularities of the application specific processing involved in the design (SOUZA Jr.; CARRO, 2003-b; SOUZA Jr; CARRO, 2004-a; SOUZA Jr.; CARRO, 2004-c; MAINARDI et al., 2004).

7.2.2 Passive Sensors

A particular situation where higher frequencies can be achieved is when our signal of interest has a really narrow bandwidth centered in a well-known frequency. This is exactly the situation when we are dealing with passive sensor conditioning. As the device is responsible for the generation of the sensor stimulus it can use its well-known characteristics to tune the application specific DSP block, alleviating the requirements over the low pass linearization block. The tradeoff would be a larger latency on the

acquisition results (SCHÜLER; SOUZA Jr.; CARRO, 2004; SOUZA Jr.; CARRO, 2004-b; SOUZA Jr.; CARRO, 2004-c).

7.2.3 Analog Test

Analog test in the context of this work is a subdivision of the passive sensors problem. In fact our approach to analog test uses a multilevel random signal as stimulus and a set of spectral based parameters as signature. It is thus able to work under conditions where the relationship between the acquired spectra and the analog signal one does not need to be linear. In fact, besides this “oversampled” situation, good results were also obtained using a random signal with a much lower bandwidth than the signal frequency (NEGREIROS et al., 2003; NEGREIROS; CARRO; SUSIN, 2004). It was shown that this approach allows low-cost digital signature circuits to be built (SOUZA Jr. CARRO, 2003-a). As it will be seen in the digital modeling section, a full understanding of this later situation is a possible future issue for research.

7.2.4 Fault-Tolerant Acquisition

A property of the parallel architectures of the statistical sampler is the redundancy between each data channel. This redundancy together with the self-configuration and the built-in stimulus generator allows the system to be resilient to multiple failures scenarios without the need of additional replication of blocks. In fact the PSS presents a very interesting ability to show graceful performance degradation, such as catastrophic faults in the input comparators impact only in the total resolution to bandwidth ratio allowing the system to remain at work (SOUZA Jr.; CARRO, 2004-d; SOUZA Jr.; CARRO, 2005-a).

7.2.5 Pattern Processing in Embedded Analog Data Arrays

Many embedded applications that use analog input arrays, rely on massively parallel DSP models to process pattern identification and classification. Since this models many times are rather resilient to small non-linearity’s the statistical sampler could be employed with minimum ASAA cost. Linearization blocks, for instance, may be unnecessary or not be very demanding. Moreover the low cost of any single statistical sampler would allow multiple parallel inputs to be acquired, while the resulting bit-streams can be used directly to feed low-cost stochastic arithmetic processing blocks. This line of applications was not yet pursued in the scope of this thesis, remaining an open issue for future developments.

7.3 Hardware Features and Architectures

Another important set of problems involves the hardware considerations behind the acquisition blocks. Figure 7.3 shows the main architectural issues and the sub-sections further detail each issue.

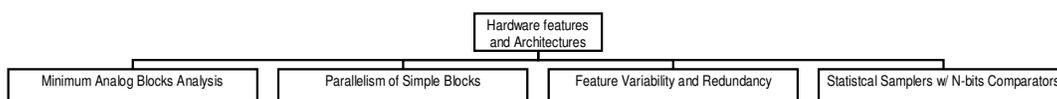


Figure 7.3: Hardware blocks and feature variation issues.

7.3.1 Analysis of the Elementary Blocks

The first set of problems was to define the smallest possible set of acquisition blocks. This comprised the analysis of non-ideal issues in the comparator and generator blocks and the comparison with alternative all-digital devices (MAINARDI et al., 2004; SOUZA Jr.; CARRO, 2004-b).

7.3.2 Parallelism and Reconstruction Models

To allow a perfect combination of the outputs of several parallel low-cost comparators (PSS) several non-ideal hardware issues (like offsets and slew rate) must be dealt with. The main problem is to define the best way to combine the outputs of several comparators. If our noise is not uniform and there is a high variability in the offsets of the inputs the reliability of each channel is not the same over the whole dynamic range of the input. A domain restriction and weighting technique, as well as some self-configuration procedures were developed with lead to some improvement on the resulting output characteristics (SOUZA Jr; CARRO, 2004-a; SOUZA Jr; CARRO, 2004-d; SOUZA Jr; CARRO, 2005-b).

7.3.3 Redundancy and Self-Configuration and the Area/Frequency Tradeoff

Previous work for Flash ADCs performed by Flynn was able to show that using several low area comparators and selecting the best ones using a self-configuration stage allowed the designer to improve the digital converter performance without area penalty. From the basic work on feature variation (PELGROM; DUINMAIJER; WELBER, 1989) one knows that to guarantee a low parameter variation for analog blocks designed over standard digital CMOS the designer must add extra area or analog components. This means that, it is sometimes better to design several smaller comparators with higher feature variations and select the best ones. The main idea here was to test whether this proposition holds true for the massively parallel statistical sampler architecture. Future research should allow one to determine the number of redundant comparators required for any give technology.

7.3.4 Defining a Complete Path Using Statistical Samplers with more than One Bit

The idea here was to use the statistical sampling approach with high amplitude noise references and low cost converters (in this case the comparison elements or CEs) with more than one bit (GPSS). It was shown that a variable amount of improvement in resolution can be achieved this way. However, total improvement has an asymptotic characteristic and the idea does not scale up very well. Also, it was possible to show that the additional parallelism have a high cost in total linearity of the acquisition. Digital linearization can be employed, with a consequent lower resolution at the fringes of the input range. A research paper is being written with the results found from this analysis and will be submitted to a design conference in the near future.

7.4 Modeling Techniques

To allow the use of the statistical sampler it was necessary to determine how one could digitally compensate the non-ideal characteristics of the statistics acquisition process. Three different techniques were employed: (i) linearization using the knowledge of the statistic properties of the noise used in the sampler; (ii) statistic

generator control and; (iii) adaptive filtering to improve resolution using different topologies.

The first two techniques were rather successful and are fully described in this thesis proposal. In the total, the filtering approach was tested in two situations and employing four different architectures.

1. An attempt to improve the output of an unusual statistical sample setup (which is sometimes employed in analog test applications), where the noise has a much lower bandwidth than the signal and one is interested in acquiring this signal, was performed with a non-linear adaptive filtering topology without success. Every other attempt to use adaptive filtering was performed on the traditional “oversampled” SS-ADC;
2. A self-correlation adaptive filter was employed with success to increase the effective number of bits of a statistical sampler without any linearization block ($\Gamma(m)$). The main drawback was that, although resolution improved, the filter was unable to cope with higher degrees of non-linearity in the acquisition;
3. Exactly to deal with these situations where non-linearity was too big, an hybrid approach was proposed using a variation of the method of generator uniformization (using the function $W(i)$). In this case, however, a simple function $W(i)$, without self-configuration stage was employed. After the acquisition the averaged signal m , non-idealities were dealt by the same adaptive topology used in the issue 2.
4. Also another modeling approach where the output sampling sequence i was adaptively controlled to match an ideal model was tested, but it had to be abandoned once the adaptive filter architectures selected were not able to converge in the SS-ADC operational conditions.

Besides these architectures, a noise generator with statistical feedback loop architecture was also proposed and remains as a possible future development. Figure 7.4 gives an overall view of the work on digital modeling techniques.

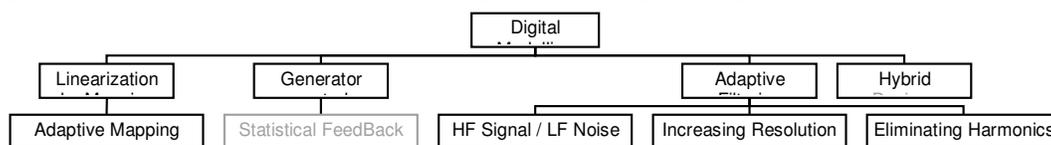


Figure 7.4: Digital modeling techniques: The gray box shows possible future research.

7.5 Original Contributions

During the course of this thesis research several contributions were made. Among those were implementations, analysis and original proposals. Results of this research originated eleven papers published on international events, plus two others published on national events. Also final results were submitted in two international journals.

A non-exhaustive list of contributions (some of them presented in the current volume, some only in the papers) would include:

- Implementation of a sigma-delta modulator using a modified ASE/ACE reinforcement learning algorithm.

- Low cost DFT (Discrete Fourier Transform) block for bitstream signals applied to signature identification on Analog Test.
- Full analysis of the statistical acquisition using non-uniform references and its linearization.
- Full analysis of the pseudo-random generator.
- Analysis of the feasibility of compensation with non-linear adaptive filters of statistical samplers with reference bandwidth much lower than the input frequency.
- A domain restriction method to combine the outputs of multiple parallel statistical samplers when the references γ are not centered in zero and very distant from each other.
- A method to keep track of model variation when using the pseudo-random generator and automatically update the linearization model.
- A linearization method using the stochastic control of the generator and the full hardware implementation of it.
- The design of a complete fault tolerant PSS architecture with the algorithms for fault-tracking and recovery.
- Use of adaptive filtering with generator uniformization to improve ENOB in a SS-ADC.
- Proposal and analysis of the GPSS architecture and its limitations.

While the work now concluded is not enough yet to fully specify an ASAA automated design environment, hopes are that it pointed important directions. In the next section some considerations are made regarding some open issues and possibilities for future research.

7.6 Open Research Issues

As it was previously discussed there are three axis in which this work has been developed simultaneously: application, architectures and digital models. Future developments were already suggested in for two of these lines of research (applications and modeling):

- Some applications of the SS-ADC for mixed signal that employ some sort of multi-input pattern recognition. An example would be sensor arrays for digital scent sensors (e-nose), or movement tracking;
- The work to find a good method to model and extract periodic signals in statistical samplers when the signal frequency is much higher than the reference bandwidth is still an open issue. During the development of this thesis, some linear and non-linear adaptive filter structures were tested, with no success. An alternative approach would be the use of methods for the extraction of almost stationary signals in the line of those proposed by Dandawaté and Giannakis (1994), or perhaps a predictive model based on the extraction of causal states (SHALIZI; SHALIZI; CRUTCHFIELD, 2003);
- Also the linearization using uniformization of the reference generator, lets open the possibility of statistically controlling the reference switching to further improve the convergence of the SS-ADC to an expected resolution.

Other interesting possibilities are in the axis of architectures. Given the already established core ideas behind the statistic acquisition of analog signals and the SS-ADC architecture one still relies on two elementary analog blocks: the comparator and the reference source. The developed tools should allow one to use really low cost elements and even so attain circuits with a well known and reliable behavior. One can take one step further and exchange the blocks for even smaller non-linear ones. Instead of low-cost comparators taking twenty transistors, one could use a simple arrangement of CMOS inverters, like the one proposed by Tangel (1999). In this situation, the required level of redundancy will have to be much higher and the design will be stochastic in its essence, but at the same time the resilience and capability to cope with more variable technologies will increase too. The author believes that the stochastic quantization framework will be fundamental in such scenario.

REFERENCES

- ANDÒ, B.; GRAZIANI, S. CNNs for noise generation in dithered transducers. INSTRUMENTATION AND MEASUREMENT TECHNICAL CONFERENCE, 2000. **Proceedings...** Baltimore: [s.n.], 2000. p. 1071-1076.
- ANTIC, B. M.; NARANDZIC, M. Bitwise random number generator improvement of stochastic A/D conversion. In: MIDWEST SYMPOSIUM ON CIRCUITS AND SYSTEMS, 42., 1999. **Proceedings...** Las Cruces: [s.n.], 1999. v.1, p.198–200.
- AUMALA, O. **Dithering in Analog-to-Digital Conversion**. 2001. 46 f. Dissertation (Doctor of Technology) – Tampere University of Technology, Tampere, Finland.
- BASU, A.; LEE, V.; MA, A. **A 10-bit 10MS/s SAR ADC**. 6th. Design Contest Application - EECS598 Analog to Digital Converters. University of Michigan. Fall - 2002. Available at: http://www.eecs.umich.edu/~mpflynn/Design_Contest/Fall2002. Visited on: 10 March, 2005.
- BENNET, W. R. Spectra of Quantized Signals. **Bell Systems Technical Journal**, [S.l.], v.27, p. 446–472, July 1948.
- BENDAT, J. S. **Nonlinear Systems Techniques and Applications**. New York: Wiley, 1998.
- BERMAK, A. A CMOS imager with PFM/PWM based analog-to-digital converter. In: IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS – ISCAS, 2002. **Proceedings...** Scottsdale: IEEE, 2002. v. 4, p. 53-56.
- CHAPEAU-BLONDEAU, F.; GODIVIER, X. Theory of stochastic resonance in signal transmission by static nonlinear systems. **Physical Review E**, New York, v. 55, n. 2, p.1478–1495, Feb. 1997.
- CARRO, L. et al. Circuit Level Considerations for Mixed-Signal Programmable Components. **IEEE Design and Test of Computers**, Los Alamitos, p. 76-84, Jan./Feb., 2003.
- CAWEMBERGHS, G. A Nonlinear Noise-Shaping Delta-sigma Modulator with On-Chip Reinforcement Learning. **Analog Integrated Circuits and Signal Processing**, [S.l.], v. 18, 1999.
- CICHOCKI, A.; UNBEHAUEN, R.; Switched-capacitor Selfoscillating Capacitance Transducers with Duty-cycle or Digital output. In: EUROPEAN CONFERENCE ON CIRCUIT THEORY AND DESIGN, 1989. **Proceedings...** [S.l.: s.n.], 1989. p. 185–189.

CVETKOVIC, Z.; VETTERLI, M. On Simple Oversampled A/D Conversion in L2(IR). **IEEE Transactions on Information Theory**, New York, v.1, n. 47, p. 146-154, 2001.

DANDAWATÉ, A. V.; GIANNAKIS, G. B. Extraction of Almost Periodic Signals Using Cyclostationarity. In: IEEE INTERNATIONAL CONFERENCE ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING - ICASSP, 1994. **Proceedings...** Piscataway: IEEE, 1994. v. 4, p.141-144.

FLORES, M. G. C. et al. A Noise Generator for Analog-to-Digital Converter Testing. In: IEEE SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEM DESIGN – SBCCI, 2002. **Proceedings...** Porto Alegre: UFRGS, 2002. p. 135-140.

FLORES, M. G. C. et al. Towards a Low cost BIST for RF Mixers. In: INTERNATIONAL MIXED-SIGNAL TESTING WORKSHOP – IMSTW, 9., 2003. **Proceedings...** Sevilla: [s.n.], 2003. v. 1, p.73 – 78.

FLYNN, M.P.; BOGUE, I. Using Redundancy to Break the Link Between Accuracy and speed in an ADC. IEEE INSTRUMENTATION AND MEASUREMENT TECHNOLOGY CONFERENCE – IMTC, 2003. **Proceedings...** Vail: IEEE, 2003. p. 850-853.

FLYNN, M.P.; DONOVAN, C.; SATLER, L. Digital Calibration Incorporating Redundancy of Flash ADCs. **IEEE Transactions on Circuits And Systems—II: Analog And Digital Signal Processing**, [S.l.], v. 50, n. 5, p. 205- 212, May 2003.

GIELEN, G. G. E.; RUTENBAR, R. A. Computer-Aided Design of Analog and Mixed-Signal Integrated Circuits. **Proceedings of the IEEE**, New York, v. 88, n. 12, p. 1825-1852, Dec. 2000.

GRAY, R. M.; STOCKHAM Jr, T. G. Dithered quantizers. **IEEE Transactions on Information Theory**, New York, v.38, n. 3, p. 805-812, May 1993.

GROSHONG, R. RUSCAK, S. Undersampling techniques simplify digital radio. **Electronic Design**, [S.l.], v. 39, n. 10, p. 67-78, May 1991.

GUILHERME, J. et al. Design Considerations for High Resolution Pipeline ADCs in Digital CMOS Technology. In: IEEE INTERNATIONAL CONFERENCE ON ELECTRONICS, CIRCUITS AND SYSTEMS – ICECS, 8., 2001. **Proceedings...** Malta: IEEE, 2001. p. 497-500.

HOLMAN, W., T.; CONNELLY, J. A.; DOWLATABADI, A. B.. An Integrated Analog/Digital Random Noise Source. **IEEE Transactions on Circuits and Systems – I Fundamental Theory and Applications**, New York, v. 44, n. 6, p. 521-528, June 1997.

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS – SYSTEM DRIVERS, ITRS, 2003. **Proceedings...** Available at: <http://public.itrs.net>. Visited on: 10 March, 2005.

JACOMET, M. et al. On the Dynamic Behavior of a Novel Digital-Only Sigma-Delta A/D Converter. In: IEEE SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEM DESIGN , SBCCI, 17., 2004. **Proceedings...** Porto de Galinhas: IEEE, 2004. p. 222-227.

- JERRI, A. J. The Shannon sampling theorem - Its various extensions and applications: A tutorial review. **Proceedings of the IEEE**, New York, v. 65, p. 1565-1596, Nov. 1977.
- KANG, C.-K.; CHEN, J.-Y.; CHUEH, J.-Y. **A 10-bit 10MHz Samples/s 5mW Successive approximation Register A/D converter**. 6th. Design Contest Application - EECS598 Analog to Digital Converters. University of Michigan. Fall - 2002. Available at: http://www.eecs.umich.edu/~mpflynn/Design_Contest/Fall2002>. Visited on: 10, March, 2005.
- KESTER, W. Undersampling Applications. In: KESTER, W. **Practical Analog Design Techniques**. Norwood: Analog Devices, Inc., 1995.
- KUNDERT, K. et al. Design of mixed-signal systems-on-a-chip. **IEEE Transactions on CAD**, New York, v.9, n.12, p. 1561-1571, Dec. 2000.
- KUNDERT, K. A Formal Top-Down Design Process for Mixed-Signal Circuits. In: KUNDERT K. **The Designer's Guide to Verilog-AMS**. [S.l.: s.n.], 2004.
- LOFTI, R. et al. A Low-Power Design Methodology for High-Resolution Pipelined Analog-to-Digital Converters. In: INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN - ISLPED, 2003. **Proceedings...** Seul: ACM/SIGDA, 2003. p. 334-339.
- LU, C.; LEMKIN, M.; BOSER, B.E. A Monolithic Surface Micromachined Accelerometer with Digital Output. **IEEE Journal of Solid- State Circuits**, New York, v.30, n.12, p. 1367 -1373, Dec. 1995.
- MAINARDI, J.O.; SOUZA JR. A. A. et al. A Comparison of Totally Digital ADCs for SoCs. In: IEEE INTERNATIONAL SYMPOSIUM ON SYSTEMS AND CIRCUITS, ISCAS, 2004. **Proceedings...** Vancouver: IEEE, 2004.
- MEDEIRO, F. et al. A Vertically-Integrated Tool for Automated Design of $\Sigma\Delta$ Modulators. **IEEE Journal of Solid-State Circuits**, New York, v. 30, p. 762-772, July 1995.
- NEGREIROS, M.; CARRO, L.; SUSIN, A. A. A Statistical Sampler for a New On-line Analog Test Method. In: IEEE INTERNATIONAL ON-LINE TESTING WORKSHOP, IOLTW, 8., 2002. **Proceedings...** Bendor: IEEE, 2002. p.79-83.
- NEGREIROS, M.; SCHULER, E.; CARRO, L.; SUSIN, A. A. Testing RF signal paths using spectral analysis and subsampling. In: IEEE SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN, SBCCI, 16., 2003. **Proceedings...** São Paulo: IEEE, 2003. p. 329-334.
- NEGREIROS, M.; CARRO, L.; SUZIM, A. A. Low Cost Analog Test of RF Signal Paths. In: DESIGN, AUTOMATION AND TEST IN EUROPE, DATE, 2004. **Proceedings...** Paris: EDA, 2004. p. 292-297.
- NYQUIST, H. Certain topics in telegraph transmission theory. **Transactions of the AIEE**, New York, 1928.

KWON, O.-B. et al. A novel double slope analog-to-digital converter for a high-quality 640x480 CMOS imaging system. In: INTERNATIONAL CONFERENCE ON VLSI AND CAD- ICVC, 6., 1999. **Proceedings...** Seul: IEEE, 1999. p. 335-339.

PAPOULIS, A. **Probability, Random Variables and Stochastic Processes**. 3rd ed. [S.l.]: McGraw-Hill, 1991.

PARK, J. et al. A 1mW 10-bit 500KSPS SAR A/D Converter. In: IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, ISCAS, 2000. **Proceedings...** Geneva: IEEE, 2000,

PELGROM, M. J. M. ; DUINMAIJER, A.C. J.; WELBERS A. P. G. Matching Properties of MOS transistors. **IEEE Solid State Circuits**, New York, v. 24, p. 1433-1440, Oct. 1989.

RICE, R. A useful theorem for nonlinear devices having Gaussian inputs. **IRE Transactions on Information Theory**, New York, 1958.

RITONIEMI, T.; KAREMA, T.; TENHUNEN, H. Design of Stable High Order 1-bit Sigma-delta Modulators. In: IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, ISCAS, 1990. **Proceedings...** New Orleans: IEEE, 1990. v.4, p. 3267-3270.

SARPESHKAR, R.; HERRERA, R.; YANG, H. A current-mode spike-based overrange-subrange analog-to-digital converter. In: IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, ISCAS, 2000. **Proceedings...** Geneva: IEEE, 2000. v. 4, p. 397-400.

SCHÜLER, E.; SOUZA JUNIOR A. A.; CARRO, L. Parallel Statistical Sampler For Low Frequency Instrumentation. CONGRESSO BRASILEIRO DE AUTOMÁTICA, CBA, 5., 2004, Gramado. **Anais...** Gramado: UFRGS, 2004. 1 CD-ROM.

SHALIZI, C.; SHALIZI, K.; CRUTCHFIELD, J. P. An Algorithm for Pattern Discovery in Time Series. **Journal of Machine Learning Research**, [S.l.], 2003.

SMITH, T.; HUIJSING, J.H. An Integrated Linear Position Sensitive Detector with Digital Output. INTERNATIONAL CONFERENCE ON SOLID-STATE SENSORS AND ACTUATORS , TRANSDUCERS, 1991. **Digest of Papers...** [S.l.: s.n.], 1991. p. 719-722.

SOUZA JUNIOR, A. A.; CARRO, L. Aprendizado por Reforço em Interfaces Analógico-digitais. In: SIMPOSIO BRASILEIRO DE AUTOMAÇÃO INTELIGENTE – SBAI, 5., 2001. **Anais...** Canela: UFRGS, 2001. 1 CD-ROM.

SOUZA JUNIOR, A. A., et al. Complex Adaptive Signal Processing for Analog Testing, In: IEEE LATIN AMERICAN TEST WORKSHOP – LATW, 3., 2002. **Digest of Papers...** Montevideo: IEEE, 2002. v.1, p.166-173.

SOUZA JUNIOR, A. A.; CARRO, L. A DFT Macrocell for DigitalTest of Analog Blocks. In: IEEE LATIN AMERICAN TEST WORKSHOP, LATW, 4., 2003. **Digest of Papers...** Natal: IEEE, 2003-a. p. 217-222.

SOUZA JUNIOR, A. A.; CARRO, L. An All-Digital ADC for Instrumentation within SoC's. In: IFIP INTERNATIONAL CONFERENCE ON VERY LARGE SCALE

INTEGRATION, VLSI/SoC, 2003. **Proceedings...** Darmstadt: IFIP, 2003-b. p. 398-403.

SOUZA JUNIOR, A. A.; CARRO, L. Highly Digital, Low-Cost Design of Statistic Signal Acquisition in SoCs. In: DESIGN AUTOMATION AND TEST IN EUROPE , DATE, DESIGNER'S FORUM, 2004. **Proceedings...** Paris: EDA, 2004-a. v. 3, p. 10-15.

SOUZA JUNIOR, A. A.; CARRO, L. Amostragem Estatística Não-uniforme e Modelagem Não-linear no Projeto de ADC's em Processos Digitais. In: WORKSHOP IBERCHIP, 10., 2004. **Proceedings...** Cartagena de Índias: Iberchip, 2004-b. 1 CD-ROM.

SOUZA JUNIOR, A. A.; CARRO, L. Statistical Acquisition for Embedded Instrumentation. In: IEEE INSTRUMENTATION AND MEASUREMENT TECHNOLOGY CONFERENCE, IMTC, 21., 2004. **Proceedings...** Como: IEEE, 2004-c. v.1, p.314- 317.

SOUZA JUNIOR, A. A.; CARRO, L. Robust Low-Cost Analog Signal Acquisition with Self-test Capabilities. In: IEEE INTERNATIONAL SYMPOSIUM ON DEFECT AND FAULT TOLERANCE IN VLSI SYSTEMS, IMTC, 19., 2004. **Proceedings...** Cannes: IEEE, 2004-d. p. 239-247.

SOUZA JUNIOR, A.A.; CARRO, L. Self-test in a Stochastic Analog-to-Digital Converter, In: IEEE LATIN-AMERICAN TEST WORKSHOP, LATW, 6., 2005. **Digest of Papers...** Salvador: IEEE, 2005-a.

SOUZA JUNIOR, A.A., TOUSAAD, J.; CARRO, L. Adaptive Processing Applied to the Design of Highly Digital Analog Interfaces. In: IEEE INTERNATIONAL SYMPOSIUM ON SYSTEMS AND CIRCUITS, ISCAS, 20., 2005. **Proceedings...** Kobe: IEEE, 2005-b.

TANGEL, A. **VLSI Implementation of the Threshold Inverter Quantization (TIQ) Technique for CMOS Flash A/D Converter Applications.** 1999. 65f. Dissertation (PhD degree), The Pennsylvania State University, Pennsylvania, USA.

TAPANG, G.; SALOMA, C. Dynamic-range enhancement of an optimized 1-bit A/D converter. **IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing**, New York, v. 49, n.1, p.42-47, Jan. 2002.

TEMES, G. C.; CANDY, J. C. A Tutorial Discussion of the Oversampling Method for A/D and D/A Conversion. In: IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, ISCAS, 1990. **Proceedings...** New Orleans: IEEE, 1990. v. 2, p. 910-913.

VUJICIC, V. V. et al. Low Frequency Stochastic True RMS Instrument. **IEEE Transactions on Instrumentation and Measurement**, New York, v.48, n.2, Apr. 1999.

WALDEN, R. H. Analog-to-Digital Converter Survey and Analisis. **IEEE Journal of Selected Areas in Communications**, New York, v. 17. n. 4, p. 539-550, Apr. 1999.

WANNAMAKER, R. A. et al. A Theory of Nonsubtractive Dither. **IEEE Transactions on Signal Processing**, New York, v. 48, n. 2, p.499-516, Feb. 2000.

- WANNAMAKER, R.A.; LIPSHITZ, S. P.; VANDERKOOY, J.; "Stochastic resonance as dithering". **Phys. Rev. E**, New York, v. 61, n. 1, p. 233–236, Jan. 2000.
- WANNAMAKER, R. A. **The Theory of Dithered Quantization**. 2003. 135f. Dissertation (PhD degree), Univ. Waterloo, Waterloo, Canadá.
- WATANABE, T.; MIZUNO, T.; MAKINO, Y. A 14-bit 12 μ V/LSB resolution A/D converter for sensors using only digital circuit with low-pass filter effect. In: IEEE INTERNATIONAL CONFERENCE ON ELECTRONICS, CIRCUITS AND SYSTEMS, ICECS, 8., 2001. **Proceedings...** Malta: IEEE, 2001. v.2, p. 677-680.
- WIDROW, B.; KOLLÁR, I.; LIU, M.-C. Statistical theory of quantization. **IEEE Transactions on Instrumentation and Measurement**, New York, v. 45, p. 389–396, June 1996.
- WOLFFENBUTTEL, R. F.; KURNIAWAN, W. Stochastic analog-to-digital converter based on the asynchronous sampling of a reference triangle. **IEEE Transactions on Instrumentation and Measurement**, New York, v. 38, n.1, p. 10–16, Feb. 1989.
- YAMADA, M. et al. Switched-Capacitor Interface for Capacitive Pressure Sensors. **IEEE Transactions on Instrumentation and Measurement**, New York, v.41, n.1, p.81-86, Feb. 1992.
- YOO, J; CHOI, K.; LEE, D. Comparator Generation and Selection for Highly Linear CMOS Flash Analog-to-Digital Converter. In: IEEE INTERNATIONAL SYMPOSIUM ON QUALITY ELECTRONIC DESIGN, ISQED, 2002. **Proceedings...** San José: IEEE, 2002. p. 138-142.
- ZORIAN, Y.; MARINISSEN, E. J. System Chip Test - How Will It Impact Your Design. In: DESIGN AUTOMATION CONFERENCE, DAC, 37., 2000. **Proceedings...** Los Angeles: SIGDA/EDA/IEEE, 2000. p136-141.

APPENDIX RESUMO DA TESE EM PORTUGUÊS

Uma Abordagem Digital para o Projeto de Aquisição Estatística de Dados Analógicos em Sistemas Integrados (SoCs)

O interfaceamento entre os domínios analógico e digital, dentro do contexto dos sistemas integrados híbridos (Mixed-signal SoC's) é hoje um tópico de grande investigação. É muito provável que a diferença atualmente existente entre velocidades de processamento digital e frequências de aquisição dos conversores A/D disponíveis não venha a diminuir no futuro. De fato, tudo indica que, para requisitos de preço compatíveis a atual diferença venha a aumentar. Existem duas razões para a persistência dessa tendência são duas: as melhores tecnologias de integração digitais estão sempre uma ou duas gerações à frente das analógicas, e as tecnologias digitais de estado da arte possuem variações de processo intrínsecas que representam um grande desafio para projetistas analógicos.

Neste trabalho, o projeto de conversores A/D é abordado no contexto de sistemas híbridos. Nestes sistemas as tecnologias de integração existentes, os procedimentos preexistentes para desenvolvimento e teste de projetos, assim como os recursos computacionais disponíveis podem desempenhar um papel preeminente na redução impacto em custo de qualquer arquitetura de conversor A/D escolhida (CARRO et al., 2003). Na verdade, desenvolvimentos futuros em conversores A/D irão requerer que muitos recursos de projeto, atualmente apenas disponíveis para o projeto dos blocos digitais, sejam estendidos para lidar também com a aquisição de dados analógicos.

Partindo desse objetivo primordial: tornar o problema de projeto de conversores A/D em um problema de modelagem digital de sistemas é necessário verificar se tal abordagem cobre as principais questões que cercam o problema da aquisição de sinais analógicos em sistemas híbridos. A solução proposta emprega blocos analógicos muito pequenos e de baixo custo, para então, usando redundância, autocalibração e compensação digital atender aos requisitos de projeto dados pela aplicação especificada. Deste modo, os desafios de projeto de conversor A/D em sistemas altamente integrados nas tecnologias futuras podem ser tratados:

- Questões de tecnologia: a taxa mais lenta de melhoria dos blocos analógicos é contornada definindo-se uma arquitetura quase completamente digital, e que é capaz de tirar proveito das mais altas frequências de chaveamento que estas apresentam; a autocalibração digital, junto com a possibilidade de usar blocos analógicos altamente variáveis (e, portanto de baixo custo) é definida como procedimento padrão para lidar com as grandes variações paramétricas das novas tecnologias. Ao mesmo tempo, o baixo custo dos blocos analógicos mínimos permite redundância maciça e uma maior

tolerância aos erros que serão mais frequentes devido às baixas tensões de alimentação futuras.

- Questões de projeto: assumindo que o bloco analógico mínimo seja realmente pequeno, pode-se construir o sistema de baixo para cima, permitindo que se alcance um custo mínimo para cada dado conjunto de requisitos; isso, por sua vez, torna possível um projeto de aquisição analógica mais orientado a aplicação. Ao mesmo tempo, uma vez que blocos analógicos exigentes não são necessários, a estrutura final poderá ser facilmente arranjada em estruturas configuráveis (como matrizes analógicas configuráveis), uma característica que tornará a prototipação analógica muito mais fácil.
- Questões de confiabilidade: as mesmas características tornam a redundância mais barata, o que, juntamente com a autocalibração e o processamento digital pode ser usado para permitir a tolerância à falhas múltiplas e uma degradação graciosa do desempenho, também reduzindo os custos de teste do sistema.

Para ser possível que se atendam todos os itens acima a primeira grande questão a responder é qual o mínimo bloco analógico a ser usado. O capítulo dois revisa algumas das principais arquiteturas para conversores A/D que empregam blocos analógicos de baixo custo e processamento digital adicional. Neste capítulo também se explica o modelo de bloco escolhido: o amostrador estatístico compensado digitalmente (digitally compensated statistical sampler). O mesmo capítulo também explica como a modelagem digital é utilizada em conjunto com esta arquitetura e como desse modo, é possível transferir complexidade de projeto analógico para o domínio digital.

A geração de múltiplas referências não correlacionadas para a aquisição estatística é um item importante para o desenvolvimento de arquiteturas mais complexas e por esta razão é discutida em detalhes no capítulo três. O capítulo quatro aborda algumas aplicações práticas dessas idéias ao mesmo tempo que introduz uma forma de linearização alternativa: a linearização através do controle da distribuição de amostragem na referência.

A segunda grande questão é se é possível usar esse bloco básico como elemento de construção para arquiteturas mais exigentes. Isso envolve a necessidade de determinar os limites de desempenho dessa abordagem de conversão estatística de sinais analógicos. No capítulo cinco se buscam as respostas para essa questão, resumindo-se as diversas estratégias de melhoria de desempenho que foram estudadas. Estas estratégias incluem o uso de conversores estatísticos paralelos redundantes (PSS), o uso de elementos discretizadores de mais de um bit (GPSS) e o emprego de filtragem adaptativa do sinal lido. O objetivo desse capítulo é fornecer um conjunto de ferramentas que permita ao projetista escolher entre os muitos compromissos para melhor ajustar o bloco de aquisição analógica a uma dada aplicação.

A última questão a responder é como essa estratégia de projeto se compara a outras soluções usuais de projeto de conversor A/D para as mesmas aplicações. Para responder essa pergunta, uma comparação de área analógica entre os conversores gerados pela estratégia proposta e duas outras arquiteturas comuns (SAR e Flash) é realizada e apresentada no capítulo seis.

No capítulo sete, é fornecido um rascunho do fluxo de projeto total proposto, além de se resumir as principais contribuições feitas ao longo dessa pesquisa e se apontar novas possibilidades a explorar dentro da mesma linha de pesquisa.