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Mixed-Signal Analog-Digital Circuits Design on the Pre-Diffused Digital Array Using Trapezoidal Association of Transistors

by

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List of Abbreviations

ADC / DAC	-	Analog-to-Digital Converter / Digital-to-Analog Converter
A/D / D/A	-	Analog/Digital / Digital/Analog
AMP_S	-	Full-custom Amplifier (Single transistors)
AMP_T	-	SOT Amplifier (TAT transistors)
ASIC	-	Application Specific Integrated Circuits
CAD	-	Computer Aided Design
CMFB	-	Common mode feedback
cond.	-	conduction
CurS	-	Current mirror source
CS	-	Common-source
DC / AC	-	Large and Small signal
DECT	-	Digital Enhance Cordless Telecommunications
DIBL	-	Drain Induced Barrier Lowering
DR	-	Dynamic range
eff	-	effective
eq	-	equivalent
estim	-	estimation
FPGA	-	Field Programmable Gate Array
FET / N_FET	-	Field Effect Transistor / N type FET
GBW	-	Gain-Bandwidth
GSM	-	Groupe Spécial Mobile
IC	-	Integrated Circuit
LD	-	Lateral diffusion
max / min	-	maximum / minimum
max-swing	-	maximum signal swing
meas	-	measurement
MOS / CMOS	-	Metal Oxide Silicon / Complementary MOS
nom	-	nominal
OTA	-	Operational Transconductance Amplifier
out-swing	-	output signal swing
OSR	-	Oversampling Ratio
P & NMOS	-	P / N type MOS
SAT / sat.	-	saturation
sim	-	simulation
SC	-	Switched-capacitor
SD	-	Sigma-Delta
SNR	-	Signal-to-Noise Ratio
SOG	-	Sea-Of-Gates
SOT	-	Sea-Of-Transistors
SR	-	Slew-Rate
TAT	-	Trapezoidal Association of Transistors
THD	-	Total Harmonic Distortion
VLSI / ULSI	-	Very / Ultra Large Scale Integration

List of Symbols

V_{DD} / V_{SS}	-	Supply voltages
L / W	-	Channel Length / Width
D / G / S / B	-	Drain / Gate / Source / Bulk
g_o	-	Output transconductance
MD / MS	-	Upper / Bottom transistors composing a TAT
L_u / W_u	-	Channel length / width of unit transistor
$(W/L)_u$	-	W/L ratio of unit transistor
I_D	-	Drain current
ND / NS	-	Number of unit transistors of upper / bottom transistor
Nu	-	ND or NS
X	-	MD or MS
x	-	X-axis
C_{GS}	-	Gate-to-Source capacitance
C_{GD}	-	Gate-to-Drain capacitance
C_{GB}	-	Gate-to-Bulk capacitance
C_L	-	Load capacitance
m	-	ND/NS ratio
I_F / I_R	-	Forward / Reverse current
V_{TO} / V_T	-	Threshold voltage: at $V_S = 0V$ / $V_S > 0V$
V_P	-	Pinch-off voltage
V_D / V_G / V_S	-	Drain, Gate and Source voltage
V_{CH}	-	Channel voltage
I_S	-	Specific current ($=2n\beta U_T^2$)
$\hat{a}$	-	Transconductance factor ($= \frac{W}{L} \cdot m \cdot C_{ox}$)
U_T	-	Thermodynamic potential
μ / μ_0	-	Carrier mobility / Surface mobility
$\tilde{a}$	-	Body effect factor
$Ø_0$	-	Bulk Fermi potential
q	-	= 1.602×10^{-19}C electron charge
T	-	Absolute temperature (in degrees *Kelvin*)
k	-	Boltzman constant
C_{ox}	-	Oxide capacitance
n	-	Slope factor
á	-	angle
f	-	Frequency
f_s / T_s	-	Sampling frequency / Period
t_s	-	Settling time
md / *nl*	-	Drain width time-step / Number of series transistors
V_m	-	TAT middle node voltage
S	-	W/L ratio
V_E	-	Early voltage
λ	-	Channel modulation factor
g_m	-	Transconductance
1/f	-	Flicker noise
Kf	-	Flicker noise coefficient
f_k	-	Flicker noise corner frequency

Abstract

The mixed-signal and analog design on a pre-diffused array is a challenging task, given that the digital array is a linear matrix arrangement of minimum-length transistors. To surmount this drawback a specific discipline for designing analog circuits over such array is required. An important novel technique proposed is the use of TAT (Trapezoidal Associations of Transistors) composite transistors on the semi-custom Sea-Of-Transistors (SOT) array. The analysis and advantages of TAT arrangement are extensively analyzed and demonstrated, with simulation and measurement comparisons to equivalent single transistors. Basic analog cells were also designed as well in full-custom and TAT versions in 1.0µm and 0.5µm digital CMOS technologies. Most of the circuits were prototyped in full-custom and TAT-based on pre-diffused SOT arrays. An innovative demonstration of the TAT technique is shown with the design and implementation of a mixed-signal analog system, i. e., a fully differential 2^{nd} order Sigma-Delta Analog-to-Digital (A/D) modulator, fabricated in both full-custom and SOT array methodologies in 0.5µm CMOS technology from MOSIS foundry. Three test-chips were designed and fabricated in 0.5µm. Two of them are IC chips containing the full-custom and SOT array versions of a 2^{nd}-Order Sigma-Delta A/D modulator. The third IC contains a transistors-structure (TAT and single) and analog cells placed side-by-side, block components (Comparator and Folded-cascode OTA) of the Sigma-Delta modulator.

Keywords: VLSI, CMOS analog design, Physical implementation, SOT array, TAT transistors, Analog cells, Sigma-Delta converters.

1 Introduction

1.1 Motivation

The perspectives of increasing demand for sophisticated electronic products have created higher competition in the market. As the result, industries are permanently incorporating advanced characteristics in their products. Since the invention of Integrated Circuits (IC's) hundreds of thousands of miniaturized equipments and machines were designed, which still are getting increasingly advanced thanks to the VLSI (Very Large-Scale Integration) and ULSI (Ultra Large-Scale Integration) technologies. Moreover, providing advantages in cost, reliability and performance to the system, as the degree of integration increases.

The wireless communication equipments are everywhere [ALI94], [COU94], [YAM94] and became now an important part of our lives. The use of battery-driven mobile equipment with communication functions has expanded rapidly in recent years as cellular telephones, personal digital assistants (PDA's), and laptop and palmtop computers are widely used. Such devices have helped to establish an "anytime, anywhere, and with anyone" communication style, and have driven the diffusion of multimedia services throughout modern society.

From process to high-level design CAD tools and techniques, digital area is advancing rapidly at constantly decreasing cost. There is a number of advanced digital CAD (Computer-Aided Design) tools available for countless applications. Digital technologies are largely available on dozens of foundries at very low cost. Larger and more complex systems are integrated into small silicon area at higher speed, lower power and higher reliability. Nevertheless, the design time turn-around from specification to the product is critical and

essential to the industries survival, since consumers and their competitors still are claiming high quality and advanced products.

Contrarily to the digital counterpart, analog design is almost “the art of hand-made”. It cannot use the same digital design tools and methods. Analog CAD tools and special technologies are still costly and there is a lack of good and readily available MOSFET models. In any communication systems, there are embedded analog circuits as front-end of the whole system, interfacing digital and analog world. In a competitive market, time is the key to success. Nonetheless, the bottleneck of modern electronic products is the analog design. Today, most digital systems design time for systems with about 100K gates takes about few weeks. On the other hand, analog systems with around 100 transistors can take months of design time to converge to an acceptable performance.

Another major and essential concern for battery-driven mobile equipment is the power consumption due to battery lifetime, weight and compactness. The heat generated inside an IC is unwanted and must be controlled and minimized, even for non-portable systems. For digital systems, there is a good body of research, many techniques and design methodologies to reduce the power consumption. There are different abstraction levels for design methodologies that must be considered, such as: system, functional, architectural, logic, electrical and layout levels. The main techniques are the reduction of circuit activity, operating frequency, switching capacitances and supply voltages. Contrary to digital designs, for which decreasing the power supply (V_{DD}) voltage contributes to power consumption reduction, lowering V_{DD} is not beneficial to analog performance. Lower supply voltages for the analog circuits do not mean less power consumption; on the contrary, it causes several problems, such as: signal-to-noise ratio and performance degradations [VIT94a], [ENZ96b].

It is a commonly accepted view that the role of analog in future VLSI circuits and systems will be confined to that of an interface. That is, the very thin “analog shell” between the fully analog outer world and the fully digital core of the growing signal processing in wireless communications. The main advantage of all-digital computation is its cheap and potentially unlimited precision and dynamic range, due to the systematic regeneration of the binary states at every processing step.

As already pointed out, other advantages are the cheap and easy design and test of the circuits. Digital circuits are designed by computer scientists working with advanced synthesis tools to implement specific or programmable algorithms. Therefore, the task of analog

designers will be essentially concentrated on developing good performance interfaces. The goal for this interface is to translate as early as possible all information into numbers (with increasing demand on precision and with higher level of exposure to digital noise in the chip environment) and to bring the results of the all-digital computations back to the analog world.

The research work in the author's Master thesis [CHO94] was on this analog-digital border, where the design and a comparative analysis of the A/D (analog-to-digital) converters were performed, searching for the one with the better performance. In this process, several analog circuits have been designed and validated by electrical level simulations. A number of Sigma-Delta A/D modulator architectures have also been designed and investigated as well, due to their practical importance.

Furthermore, electronic industries can use pre-diffused gate arrays at least for the ASICs (Application-Specific Integrated Circuit) systems with the purpose of decreasing design and fabrication turnaround time, from specification to the product. Advantages of using semi-custom design approach are that it allows high level of design abstraction, holding back the steps of layout design time, offering high quality and performance at very low cost, short time-to-market and short prototyping time. The cost, performance and design time are also the main concerns for analog systems. Using the advantages of semi-custom in the analog design seems to be worthy of study. On the other hand, pre-diffused semi-custom arrays are not appropriate for analog applications. A fair amount of research was developed, but none of them was able to address all the designers needs, and the industry and market requirements.

In this context, a rapid response from industries and universities and new chip design methodologies are required. The universities are not responsible only for human resources development, but need also to work in partnership with industries to offer innovative products and novel design techniques and tools.

1.2 Objective

The objective of this work is to present an innovative principle, which is applicable to analog designs on semi-custom arrays in a deeply scaled digital CMOS technologies. A particular building block – a Trapezoidal Association of Transistors (TAT) of minimum-length – is proposed to leverage the benefits of good analog performance by using digital, uniformly sized, unit transistors on the Sea-of-Transistors (SOT) array [AIT96b], [CHO99a], [CHO99b], [CHO2000a]. This work compares two different strategies: fully customized place & route of transistors versus a semi-custom layout strategy of regularly placed (linear matrix) transistors. The latter are used to design the analog modules using the so-called trapezoidal association of transistors. The focus is a design case study, which can be handy to a wide range of analog and mixed-signal systems.

The problem of designing analog building blocks – current mirrors, comparators, common-source amplifiers and operational transconductance amplifiers – in a SOT digital array is addressed in this work. Moreover, this work goes as far as exemplifying and comparing implementations of the OTAs and Sigma-Delta modulators, which may find many applications in analog/digital interfaces. The approach demonstrated herein deals with the issues of poor analog performance of digital technology, minimum-L transistors. The layout step of this approach is regular, can be more automated, and more insensitive to the greater statistical variations present in any fabrication process. Additionally, power consumption is a concern. The difficulties involving low voltage operation of analog circuits are tackled indirectly. The ways out and the suitability of SOT array to deal with low-voltage applications, aiming adaptability to the deep sub-micron technologies are the focus of the TAT technique.

The idea of the TAT technique can be extended to any design or application that requires an acceptable level of analog performance instead of the best performance (in current sources, voltage references, comparators, amplifiers, etc.) in a mixed-signal environment, for which digital CMOS technology is unavoidably the implementation alternative.

This text begins with a discussion of several problems arise in with analog semi-custom designs and power consumption in the modern ASIC systems. The principle of TAT transistor is extensively investigated and contrasted to its equivalent single transistor,

supported by electrical simulations and experimental measurements carried out in a number of test-chip samples.

The same procedure and analysis are also carried out for common-source amplifier, comparator and OTA (Operational Transconductance Amplifier) to show the applicability and advantages of using TAT transistors. As a final point, a mixed-signal system implemented in both methodologies, full-custom and SOT array, is proposed and investigated. This A/D system is part of multi-standard Second-order Sigma-Delta modulator for wireless communication systems as described in chapter 6.

The conclusions are supported by both simulations and silicon data, measured in silicon for all building blocks addressed. Several test vehicles, comprised of chips in both 1.0µm and 0.5µm digital CMOS, were fabricated. Experimental tests that provide several comparisons of SOT array methodology versus Full-custom methodology were extensively done. It is worth to point out that, among others MOSFET models ([CUN96], [GAL96], [JES95]), TAT modeling and analysis herein assessed is based on the EKV model [ENZ89]. All electrical simulation results are done in the HSpice electrical simulator.

1.3 Text Organization

In chapter 2, the topics of this work are presented and put in prospective. The statement of the problem, regarding analog and mixed design on semi-custom arrays, is presented. Moreover, why it should be solved and references to and comments upon relevant research by other authors on the same or similar problems are addressed. The proposed ideas, solutions and experiments contributed by this work follow in chapter 2.

In chapter 3 the SOT array is quickly reviewed. The TAT technique is introduced and, aiming its better understanding, first a trapezoidal FET is briefly described. Then, in chapter 4, the TAT transistor array is extensively evaluated, investigated and experimentally compared in the same chip to the equivalent single transistors, supported by electrical simulations and measurements, accomplished in transistor structures designed into test-chips.

Large (DC) and small (AC) signal modeling and noise performance investigations are also carried out.

The chapter 5 is dedicated to basic analog cells and circuits design, as well as presenting electrical simulations and measurements, using TAT transistors on SOT array compared to their equivalent full-custom implementation.

In chapter 6 the design of a system by means of the previous technique is put forward. A 2^{nd}-order Sigma-Delta analog-to-digital converter on SOT digital array with the purpose of validating TAT technique is implemented and experimentally tested using semi-custom array methodology.

2 Discussion of Analog Semi-Custom Design Issues and Solutions

This chapter focuses on discussing the problems involved in the field of analog design and circuit implementation on pre-diffused digital gate arrays, which motivated this work. Ideas and solutions are proposed that challenge many analog VLSI designers.

2.1 The Problems

In the last decades, CMOS technology was extensively used and spread over the world by its well-known advantages in cost, performance and low power operation. The reasons for its dominance are its robustness and high density. Nowadays, portable and wireless system equipments are pervasive and are becoming a major trend in the market by their importance to the modern society. Wireless communication systems are driving electronic industries to develop high quality products. Consequently, extra functions are required and merging services is a necessity. For example cellular phones, GPS, video-conference, internet access, agenda, and similar functions on a single device. This trend is pushing research towards VLSI/ULSI technologies since cost and power consumption becomes an essential design target because of portability and short battery lifetime. Industries must put forward not only higher quality products but bring them fast into competitive markets.

To facilitate faster VLSI/ULSI integrated circuits design, industries are using pre-diffused arrays, such as gate arrays, SOGs (Sea-Of-Gates), SOTs and FPGAs (Field Programmable Gate Array), which are good alternative to decrease the design turn-around time and prototyping time. The semi-custom arrays are a good compromise/trade-off between design time and performance. Field programmable analog arrays are still very limited in scope

and performance, so that mask-programmable SOT is the best option for high degree of digital integration. The speed and silicon area is often smaller and larger, respectively, than its equivalent full-custom version. The design proceeds mostly at a high level of abstraction and the remaining steps are automated (partitioning, placement and routing), using pre-defined cells and IP (Intellectual Property) blocks from the pre-defined libraries.

High packing density in large VLSI ICs is also a main concern. There is the enormous power consumption per unit area, where the heat generated may not be a negligible factor. An efficient way to reduce power consumption in digital circuits is by decreasing supply voltage (V_{DD}) [CHA92], [SHI93], [LIU93], [RAB94], [PIG95], [RAB96]. The reason is that the average power consumption in digital-only systems is directly proportional to the square of V_{DD}. However, the overall system performance (gates delay, clocking frequency, etc) decreases, which can be minimized by introducing more parallelism and/or modifying technology process and optimizing the operation at lower V_{DD} [MAC96]. Lowering V_{DD} is necessary to keep electrical field constant at the oxide gate in the technology scaling [TAU97]. Traditionally, CMOS technology has been known to be relatively slow and to consume very low power. Nowadays, this has changed: deep sub-micron CMOS is no longer a slow technology. Unfortunately, the power consumption in complex systems like microprocessors is approaching highest unacceptable levels.

The advantages of digital signal processing are also well known, however the world is analog and front-end communication interfaces, between the real world and digital environment, are still greatly required. These interfaces frequently require basic building blocks known as analog cells or systems, which are the main component blocks for the Analog-to-Digital and Digital-to-Analog converters (ADC and DAC). However, available digital technologies are not well appropriate for analog applications, and specialized analog technologies are still costly alternative and mixing analog-digital circuits can be prohibitive.

A number of performance issues arise when implementing an analog circuit in the technology and environment that is traditionally dedicated to digital applications. The noise, DC and AC performances of MOSFETs are poor compared to bipolar devices. Mixed-signal or analog-digital systems placed side-by-side on the same silicon suffer from crosstalks and increased switching noise levels. In addition, MOSFET models from the digital CMOS foundries do not reflect real behavior of these devices. Even in dedicated analog process, analog design is not straightforward. The design difficulty increases in the digital technology

environment. Analog IC design demands careful physical design, better device modeling and new design techniques. It demands improvements on CAD tools that reflect more accurately the linear and non-linear behavior of the devices, accounting also for RF effects. Hence, the same digital rules can not be applied to analog circuits.

In analog circuits, power performance is mainly dictated by the expected signal-to-noise ratio (SNR) and operating frequency [VIT94a], [MAT94]. Consequently, for mixed-signal systems, as supply voltages (V_{DD}) of the digital part are required to be reduced, the analog part must also operate at lower V_{DD} for device reliability due to technology scaling. This is a severe constraint for power consumption, AC and noise performance. As IC process geometries continue to scale down, supply voltages must often follow to ensure reliable device operation. Unfortunately, as the supply voltage is reduced, the threshold voltage does not necessarily scale proportionally. In fact, some sub-micron processes have threshold voltages as high as 0.8V. With such high threshold voltages, it is difficult to design high performance analog circuits, such as cascaded amplifiers using this standard high-V_T CMOS technology.

While digital circuits can take full advantage of shorter device lengths in modern CMOS technologies, low noise analog circuits are usually constrained by short channel effects and *1/f* noise effects [MIK82], [REI84], [TSI88]. These effects often impose the design of MOSFETs with gate lengths much longer than the minimum design dimension allowed by the specific technology. Digital circuits, by nature, do not suffer significantly under low voltage conditions and can perform their functions with slight modifications, while low voltage analog techniques are much different from design techniques of analog cells that operate with a relatively high supply voltage (those in which V_{DD} is 5 to 20 times larger than the transistor threshold voltages).

In a digital design, lowering the supply voltage will always imply low power consumption whereas in analog design it not always represent a power reduction, for the same SNR specified for the analog block. This is because lowering the supply may or may not reduce power depending on whether certain design changes are made to maintain or restore the analog performance at acceptable levels. In many of the existing low voltage design strategies, such design changes are often made to the DC part of the circuit and this may lead to larger power consumption than it is originally anticipated.

In the technology scaling, the supply voltage is scaled by the scaling factor k (k>1), the transconductance and capacitances are multiple of k^2 [VIT94b]. The signal-to-noise ratio (SNR) and the gain-bandwidth product (GBW) do not change because SNR is directly proportional to the square of supply voltage and to the capacitance, and GBW is directly proportional to the transconductance and inversely proportional to the capacitance. The result is that the SNR and GBW are, to first order, unchanged in the technology scaling. Nonetheless, power consumption is increased k times because the total current is increased k^2 times in order to maintain the SNR and GBW.

Another issue is the robustness of the analog circuits. Depending on the application and necessity, hundreds of thousand or millions of IC's are fabricated and still are very difficult to guarantee non-failure or to predict percentage of failures. In digital systems, there are several ways and techniques to test the IC's that can be performed at a pre-design (Design For Testability – DFT) and at pos-fabrication (ex. ATE – Automatic Test Equipment, etc…) [ABR90]. These test-systems are well suited for digital systems and currently there is a concern and several techniques for analog systems. The testing procedure concept for analog is the same from digital systems, regardless that in analog circuits there is a distinction between testing functionality and testing for characterization. As all these testing techniques require additional block-testing and/or test procedures after fabrication, the final cost is still high and performance degradation can take place in analog systems.

In order to guarantee high functional yield in the production and high reliability of analog integrated circuits, the design of such circuits must be robust with respect to random process and device parameter variations. This is particularly true when analog and mixed analog-digital VLSI circuits operate from a low supply voltage (3V and below) [HUI85], [SAK96], . Since random variations do not scale down with feature size or supply voltage, the need for robust analog design is higher as scaling proceeds. Therefore, such variations could ultimately be a limiting factor on how low with the supply voltage can be operated in analog design and how reliable sub-micron designs could be.

The reasons stated above bring more rigorous design requirements to the designers and force analog designers to reconsider and redesign existing analog circuits. This should result in the development of innovative low voltage and/or low power and/or new analog design methodology.

2.2 The Semi-Custom Methodology

The fabrication of ICs is a long and costly process. It typically involves over 1,000 elementary steps, of which between 10 and 20 are associated with a photolithographic mask. To produce and sell circuits at an acceptable price, IC producers have long relied on a high level of standardization. Indeed, by making circuits that meet the needs of large markets (such as microprocessors, memories, pre-fabricated arrays like FPGAs, standard I/O interfaces, etc), industries have been able to produce mass quantities and hence lower prices.

However, the demand for ASICs has been growing for many years. Since these circuits are to be produced in small or medium quantity, their prices are potentially higher than that of standard circuits. The concept of semi-custom fabrication has been developed to overcome this problem. The main advantages of a semi-custom design methodology are the cost-effectiveness and the shorter fabrication time (turn-around time). IC production cost can be divided in two parts. First, the cost of the masks is shared among all customers and applications. Second, the gate array (wafer processed up to post-polisilicon oxide deposition) is produced in large quantities and the per-unit cost is lowered.

Since metallization steps are the same as equivalent steps in a full-custom process, no cost reduction can be expected during the custom phase. Nevertheless, the cost of a process can be roughly estimated by the number of masks involved. Under this condition, it is clear that the cost of a semi-custom process (few metallization masks) is lower than the cost of a full-custom process (several masks). Engineering costs are not dependent on the process nature, but rather on the level of expertise of the designer, the specifications, and the quality of available CAD tools and designs methodologies. The common design methodology used on semi-custom arrays is a cell-based design, similar to standard cells. The cost in both cases is the same, and much lower than those in full-custom designs.

The turn-around time is drastically reduced because the gate arrays are produced in advance and are stored ready to be fabricated. The time needed for making the metallization masks and processing the corresponding fabrication steps. Moreover, metallization step is on the average faster to process then standard steps because they do not require any diffusion or annealing. Only oxide or aluminum deposition and associated photolithography, etching and planarization by CMP are the required fabrication steps. Typically, although full-custom

fabrication requires several weeks, a semi-custom process may take few days. This advantage can be decisive in applications where time-to-market is crucial for commercial success or just for prototyping.

Semi-custom gate arrays have still three other important advantages. First, a cell-based design methodology guarantees a greater degree of independence from the underlying process. In fact, when a new technology generation is introduced, most of the maintenance work is done by the cell library designer, usually the array manufacturer itself, to update the library (models and layout). Scaling of the cells can be automated and designer's schematics do not need to be modified [REA84]. Second, since gate arrays are produced in large quantities, they can be produced in large batch runs, allowing a better control over process characteristics and a better regularity in circuit parameters. Lastly, for foundries that produce full-custom as well as semi-custom circuits, gate array production can fill some gaps between full-custom processes, thus increasing the productivity of the foundry [DUC91].

Using cell libraries instead of designing at the transistor level has advantages and disadvantages. Among the advantages, it is worthy emphasizing that:

- eases the designer from problems associated with working at the lowest level of the design;
- eases the designer from dealing with process and technology dependent details, such as design rules, electrical behavior, etc…;
- provides some technology and process independence, since technology-dependent parameters are kept in the library (layout, models) and are not directly visible to the library user. If a customer wishes to move to a new process generation, he simply needs to select a new library and to re-simulate the design. In most cases, no changes are needed in the schematics.

Nonetheless, there are limitations in this type of methodology, which are the limitation in design flexibility, area increase and limitation in design complexity, reduction in performance and limitation in the volume of production. Moreover, the designer has no access to the individual transistor, functional possibilities are restricted to the functions offered by the cell library and finally, cell library development and maintenance represent important costs to the foundry.

The gate array contains devices whose place, size and shape are pre-determined and cannot be changed. This strongly limits the degree of freedom of the designer, who can only choose how those devices are interconnected. This limitation is obviously implied by the semi-custom nature of the circuit. The second limitation comes from the cell-based methodology. When constrained to work with a cell library, the designer has no access to the individual device, but only to an upper level. The main consequence is that some functions can simply not be realized (such as analog circuits), or must be realized with existing cell libraries, not necessarily suited to the designer's needs (which may include memories, parallel multipliers, etc).

Due to some reasons, a given function normally requires more devices in a semi-custom design than in full-custom. Additionally, in classical semi-custom methodologies, channels (area without any functional transistor use) are used for routing the connections. Circuit area is thus larger. This contributes to an increase of production costs, and lowers the yield. For that reason, the complexity that semi-custom methodologies can handle is significantly smaller than for full-custom. The lack of device sizing also has a significant impact on circuit performance (power consumption, speed).

Usually, all transistors have the same size in the semi-custom array. As the result, optimization – such as increasing the size of transistors that drive high currents and reducing others – is not possible or is limited to the assemblage of several transistors in parallel in order to increase their size. Nevertheless, even this is not possible if cell libraries are used. Furthermore, the higher area implies that connection wires are, on the average, longer than in full-custom. Obviously, associated parasitic capacitances are higher as well, and this again contributes to reducing performance.

Due to these limitations, the fabrication of very large quantities of semi-custom circuits is economically unjustified. Thus, semi-custom arrays are restricted to low- or medium-volume production of moderate high performance and complexity digital circuits. However, the latest advancement in process technology and the dramatic progress made in array architectures and CAD tools are moving the limit of technical and economical choices to the advantage of semi-custom arrays.

The usual design flow of a digital semi-custom circuit initiates with schematic capture and simulation, the customer sends the netlist to the factory. It is usually the role of the manufacturer to run the placement and routing tools and generate the complete layout of the

metallization steps. Optionally, he can feed back a netlist annotated with parasitic elements due to the physical realization of interconnections (capacitance and resistance). The customer may then re-simulate the annotated netlist to check if circuit specifications are still met. The schematics can be changed if necessary. If the design is accepted, the factory then produces the masks and metallization of the array. Testing may be at the factory or by the customer.

2.3 Analog Design on Semi-Custom Array

Analog circuits must be considered apart, for the reason that they have fundamentally different requirements than digital circuits: non-minimum size transistors, resistances and capacitances may need particular design, etc. Consequently, digital semi-custom arrays usually do not support analog circuits. However, the demands exist. Physical phenomena are analog in nature, and since ASICs are frequently used in peripherals and in interface circuits, system designers are faced with analog signals.

A number of previous works [HAS88], [DUC89], [DUC93], [DON94], [HAA96] demonstrated several techniques to overcome analog semi-custom design. In order to allow implementation of analog circuits in digital pre-diffused arrays, a number of solutions have been proposed such as: pure analog array; digital array with embedded analog circuits; digital array with embedded analog core; and analog circuits realized on a digital gate array.

Full analog arrays are usually implemented in bipolar technology. They contain bipolar devices, diodes, resistors and capacitances. Unfortunately, the complexity is limited and mixed analog-digital processing is not achievable. A second solution is to include standard analog circuits on a digital array, for example OTA, comparator, oscillator, A/D or D/A converter. This is the translation to the analog world of the embedded arrays found on digital gate arrays. It suffers from the same previous advantages and limitations. The main drawback can be the performance unsuitability of pre-diffused circuits to the needs of a particular application. For example, if the circuit application requires a low-noise, low-offset operational amplifier, while the available embedded amplifier is a fast but noisy one, the applicability of analog circuits on the semi-custom array may not be acceptable.

Some companies have proposed a more general solution, where the gate array contains two cores. One dedicated to analog applications, while the other is a conventional digital gate array. The analog core contains devices suited to analog requirements – non-minimum length MOS transistors, bipolar transistors, resistances, and capacitors – and the layout design finished by the usual metallization step. Of course, this is more suitable to BiCMOS (Bipolar CMOS) technologies.

While all these gate arrays may provide adequate performance for analog applications, due to their high cost and mixing analog-digital in the same piece of silicon, they are not the most cost effective. A conventional digital semi-custom can be used for analog implementation advantageously in comparison to the previous solutions, and to investigate this alternative this Ph.D. work was carried out.

2.4 The Ideas and Solutions

For convenience, repeating and emphasizing the characteristics of semi-custom design approach, the advantages of the pre-diffused gate array methodologies are well known. It allows fast system prototyping, as the front-end process steps are fabricated well ahead of the prototyping phase. Currently, the system performance in gate arrays is following the performance envelope of full-custom methodology. Its lowest cost combined with fast design turn-around time made gate arrays a viable implementation choice since the early 1980's.

In many IC designs, specially for digital circuits, problems such as transistor sizing and layout design (positioning and routing) are abstracted, leaving the IC design performed at system level. It leads to the design automation and to the pre-defined and characterized cells and gates, accessible in libraries. Additionally, as the technology scales down to deep sub-micron features, below 0.1μm, the down scalability and reusability (reusable IP's) of the cells, gates and systems are indispensable feature and strongly required for design cost trimming.

The array itself and cells/gates library can be fast and easily upgraded (or downscaled) to the new technology, that is, the technology is also abstracted from a system level design or leaving it to the pre-characterization phase. Such tasks also can be accomplished automatically with the technology mapping. Moreover, layout is not performed manually, i.

e., it is also automated and only the metallization steps are needed. The problems involved in the low level (speed, delay, sizing, etc) are left to the all pre-characterization. This task is done prior to the design itself. Any cells and gates are already designed and characterized. Hence, a priori, all cells/gates are available and known to be reliable. Furthermore, fast and easy technology migration is another foremost advantage, allowing that all library and arrays are ready to be reused in the new technology.

Now visualize, for instance, analog and mixed-signal circuits workability and achievability in the pre-diffused gate array are true, with all the previous features and advantages. The implementation of an analog circuit on semi-custom gate arrays is enormously facilitated. Analog design time is quite shortened and a large amount of layout design step is automated, pre-fabricated and stored. Additionally, technology is easily upgradeable, IC's rapidly prototyped, analog cells/subcircuits are freely accessed in libraries already existent and largely available digital CAD tools can be used for analog design.

Moreover, the matching is reasonably improved since sea-of-gates array is physically arranged by unitary transistors over linear matrix, naturally leading to the possibility of employment of the specific layout matching technique that is largely applied in analog layouts. The interdigitizing technique can be mostly employed [ALE97], [ISM94], [TSI96], which is also a common-centroid geometry technique – large pairs of transistors are partitioned into several fingers and interdigitized, which improves the matching. As well as it minimizes parasitic capacitances, resistances and lateral reverse diode effect [GRO67] by reducing source and drain area/perimeter and sharing drain-source terminals.

In the previous section the importance of robustness of analog circuit designs was pointed out, in view of random process and device parameter variations. In fact, currently this feature is also an important design concern and due to the higher ratio performance/cost of the testability techniques, robust design becomes a quite good alternative. As semi-custom gate array has well known problems due to the minimum geometry of transistor and, since naturally the transistors are partitioned, the robustness is relatively improved and better than in a full-custom methodology. All poor parameters can be extracted and characterized prior to the design itself and can be avoided and/or minimized before fabrication.

Evidently, all these features are, in theory, ideally perfect. Some characteristics are not feasible. For example, transistor sizing is still required by the designer and IP reusability and

technology downscaling are not straightforward, in contrast to the digital counterpart, and a more difficult technology migration is required.

There is a need for research work to improve and to develop new techniques to be employed and included into existing technologies. One of them is the pre-diffused semi-custom SOT methodology, which is very appropriate for digital ASIC systems. The SOT array is an arrangement of unitary digital transistors over an active region in a linear matrix style (described in chapter 3).

This style of semi-custom design methodology is cheap and allows fast IC fabrication since all of transistors are pre-defined, -characterized and set regularly on a linear array. Just a metallization process is later required to terminate the IC fabrication. As the SOT array is composed by transistors with minimum channel length, it can not be applied directly in analog applications, unless a special technique is exploited. Whether an analog system is feasible to be implemented in a semi-custom array, all advantages described previously will be helpful and valuable for the analog-digital applications. It is a good alternative of combining analog and digital systems side-by-side on a same piece of silicon, that leads to mixed-signal system integration in a same chip.

Once possible, there are numerous returns. For example: rapid prototyping, low cost, scalability and easy technology migration. The main return of analog SOT arrays are the fast design time turn-around, that is the time from specification to the IC prototype is considerably reduced. Analog semi-custom SOT approach allows the utilization of ordinary digital technologies, since it is largely available in any foundry at very low cost. The main disadvantage is that digital technology is not well suited for analog circuits and it gets worse in an environment traditionally for digital applications. The matching of the transistor modeling and the real behavior is insufficient when using digital models. The electrical models from the foundries are appropriate for digital applications and do not reproduce the real MOS device behavior for analog circuits. The MOSFET behavior characteristic is clarified in the chapter 4, where comparison analysis are put together for comparison purposes, with the results from HSpice electrical simulator and experimental tests.

The use of pre-diffused arrays for analog applications has been reported in the literature [HAS88], [DUC89], [DUC93], [DON94], [HAA96]. The solutions proposed by them are not reasonable to provide the requirements for analog circuits on digital semi-custom arrays. The main idea of those approaches is emulating a single transistor with an equivalent

association of fixed-size transistors, i. e., a composite transistor (similar to the technique proposed here).

A composite transistor is an arrangement of a "rectangular" shape of an in-series and in-parallel association of digital transistors with no restriction in the number of transistors in-series, which can be reduced or increased when required for a smaller or larger channel length, respectively. This approach does not present adequate performance for a wide range of modern analog applications. Low voltage operation is not feasible and voltage swing is poor due to the several transistors in-series, that hinders proper AC signal excursion required for normal operation. The emulation of a long channel length by series arrangement is a challenging task [DUC89]. The body effect is another characteristic that can affect the overall performance of the series association of transistors. Moreover, this technique has no improvement aggregated to it. The overall device matching is kept (dependent on area), however the effect on output conductance is not as good as expected.

To surmount the described drawbacks and to make possible the implementation of analog circuits on the pre-diffused digital SOT array, a special technique has to be developed. The innovative principle of Trapezoidal Association of Transistors (TAT) has been put forward and developed in several works [GAL94], [AIT96b], [CHO99b], [CHO2000a]. It is one of the novel ideas and can be extended to any digital-based transistors, pre-diffused digital arrays and even to full-custom methodology. TAT approach is not tied only to the SOT array or any digital arrays because of its natural independency to the specific type of transistors or array. It can be extended even to full-custom layouts, as this methodology makes use of interdigitizing technique for matching, transistors are partitioned for easy matching, to minimize parasitic effects and to reduce silicon area.

The TAT technique herein proposed is supported by two past research works. First, it is based on the trapezoidal-FET transistor demonstrated in [RIC84]. It has shown substantial improvement on the output conductance by shaping the FET channel width, that is, enlarging the channel width at the drain-end of the channel (small source width, large drain width). It suggests that non-rectangular geometry channels substantially broadening toward the drain can be used to reduce the transistor output conductance in saturation. This in turn can be beneficial in designing analog circuits as well as in controlling short channel effects and furthermore, narrowing channel geometries lead to increased output conductance.

Second, originally the TAT technique was first introduced in the work by [GAL94]. It has proved that a trapezoidal association of FET transistors can be exploited for the generation of electrically equivalent to a single FET device. The variable channel-geometry lengths, widths and W/L ratios that are required for any analog systems design can be emulated with series-parallel association of fixed-size transistors. In the composite transistors used in this thesis, the series association of transistors is limited to two. Later, as shown in this thesis, besides other advantages, "shaping" the association in a trapezoidal structure is helpful to improve the output conductance, just like the trapezoidal-FET.

Here, TAT approach is extended to the exploration in the field of VLSI-ULSI CMOS technology. Moreover, this extension is further considered to the semi-custom SOT array design strategy for analog applications. Indeed, the principle of the TAT is put forward here as an alternative, among the others, for the analog implementation in a digital environment and to provide faster analog systems prototyping. Although TAT devices present moderately by larger noise in comparison to the equivalent single transistor, it has shown overall good performance. This work demonstrates theoretically and experimentally that the TAT technique can be a good choice for the analog semi-custom ASIC designers.

The TAT technique will be extensively described and systematically analyzed. To better understanding and investigation, several transistors structures were included in both SOT and full-custom methodologies. A presentation of the results for 1.0µm digital CMOS technology is done first. Several electrical simulations are presented with comparisons between TAT and conventional transistor. The same procedure is accomplished with experimental measurements from the fabricated test-chips, including also comparison evaluation from measures and simulation results. Basic analog circuits have been also designed and implemented, such as current mirrors, comparators and amplifiers. Additionally, each block is validated employing CMOS technologies at both 1.0µm and 0.5µm of minimum-length.

The OTAs (in full-custom and SOT array methodology) are for 1.0µm CMOS technology since these OTA designs are originally from research work developed in a Master dissertation [CHO 94]. These OTAs are the subject of SOT array methodology exploration, but they are not directly employed in the Sigma-Delta modulator design, given that a fully differential OTA was required. The A/D converter design is based on the design done by the

author in the Analog VLSI Laboratory at Ohio State University (OSU), where a multi-standard Sigma-Delta A/D converter for wireless communication was designed.

The current mirrors were included in order to check the matching in the transistor pairs, which demonstrated interesting results. The comparator is also from the design in [CHO94], but now it was updated and re-designed for a 0.5µm CMOS technology. This latter component block is used in the Sigma-Delta design, since it was the comparator implemented in the Sigma-Delta project done at OSU.

3 Trapezoidal Association of Transistors

This chapter introduces the innovative TAT technique that basis in the VLSI CMOS technology, with its description and analysis. The investigation and validation are supported by simulations with HSpice simulator (Level 3, 6 and 49) and experimental comparisons in test IC's that implement transistors structures in 1.0μm digital CMOS technology in chapter 4. In the following section, before presenting TAT approach, the digital gate array that was taken here to implement TAT transistors is presented. That is, next section is set aside to an overview of Sea-Of-Transistors array with its origin, basis and electrical characteristics. In this chapter and the following, all voltages are referred to the bulk terminal of all devices.

3.1 SOT Array Quick Overview

The Sea-Of-Transistors array is a PROCIMS project supported by PROTEM CC, phase II, and it has been developed since March, 1995 by South Brazilian Universities with in the partnership of PROCIMS group at LINSE/UFSC, UFPR and FEJ. This SOT array was previously introduced by [AIT96a], [CHO98a], [CHO98b]. Here, the SOT array is taken as the pre-diffused gate array for design examples and applications. Consequently, the previous work with detailed TAT performance analysis is continued, and analog sub-circuits design using TAT and comparisons with full-custom methodology is developed.

The architecture of SOT array, shown in Fig. 3.1, is divided in macro-architecture and micro-architecture. The first one is associated to the general organization of the array, that is, to the construction of the array using unit cells. Therefore, the second one is the architecture of unit cells.

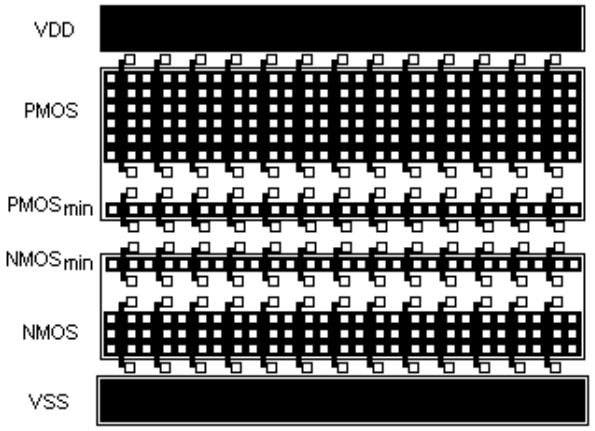


FIGURE 3.1 - Projected SOT Array with fixed size of unit transistors.

The macro-architecture has the same structure of traditional gate arrays: orthogonal structure and composed by horizontal diffusion lines and vertical polysilicon lines. This configuration presents several advantages, which shows convenient characteristics for analog design as well: It is important to pay attention to the possibility of mixed circuits over SOT array:

- higher transistors density;
- logic design flexibility due to isolation gate technique;
- routing flexibility (no routing channels);
- cells transparency principle for interconnections;
- regular structure, suitable for series-parallel association of transistors;
- symmetry and regularity allowing better matching.

The sizing process of unit transistors available on SOT array was defined in partnership with PROCIMS and Microelectronics group members. Firstly, the group has chosen the 1.0µm digital CMOS technology from ES2 foundry for semi-custom array implementation, mainly because the availability of the design rules and multi-user prototyping accesses at the beginning of the joint project between UFRGS and UFSC universities (1995). For future implementation in a higher density technology, such as 0.5µm digital CMOS technology from MOSIS, the unit transistors were designed accordingly to the constraints and principles below described.

There is a compromise by means of unit transistors dimension for different types of design. To let analog and digital designs in the same chip, minimum and non-minimum transistor geometries are required. Hence, unit transistors were sized in such a way to facilitate technology downscaling migration. It has been taken into account solely the digital circuits demand for speed (minimum L transistors only) and adequate average load drive at the digital gate outputs considering local routing (W/L of unit N-FET around 10).

TABLE 3.1 - Unit transistors available on SOT array for a given technology.

	1.0mm CMOS Technology	**0.5mm CMOS Technology**
Unit transistors on SOT	**W / L (mm)**	**W / L (mm)**
$NMOS_{mim}$ & $PMOS_{min}$	2.5 / 1.0	1.2 / 0.6
NMOS	10.5 / 1.0	5.4 / 0.6
PMOS	22.5 / 1.0	11.7 / 0.6

For the smallest transistors on the array, the channel length and width were set to the minimum values that the technology allows (L_{min} and W_{min} for contact to a minimum diffusion area), which are referred as $NMOS_{min}$ for N type and $PMOS_{min}$ for P type FET transistors in Fig. 3.1. For non-minimum transistors, channel length was set to minimum L_{min} and channel width approximately 10 times larger than L_{min} ($W \cong 10L_{min}$). The size ratio between N and P type transistors was established according to different carriers mobility in each transistor. Thus, drawn sizes of non-minimum geometry for NMOS transistors are W/L=10.5µm/1.0µm (5.4µm/0.6µm) and for PMOS transistors are W/L=22.5µm/1.0µm (11.7µm/0.6µm). Table 3.1 shows these pre-diffused transistors drawn sizes constrained by design rules forced by 1.0µm and 0.5µm digital CMOS technology from ES2 commercial foundry and from AMI foundry through MOSIS, respectively.

Routing constraints for the large digital circuits enforce furthermore the overall transistor topology for SOT array exploited in this work. The analog design cleverness is subsequently left with the task of emulating electrical behavior of arbitrarily sized transistors, which are normally larger than L_{min} and require various W/L ratios for adequate analog performance [AIT96a], [AIT97].

3.2 Trapezoidal MOSFET Transistor

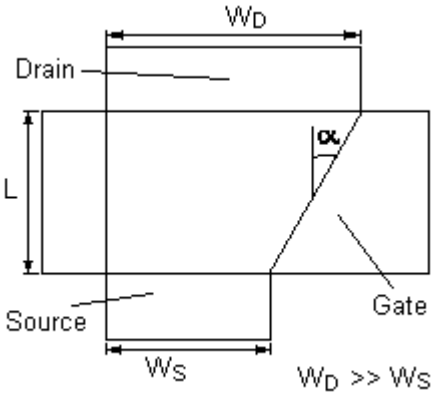


FIGURE 3.2 - A custom trapezoidal MOSFET: drain larger than source terminal.

Before starting the TAT technique analysis, it worth to present first the earlier work demonstrated by Riccò [RIC84], in order to better support and understand the trapezoidal FET, on which the TAT transistor is strongly based. By shaping the channel geometry of any MOSFET transistor (NMOS in this example), that is, making the drain end terminal larger than source end terminal – illustrated in Fig. 3.2 - leads to the following expression (from expressions 4.1.1 and 4.1.6) for the current in saturation:

$$I_D = \frac{1}{E} \cdot \frac{b}{2} \cdot \left(V_P\right)^2 \qquad 3.2.1$$

where the factor E is given by:

$$E = \frac{L}{W_S} + \frac{\log\left(\frac{W_D}{W_S}\right)}{\tan a} \qquad 3.2.2$$

where W_D, W_S, L and $\boldsymbol{a}$ are drain and source channel width, channel length and channel argument, respectively indicated in the Fig. 3.2.

From the previous expression for the drain-to-source current can be demonstrated [RIC84] that the output conductance is given by:

$$g_o = \frac{-I_D}{W_D}\frac{1}{E}\frac{dL}{dV_D} \qquad 3.2.3$$

where the last term represents the (unknown) channel-length modulation parameter, which for instance is considered independent of the geometry.

It has been proved from the above expression that it is possible to decrease the output conductance by using reasonable values of the involved parameters: making W_D very larger than W_S or increasing α. That is, a trapezoidal transistor has one additional design freedom. This is the main difference of the TAT approach to others (section 2.3).

The parameter α, that characterizes a trapezoidal shape of the gate channel, for a TAT transistor can be seen as a parameter of discrete channel transistor. For instance, consider a composite transistor that in-series transistors are not limited by two. Associating *nl* series-transistors with each one having a drain channel width increasing *md* times-step of the unit drain width W_{Du} from the previous one, the channel gate area can be approximated as a discrete trapezoidal geometry. Then, the parameter α can be roughly estimated as follows:

$$\alpha \cong \text{arc tg}\left(\frac{md \cdot (W_{D_u})}{nl \cdot (L_{\min_u})}\right) \qquad 3.2.4$$

where $L_{\min_u}$ represents the drawn length or the minimum channel-length of a particular technology. The above expression (3.2.4), shows that even for a TAT transistor, the factor E (equation 3.2.2) is dependent on α and W_D. That is, varying conveniently the number of unit transistors ND (MD in Fig. 3.3), an equivalent trapezoidal (association) shape of a transistor is achieved, as will be demonstrated later.

3.3 TAT Transistor Assembling

From the layout point of view, analog circuit design requires specific features that digital-oriented semi-custom environment may not well supported. Thus, several aspects must be discussed before presenting the construction of a TAT.

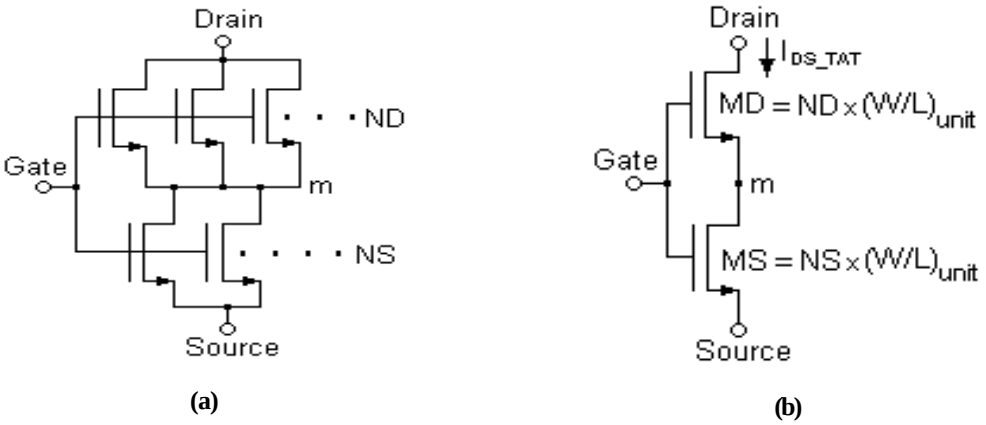


FIGURE 3.3 - (a) MD and MS serial-parallel association of unit transistors. (b) TAT as a self-cascode [ENZ96b].

Digital circuits only use transistors with minimum channel length. Moreover, even if transistor sizing may affect circuit performance, precise dimensions are usually not required. In analog design, a precise control of the transistor channel width and length is mandatory. In particular, non-minimum channel lengths are frequent. Mainly by two reasons, in analog design it is avoided:

- device matching is proportional to gate surface (at first order) [MEY85]. At fixed and increasing simultaneously W and L, matching is improved;
- the output conductance is strongly affected by short-channel effects. Longer channels yield lower output conductance (demonstrated later by experimental measurements).

Since in the SOT array is available only digital-based pre-diffused transistors, minimum channel length and pre-defined width only, a number of channel geometries (larger

L and W) is realized by serial-parallel association of these transistors. The series connection results physically in a presence of intermediate diffusion area that is associated non-ideal properties. Later these properties will be re-called to clarify TAT analysis.

The zero[th]-order approximation for the implementation of a single transistor into an electrically equivalent TAT transistor is realized with the following expressions, which give the approximate equivalent ratio $(W/L)_{eq}$ [GAL94]:

$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_{MD} \cdot \left(\frac{W}{L}\right)_{MS}}{\left(\frac{W}{L}\right)_{MD} + \left(\frac{W}{L}\right)_{MS}} = \left(\frac{W}{L}\right)_{MD} \cdot \frac{1}{m+1} = \left(\frac{W}{L}\right)_{MS} \cdot \frac{m}{m+1} \qquad 3.3.1$$

and m is given by:

$$m = \frac{ND}{NS} \qquad 3.3.2$$

where $\left(\frac{W}{L}\right)_{MD}$, $\left(\frac{W}{L}\right)_{MS}$, ND and NS are the $\left(\frac{W}{L}\right)$ ratios, and the number of unit transistors of the top and bottom parallel association MD and MS transistors, respectively.

Taking into account the limit of the function in (3.3.1), from $m=1$ *to* $m \to \infty$, the TAT transistor equivalent aspect ratio will vary between a half of the MS aspect ratio and its physical individual value ($(W/L)_{MS}$). Therefore, we must impose an aspect ratio to the MS transistor greater than the required aspect ratio and smaller or equal than twice this value in order to get a trapezoidal association transistor.

Actually, equation 3.3.1 is originated for the case when MD and MS transistors are in triode region. The equivalent W/L ratio is settled on by the equivalent resistance of the TAT structured by MD and MS, which is the same as two-sheet resistor in parallel.

Again from [GAL94], all composite transistors with same technological parameters are DC equivalent if they hold the following characteristics:

(a) similar aspect ratio (W/L);

(b) similar channel width at drain end terminal; and

(c) same short-channel effects in triode (conduction) region (MS and MD).

According to the statement (a) and (b), electrically DC equivalent channel width (W) and length (L) of a composite transistor can be proved that:

$$W_{eq} = W_D = m \cdot W_u \qquad 3.3.3$$

W_u is the width of unitary fixed transistors. Above expression can be rewritten as follows:

$$W_{eq} = \left(\frac{W}{L}\right)_{MD} \cdot L_{eq} \cdot \frac{1}{m+1} \qquad 3.3.4$$

where from the expression 3.3.1 derives the equivalent channel length:

$$L_{eq} = L_{MD} + m \cdot L_{MS} = (1+m) \cdot L_{\min} \qquad 3.3.5$$

where L_{MD} and L_{MS} are free choice design parameters for the channel lengths and/or constrained by the technology. For this particular TAT case, L_{MD} and L_{MS} are equal and have minimum-L allowed by the technology.

Consequently, with the aim to achieve a TAT transistor equivalent to a long channel, transistor with $m > 1$ (trapezoidal) have to be selected. Furthermore, even if the condition (c) is not fulfilled, the TAT transistor with larger drain end terminal has lower output conductance in saturation caused by the lower current density at the drain region or in MD transistor. That is, MD wider than MS and the total current constant in both transistors, the current density is higher in MS transistor.

The approximation of optimal W/L ratios by discrete values is not a limiting factor for the performance of analog circuits. Moreover, the implementation of wide channels by

parallel arrangement is used frequently and parallel compositions are extensively used even in full-custom designs. In the SOT array, one has the limitation of using only minimum-L for MD and MS transistors.

Additionally, a natural consequence of making very simple association of minimum transistors to build a single one is that multiples of the elementary width and length can be obtained, in parallel-only and serial-only. In this work, as already described, it is considered that TAT association may have a maximum of two series-connected transistors of L_{min}, to obtain an arbitrary $\left(\frac{W}{L}\right)_{eq}$ associations. Therefore, an optimal W/L ratio imposed by circuit design may not be exactly achieved. Thus, the TAT assembling process must be developed as follows:

1. design sizing determines optimal W/L of all devices that are converted into their equivalent TAT versions;
2. all converted W/L ratios, L's and W's must be checked with their original designed single transistors by making approximations as close as possible to the original W/L set by the designer, by multiple unit transistors;
3. check the previous procedure with hand calculations and/or by electrical simulations;
4. if the specifications are not met, transistors conversion must be modified iteratively.

The above conversion process is not tedious or time-consuming, because it is realized by the designer interactively with a TAT generation tool program [AIT2000] to help in this task. This CAD tool has a Spice file format as input and output, gives several alternatives of TATs for the same single transistor and designer experience comes in to select one among several options to lead a better choice.

4 TAT Transistor Analysis

This chapter is devoted to DC, AC and noise analysis of a TAT transistor, revealing that a TAT is equivalent to a single transistor with added improvement, that is, reduction on the output conductance. However, short-channel effects remain because of minimum-L of unit transistors. All analysis is followed by electrical simulations and experimental comparisons of the data.

4.1 Large Signal Modeling

The drain currents of the series transistors MD and MS are exactly the drain current of the TAT ($I_{D_{TAT}} = I_{D_{MD}} = I_{D_{MS}}$) and it is given by [ENZ89], [ENZ96b]:

$$I_{D_{TAT}} = I_F(V_P, V_S) - I_R(V_P, V_D) \qquad 4.1.1$$

where V_P, V_D and V_S are the pinch-off, drain and source voltages, respectively, I_F and I_R are the forward and reverse currents, respectively. The drain currents of the top MD and bottom MS transistors are given, respectively, by [ENZ89], [ENZ96b], [HAA96]:

$$I_{D_{MD}} = m \cdot \left(\frac{W}{L}\right)_u \int_{V_{CH}=V_{S_{MD}}}^{V_{CH}=V_{D_{MD}}} f(V_G, V_{CH}) \cdot dV_{CH} \qquad 4.1.2$$

$$I_{D_{MS}} = m \cdot \left(\frac{W}{L}\right)_u \int_{V_{CH}=V_{S_{MS}}}^{V_{CH}=V_{D_{MS}}} f(V_G, V_{CH}) \cdot dV_{CH} \qquad 4.1.3$$

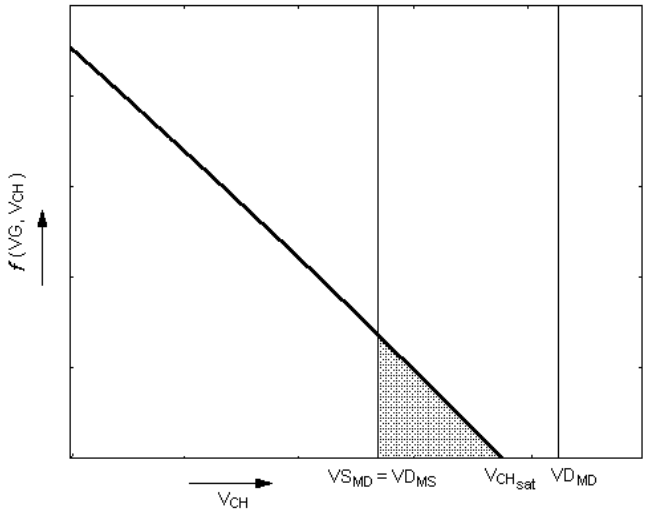


FIGURE 4.1 - Graphical representation of TAT current in saturation.

and V_{CH} is the channel potential defined as the difference between the Fermi quasi-potential of the carriers forming the channel and the Fermi quasi-potential of the bulk [ENZ89]; and $V_{D_{MD}}$, $V_{S_{MD}}$, $V_{D_{MS}}$ and $V_{S_{MS}}$ are the drain and source voltage of the MD and MS transistor, respectively.

While the $f(V_G,V_{CH})$ [TSI88], [ENZ89] is given by:

$$f(V_G,V_{CH}) = \left(U_T \frac{dQ_C}{dx} - Q_C \frac{d\phi_S}{dx} \right) \qquad 4.1.4$$

where, Q_C represents the local channel charge, U_T is the thermodynamic potential, ϕ_s is the surface potential and x a point along the channel. The first term represents the diffusion current and the second the drift current.

From equation 4.1.4 an important conclusion outcomes about the TAT transistor. The bottom MS transistor always operates in the linear region (conduction) since $V_{D_{MS}} \leq V_{S_{MD}} < V_{CH_{SAT}}$ - shaded area in Fig. 4.1 represents the current $I_{D_{TAT}}$. TAT operates in the linear region if both $V_{D_{MD}} < V_{CH_{SAT}}$ and $V_{D_{MS}} < V_{CH_{SAT}}$, and in saturation if $V_{D_{MD}} > V_{CH_{SAT}}$. The $V_{CH_{SAT}}$ is the pinch-off voltage V_P, that is, it is the channel potential corresponding to the limit of weak inversion for a given gate voltage V_G (defined in [ENZ89], [ENZ96a]).

Once more, underlining the modes of operation of the TAT transistor, both transistors operate in the weak inversion at lower gate-voltage level (bellow the equivalent TAT threshold voltage V_T), while at higher gate-voltage level both transistors are strong inverted. Then, increasing drain voltage of the TAT V_D (> V_P), the transistor MD is pinched-off (saturated) but the transistor MS remains in conduction (linear region). Under this condition, MD works as a current source and its drain current is invariable (except for channel modulation effects) even increasing V_D further than V_P. Additionally, the contribution of the transistor MS with increasing on V_D is unchanging since the drain voltage of MS is fixed by the saturated drain-source voltage of the MD transistor.

From the equation 4.1.1 and integrating the MD and MS currents (equations 4.1.2 and 4.1.3), lead to the $I_{D_{TAT}}$ in weak inversion, valid in both conduction and saturation region [ENZ96b]:

$$I_{D_X} = I_{D_{TAT}} = I_{F_X} - I_{R_X} = I_S \cdot e^{\frac{V_P}{U_T}} \left(e^{-\frac{V_{S_X}}{U_T}} - e^{-\frac{V_{D_X}}{U_T}} \right) \qquad 4.1.5$$

where X can be MD or MS. In strong inversion and saturated it is given by:

$$I_{D_{TAT}} = I_{D_X} = I_{F_X} - I_{R_X} =$$

$$= \frac{n \cdot b_X}{2} \cdot \left[\left(V_P - V_{S_X} \right)^2 - \left(V_P - V_{D_X} \right)^2 \right] =$$

$$= I_S \cdot \left[\left(\frac{V_P - V_{S_X}}{2 \cdot U_T} \right)^2 - \left(\frac{V_P - V_{D_X}}{2 \cdot U_T} \right)^2 \right] \qquad 4.1.6a$$

and for MD and MS in conduction (SI):

$$I_{D_X} = n \cdot b_X \left(V_P - \frac{V_{S_X} + V_{D_X}}{2} \right) \left(V_{D_X} - V_{S_X} \right) \qquad 4.1.6b$$

where each parameter is defined as follows:

$\beta = \mu C_{ox} \frac{W}{L}$	β is transconductance factor, μ is carrier mobility and C_{ox} is oxide capacitance;
$n \cong 1 + \frac{\gamma}{2\sqrt{\Psi_0}}$	n is slope factor, γ is body effect factor as defined in [ENZ89], [LAK94], Ψ_0 is bulk Fermi potential;
$U_T \equiv \frac{kT}{q}$	U_T is thermodynamic potential, k is absolute temperature; q=1.602x10^{-19}C electron charge
$I_S \equiv 2n\beta U_T^2$	I_S is the specific current. 4.1.7

Emphasizing over again, the TAT drain current is either MD or MS drain current and for saturation region $I_R = 0$. Remind that, the source terminal of the MD transistor is shared with drain terminal of MS transistor (the middle node *m* shown in Fig. 3.3). Then, the MD source voltage $V_{S_{MD}}$ is the same of the MS drain voltage $V_{D_{MS}}$. It leads to that, both the top MD and bottom MS transistors shown in Fig. 3.3, have the same gate voltage ($V_{G_{TAT}}$), consequently they also have the same pinch-off voltage V_P. Hence, independently of the gate voltage, considering that MD is saturated (TAT in saturation) and that MS (in conduction) source terminal is at the same bulk-voltage level, the drain currents of the MD and MS transistors (eq. 4.1.6) are:

$$I_{D_{MD}} = I_{D_{MS}} \Rightarrow \frac{n \cdot \beta_{MD}}{2}\left(V_P - V_m\right)^2 = \frac{n \cdot \beta_{MS}}{2}\left[V_P^2 - \left(V_P - V_m\right)^2\right] \qquad 4.1.8$$

where V_m represents the voltage of the middle node. Then, solving 4.1.8 leads to following voltage V_m in strong inversion [ENZ96b]:

$$V_m = V_{S_{MD}} = V_{D_{MS}} = \left[1 - \frac{1}{\sqrt{1 + \frac{S_{MD}}{S_{MS}}}}\right].V_P = \left[1 - \frac{1}{\sqrt{1 + \frac{ND}{NS}}}\right].V_P \qquad 4.1.9$$

and for the case when TAT is in weak inversion and equating 4.1.5a and 4.1.5b, the V_m is simply given by:

$$V_m = V_{S_{MD}} = V_{D_{MS}} = U_T \cdot \ln\left(1 + \frac{S_{MD}}{S_{MS}}\right) = U_T \cdot \ln\left(1 + \frac{ND}{NS}\right) \qquad 4.1.10$$

where S_{MD} and S_{MS} are the W/L ratios of the MD and MS transistors, respectively. For the case TAT is in conduction (both MD and MS in conduction), V_m is given simply by voltage divider (large resistances of MD and MS).

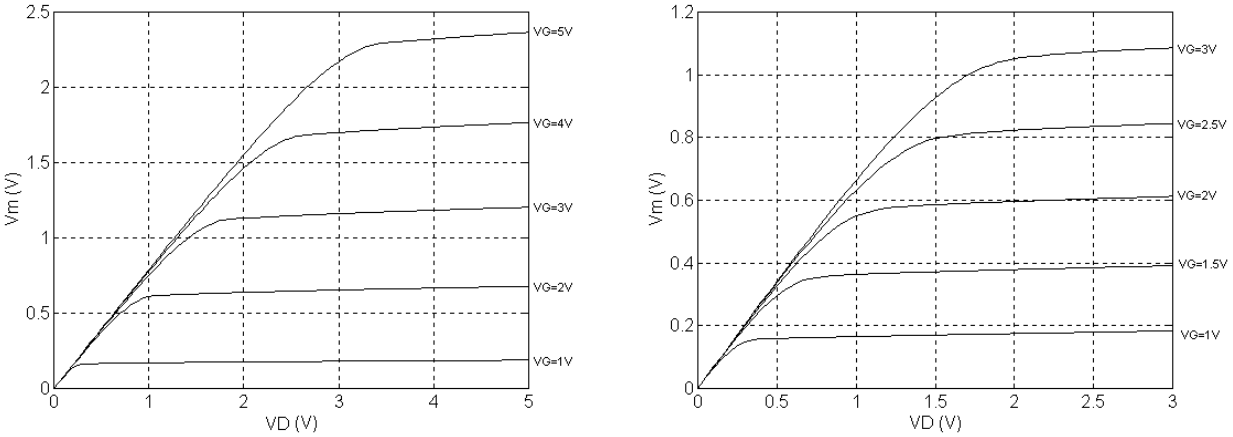
Previous results are the most significant equations that express the TAT transistor behavior and its intrinsic performance. This effect not simply aids to improve the output conductance but reduces the body effect ($0 \neq V_{SB_{MD}} \cong const.$) and parasitic capacitances ($C_{GS_{MS}}$ and $C_{GD_{MS}} + C_{GS_{MD}}$). At this point, the expression 3.3.1 can be derived from the expression 4.1.8. In the right side of equation 4.1.8 (MS in conduction), the variable $V_{S_{MS}}$ is kept, resulting in the following expression:

$$\left(V_p - V_m\right)^2 = \frac{\left(V_p - V_{S_{MS}}\right)^2}{\left(\frac{S_{MD}}{S_{MS}} + 1\right)} \qquad 4.1.11$$

and substituting $\left(V_P - V_m\right)^2$ with the expression 4.1.11 in either MD (sat.) or MS (cond.) equations leads to equivalent $\beta_{TAT} = \frac{\beta_{MD} \cdot \beta_{MS}}{\beta_{MD} + \beta_{MS}}$. The same procedure can be done to the TAT in conduction (MD and MS in conduction).

Since the TAT transistor is trapezoidal by definition, specifically MD made larger than MS ($S_{MD} > S_{MS}$ or ND > NS), the V_m voltage can be approximated to V_P (slightly smaller). Hence, while in weak inversion V_m is dependent on only S_{MD} and S_{MS} ratios, in strong

inversion V_m is clamped on V_P, as demonstrated by electrical simulations plotted in Fig 4.2. The plot in Fig. 4.2a is the V_m curve of an arbitrary example for a TAT transistor in 1.0µm CMOS technology, while the plot in Fig. 4.2b is for a TAT transistor in 0.5µm CMOS technology.



(a) (b)

FIGURE 4.2 - Simulated V_m x V_D curve characteristic of TAT: (a) ND=16, NS=4, $(W/L)_u$=(10.5µm /1.0µm), L_{min}=1.0µm, 1.0µm CMOS technology. (b) ND=20, NS=9, $(W/L)_u$=(5.4µm/0.6µm), L_{min}=0.6µm, 0.5µm CMOS technology.

The simulations show that, fixing TAT gate voltage and varying drain voltage, any additional voltage ahead of the voltage that is required for saturating MS transistor is dropped over MD transistor. In that case, the transistor MS is constantly in triode mode (linear region), that is in onset to saturation. Note that, the flat regions of the V_m curves (saturated region) are the straight values of pinch-off voltage (if ND >> NS), i. e., a fraction of V_P (4.1.9) since its value depends on the MD and MS geometry ratios.

Another important conclusion is that, a TAT transistor can be applied in several low-voltage applications, since it works as a self-cascode circuit, i. e., as an intrinsic poor cascode stage. Normally, a second gate bias for MD is required for a traditional cascode operation. It does not need higher saturation voltage levels, since the MS device never saturate and its drain voltage (V_m) is low.

4.2 Short-Channel Effects Investigation

The short-channel effects that take part in saturated region, channel length modulation and static feedback (DIBL – Drain Induced Barrier Lowering) [TSI88], only have effect on the top parallel associated MD transistor. For that reason, these effects are not associated with the intermediate diffusion (merged MS drain and MD source - Fig. 4.3) and need not be considered in this case.

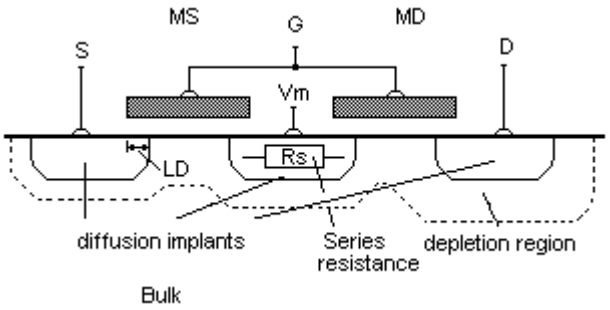


FIGURE 4.3 - Cross-section of the TAT transistor showing associated diffusion areas effects: lateral diffusion, series resistance and depletion regions.

There are well known non-ideal properties related to the diffusion areas in any MOSFET transistor, as illustrated in Fig. 4.3. First, there is the lateral diffusion effect (LD) caused by diffusion areas that get larger than defined by the layout and widen underneath the gates. This effect decreases the effective channel length defined by layout design. Second, to any diffusion implant a parasitic series resistance is associated, which appears as a reduction of the electrically effective mobility. Lastly, another effect associated to the diffusion implants is the *pn* junctions that are reverse biased under normal operation of the TAT (MD in saturation and MS in conduction), which results in depletion regions and junction capacitances.

The depletion regions of the *pn* junctions partly widen into channel region, as consequence associated charges act partially as oppose part for the charge on the gate and automatically reduces to a certain extend bulk charge. This is known as charge sharing [TSI88], which effect is seen as reduction of the body effect and the threshold voltage. In a single transistor, the short-channel effects decrease with increasing gate length. While for a TAT, an increase in an equivalent channel length, the short-channel effects remain constant since the MD and MS channel lengths remain physically constant at the minimum-L.

While in any single transistor, the lateral diffusion LD effect is negligible when the channel length L is very large ($L >> LD$) in comparison to LD, in the minimum-L unit transistors of the MD and MS transistors suffer from this LD effect. Taking into account the LD effect and depletion region introduced by drain voltage, the effective channel length of the MD $L_{eff_{MD}}$ and MS $L_{eff_{MS}}$ transistors then can be given by:

$$L_{eff_{MD}} = L_{\min} - 2 \cdot LD - \Delta L \quad \text{; MD in saturation} \qquad 4.2.1a$$

$$L_{eff_X} = L_{\min} - 2 \cdot LD \quad \text{; MD or MS in conduction} \qquad 4.2.1b$$

where L_{min} is the channel length of the unit minimum-L transistors that compose in-parallel association MD and MS transistors, LD is the lateral diffusion introduced by the process, and ΔL is the diminution caused by depletion region (in saturation case).

When V_D becomes equal to V_P, the channel is pinched-off just at drain diffusion limit. When V_D becomes higher then V_P ($V_D > V_P$), the pinch-off point moves towards the source, reducing the effective channel length by ΔL (DIBL), besides the channel length reduction introduced by LD. The inversion charge between this point and the drain is nearly zero and therefore this region can be considered as a depletion region as illustrated in Fig. 4.3. The channel length reduction ΔL can be then approximated by [TSI88], [ENZ89]:

$$\Delta L \approx L \cdot \frac{V_{D_{MD}} - V_P}{V_{E_{MD}} - V_{D_{MD}}} \qquad 4.2.2$$

$V_{E_{MD}}$ is the Early voltage of the MD transistor. It is proportional to the effective channel length L_{eff}, and is given by:

$$V_{E_{MD}} = l \cdot L_{eff_{MD}} \qquad 4.2.3$$

where l is the channel modulation factor. In practice $V_{E_{MD}}$ and l are dependent on the drain voltage [TSI88]. However, they can be assumed to be constant in a first order analysis.

Finally, the transistor effective transconductance factor β_{eff} can be estimated from equation 4.2.2. Moreover, from the ideal transconductance factor listed in 4.1.7, the transconductance ratio r_β can be approximated by [ENZ89]:

$$r_b = \frac{\beta_{eff_{MD}}}{\beta_{o_{MD}}} \approx 1 + \frac{V_{D_{MD}} - V_P}{V_{E_{MD}} + V_P} \qquad 4.2.4$$

where $\beta_{o_{MD}}$ is the ideal transconductance factor for the MD transistor.

The parasitic resistances associated with the diffusions must be accounted, particularly for the TAT device since it is an association of several minimum-L transistors. Thus, the short channel devices suffer from these parasitic resistances. There are three different categories of resistance [TSI88]: (a) the resistance of the metal contact to the n^+ implants region; (b) the resistance of the diffusion body; and (c) the resistance associated to the carriers channel itself.

The influence of the previous resistances can be roughly modeled by simply associating to the drain and source voltage, a voltage drop caused by the total parasitic series resistances, as follows:

$$V_{D_{eff}} = V_D - V_{res} = V_D - R_{total} \cdot I_{TAT} \qquad 4.2.5$$

where V_{res} is the total voltage drop due to total series resistance R_{total}. Substituting above expression in the either MD and MS drain current in conduction (equation 4.1.6b) leads to:

$$I_D = \frac{n \cdot \beta \left(V_P - \frac{V_S + V_D}{2} \right) (V_D - V_S)}{1 - n \cdot \beta \cdot R_{total} \left(\frac{V_D - V_S}{2} - V_P \right)} \qquad 4.2.6$$

Typically, the product factor $n \cdot \beta \cdot R_{total}$ is negligible in a large L and for correctly designed contact holes, which are close to the edge of the active channel, typically given by design rules of minimum poly-to-contact spacing. For short channel devices, this effect

manifests itself as an effective transconductance degradation, and can be added to the factor modeling the reduction on the effective mobility with V_G.

Separating the contribution of each parasitic resistance of the TAT device, the total resistance is expressed without difficulty as follows:

$$R_{total} = R_{DS} + R_{con} + R_{diff} \tag{4.2.7a}$$

where R_{DS} represents TAT drain-to-source resistance, R_{con} represents total resistance of the metal-to-diffusion contacts that accounts also the intermediate contacts (connection of the MD source terminal and MS drain terminal), and R_{diff} is the total intermediate diffusion resistance. Each term can be straightforward expanded and are given by:

$$R_{DS} = R_{DS_{MD}} + R_{DS_{MS}} = \frac{(R_{DS})_u}{ND} + \frac{(R_{DS})_u}{NS} = \frac{ND \cdot NS}{ND + NS} \cdot (R_{DS})_u = b_{TAT} \cdot (R_{DS})_u \tag{4.2.7b}$$

$$R_{con} = R_{con_{MD}} + R_{con_{MS}} = \frac{(R_{con})_u}{c1} + \frac{(R_{con})_u}{c2} = \frac{c1 \cdot c2}{c1 + c2}(R_{con})_u \tag{4.2.7c}$$

$$R_{diff} = R_{diff_{MS}} \tag{4.2.7d}$$

where $c1$ and $c2$ are the total number of contact heads (metal-to-diffusion) employed on the association and interconnection of the unit minimum-L transistors to assemble MD and MS devices; and $(R_{DS})_u$ and $(R_{con})_u$ represent the unit transistor drain-to-source resistance and a single contact resistance, respectively.

From expressions 4.2.7, it is obvious and clear that the improvement (reduction) on the total TAT channel resistance can be achieved enlarging MS transistor (increasing NS) and/or not saving on the number of contacts.

4.3 Small Signal Modeling: Low and Medium Frequency

The gate, source and drain transconductances of the MD and MS (conduction) transistors in weak inversion are simply given by [ENZ89], [ENZ96b]:

$$g_{mG_X} = \frac{I_{D_X}}{n \cdot U_T} \tag{4.3.1a}$$

$$g_{mS_X} = \frac{I_{F_X}}{U_T} \tag{4.3.1b}$$

$$g_{mD_X} = \frac{I_{R_X}}{U_T} \tag{4.3.1c}$$

and in strong inversion are given by:

$$g_{mG_X} = b \cdot \left(V_{D_X} - V_{S_X}\right) \tag{4.3.2a}$$

$$g_{mS_X} = n \cdot g_{mG_X} = \sqrt{2n \cdot b \cdot I_{F_X}} = \frac{2 \cdot I_{F_X}}{\left(V_P - V_{S_X}\right)} \tag{4.3.2b}$$

$$g_{mD_X} = n \cdot b \cdot \left(V_P - V_{D_X}\right) = \sqrt{2n \cdot b \cdot I_{R_X}} = \frac{2 \cdot I_{R_X}}{\left(V_P - V_{D_X}\right)} \tag{4.3.2c}$$

MD in saturation

$$g_{mG_{MD}} = b \cdot \left(V_P - V_{S_{MD}}\right) = \sqrt{\frac{2b \cdot I_{D_{MD}}}{n}} = \frac{2 \cdot I_{D_{MD}}}{n \cdot \left(V_P - V_{S_{MD}}\right)} \tag{4.3.3a}$$

$$g_{mS_{MD}} = n \cdot g_{mG_{MD}} = \sqrt{2n \cdot b \cdot I_{F_{MD}}} = \frac{2 \cdot I_{F_{MD}}}{\left(V_P - V_{S_{MD}}\right)} \tag{4.3.3b}$$

$$g_{mD_{MD}} = 0 \tag{4.3.3c}$$

Consider once more Fig. 3.3b. It can be demonstrated that the output conductance of the TAT transistor $g_{o_{TAT}}$, a combination of association of the unit transistors that generate MD and MS transistors with an Early voltage $V_{E_{MD}}$ and $V_{E_{MS}}$, respectively, is given by [ENZ96b]:

$$g_{o_{TAT}} = g_{ds_{MD}} \frac{1+\left(\frac{g_{ds_{MS}}}{g_{mD_{MS}}}\right)}{1+\left(\frac{g_{mS_{MD}}}{g_{mD_{MS}}}\right)} = g_{ds_{MD}} \frac{1+r\cdot\left(\frac{g_{ds_{MS}}}{g_{mS_{MD}}}\right)}{1+r} \qquad 4.3.1$$

where $g_{ds_{MD}} = \frac{I_{D_{TAT}}}{V_{E_{MD}}}$ and $g_{ds_{MS}} = \frac{I_{D_{TAT}}}{V_{E_{MS}}}$ are the output conductances of the MD and MS transistor, respectively, $g_{mS_{MD}}$ (eq. 4.3.3b) is the MD (in saturation) drain transconductance and $g_{mS_{MS}}$ (eq. 4.3.2b) is the MS (in conduction) source transconductance, and the factor r is the ratio between MD forward-current and MS reverse-current $r = \frac{g_{mS_{MD}}}{g_{mD_{MS}}} = \frac{I_{F_{MD}}}{I_{R_{MS}}}$:

Weak inv.: $$r = \frac{S_{MD}}{S_{MS}} \cdot e^{\left(\frac{V_P}{U_T}\right)} = \frac{ND}{NS} \cdot e^{\left(\frac{V_P}{U_T}\right)} \qquad 4.3.2a$$

Strong inv.: $$r = \frac{S_{MD}}{S_{MS}} \cdot \left(\frac{V_P - V_{S_{MD}}}{V_P - V_{S_{MD}}}\right)^2 = \frac{ND}{NS} \cdot \left(\frac{V_P - V_{S_{MD}}}{V_P - V_{S_{MD}}}\right)^2 \qquad 4.3.2b$$

If both transistors have the same threshold voltages $V_{TO_{MS}} = V_{TO_{MD}}$ (neither short- nor narrow-channel effects), the factor r reduces to S_{MD}/S_{MS}, in both weak and strong inversion. It is partially true since MD and MS transistors are equivalent transistors obtained by way of several unit transistors, physically laid out in parallel association. Therefore, the equivalent threshold voltage is, in fact, an averaging over many unitary transistor threshold voltages, i. e., the higher spread of V_T for minimum lengths is in fact compensated by this averaging.

In view of the fact that, S_{MD}/S_{MS} is made much larger than 1 (trapezoidal association), the factor r also becomes much larger than 1. Hence, the output conductance given in equation 4.3.1 tends toward a traditional cascode stage [CHO99a], and it reduces to:

$$g_o \cong g_{ds_{MD}} \cdot \frac{g_{ds_{MS}}}{g_{mS_{MD}}} \Rightarrow r_o \cong r_{ds_{MS}} \cdot \left(r_{ds_{MD}} \cdot g_{mS_{MD}}\right) \; ; \quad for \quad r >> 1 \qquad 4.3.3$$

The expression above can be effectively realized by proper TAT association design, since a TAT is trapezoidal by definition. That is, both MS and MD transistors have the same drawn minimum channel length (minimum-L) and the channel widths or the ratio S_{MD} is much larger than S_{MS} (equation 3.2.3). Furthermore, setting S_{MS} to the minimum width ($NS_{min}=1$), the threshold voltage $V_{TO_{MS}}$ increases with respect to $V_{TO_{MD}}$ due to narrow-channel effect in MS transistor ($V_P = \frac{V_G - V_{TO}}{n}$). Consequently, it helps to further increase the factor r significantly, while maintaining a reasonable S_{MD}/S_{MS}. Although applicable in both weak and strong inversions, it is however mostly effective in weak inversion, thanks to the exponential term in equation 4.3.2.

Transistor MD is made wider, then the output conductance is higher than in MS transistor. However, the high output conductance of the MD transistor is balanced by its large transconductance due to $g_{mS_{MD}}$ being directly proportional to the square root of S_{MD} and to forward current (saturation). The overall results are that, the TAT output conductance is almost similar to a single transistor. On the other hand, it can be made as low as desired, through proper design of MD (trade-off between output conductance and transconductance). Nonetheless, there is a design constraint for the TAT assembling: decreasing ND closer or even lower than NS value, TAT is no longer a trapezoidal association. Expression 4.3.3 reflects the cascode nature of the TAT, because MD provides for the gain but in fact it is not independently biased, as the conventional cascode would require.

The effective TAT transconductance can be calculated from the small-signal model of Fig. 4.4 (MD saturated and MS in conduction or in triode region):

$$g_{m_{TAT}} = \frac{g_{ds_{MS}}}{g_{mS_{MD}}} \left[\frac{g_{mG_{MS}} \cdot g_{mS_{MD}}}{g_{ds_{MD}} + g_{mD_{MS}}} + \frac{g_{mG_{MD}} \cdot g_{mD_{MS}}}{g_{mD_{MS}} - g_{mS_{MD}}} \right] \qquad 4.3.4$$

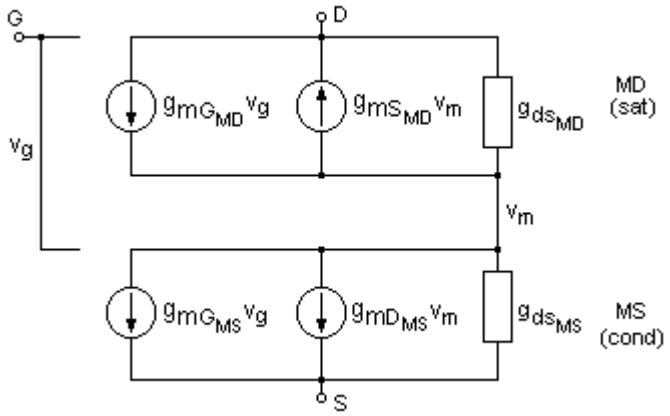


FIGURE 4.4 - TAT small-signal model for MD in saturation and MS in conduction.

where, $g_{mS_{MD}}$ and $g_{mD_{MS}}$ account for the effect of the intermediate node V_m on MD an MS devices, respectively. After some approximations [CHO99a], an important characteristic of the TAT results:

$$g_{m_{TAT}} \cong g_{mG_{MS}} \qquad 4.3.5$$

Hence, MS transistor establishes the asymptotic value of TAT transconductance, as r>>1. To improve overall TAT performance characteristics one needs to increase the MS transconductance (increasing NS), decreasing the effective output conductance of the MD (decreasing ND) and/or increasing its transconductance.

The main parasitic capacitances in TAT transistor are shown in Fig. 4.4: gate-to-source capacitance from MD transistor (in saturation); and gate-to-source and gate-to-drain capacitances from MS transistor (in conduction). It can be proved that the combination of the parasitic capacitances is similar to the capacitances present in the equivalent single device. The existence of one more node in the TAT (poles) does not degrade the bandwidth significantly since the gain-bandwidth product is kept almost constant because of its cascoding effect. This is demonstrated by electrical simulations in section 5.2.

4.4 Small Signal Modeling: High Frequency

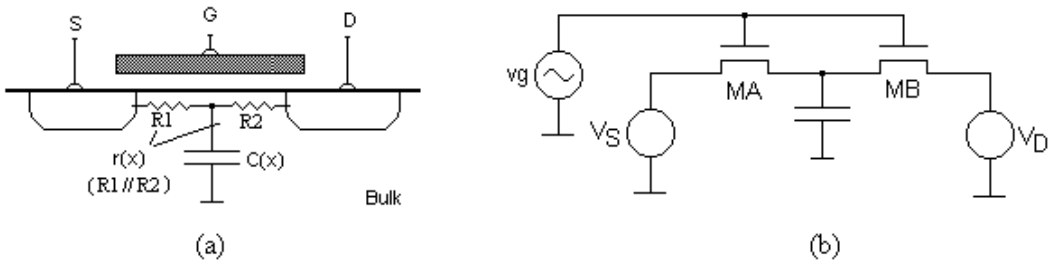


FIGURE 4.5 - Equivalent circuit to calculate the time constant approximation for high frequency.

From high frequency modeling in [ENZ89], and using the zero-value time constant approximation, the elementary resistance seen by the elementary capacitance between two elementary transistors *MA* and *MB*, from a single transistor split into a series of two elementary transistors working in a quasi-static mode (shown in Fig. 4.5), along the elementary channel, are given by [ENZ89]:

$$r(x) = \frac{1}{g_{mD_{MA}} + g_{mS_{MB}}} = \frac{x.(L-x)}{2 \cdot n \cdot W \cdot L \cdot m \cdot C_{ox} \cdot U_T} \cdot \frac{\sqrt{1+\frac{1}{2}\sqrt{i_i}+i_i}}{i_i} \qquad 4.4.1$$

$$c(x) = C_{gd_{MA}} + C_{db_{MA}} + C_{gs_{MB}} + C_{sb_{MB}} = 2 \cdot n \cdot W \cdot C_{ox} \cdot \frac{i_i}{i_i + \frac{1}{2}\sqrt{1+\frac{1}{2}\sqrt{i_i}+i_i}} \qquad 4.4.2$$

where $i_i = i_{F_{MB}} = i_{R_{MA}}$, since the forward current of MB and the reverse current MA depend only on V_m. Note that *r(x)* is the total small-signal resistance at point x along the channel (or the inverse of transadmittance Y_{mG}) and *c(x)* is the per unit length capacitance at point x. The relation between normalized current i_i and the position in the channel is [ENZ89]:

$$i_i(x) = i_F - \frac{x}{L}(i_F - i_R) \qquad 4.4.3$$

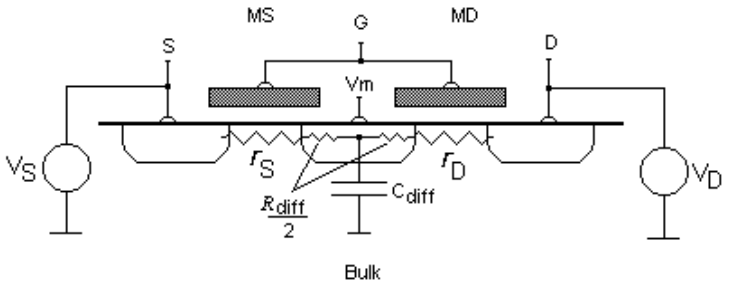


FIGURE 4.6 - Equivalent TAT circuit to calculate the time constant.

The first order time constant is calculated by integrating all elementary time constants along the channel. The time constant of the transistor in weak inversion is given by [ENZ89]:

$$t \approx \frac{t_0}{(i_F - i_R)^3} \int_{i_R}^{i_F} 2(i_F - i_i)(i_i - i_R) \cdot di_i = \frac{t_0}{3} \qquad 4.4.4$$

where $t_0 = \frac{L^2}{2mU_T}$.

In strong inversion, the time constant of a transistor is given by [ENZ89]:

$$t \approx \frac{t_0}{i_F^3} \int_{i_R}^{i_F} (i_F - i_i)\sqrt{i_i} \cdot di_i = t_0 \cdot \frac{4}{15} \cdot \left(\frac{i_F + 3 \cdot \sqrt{i_F \cdot i_R} + i_R}{\left(\sqrt{i_F} + \sqrt{i_R}\right)^3} \right) \qquad 4.4.5$$

In conduction mode ($i_F = i_R$, $V_{DS} << kT/q \Rightarrow V_S @ V_D$), the time constant reduces to $t = \frac{t_0}{6}$. In saturation mode ($i_R = 0$), the time constant is equivalent to the result found in [TSI88].

The same analysis above described can be applied to the TAT transistor behavior at high frequencies. In the TAT association shown in Fig. 4.6, if the MS and MD transistors in series are sized such that R_{diff} is much smaller than the small signal resistance r_S and r_D, the AC model of TAT, in relation to the diffusion influence, becomes:

$$C_m = C_{gd_{MS}} + C_{db_{MS}} + C_{gs_{MD}} + C_{sb_{MD}} + C_{diff} \qquad 4.4.6$$

where C_{diff} is given by:

$$C_{diff} = (ND + NS) \cdot C_{ju} \qquad 4.4.7$$

where $C_{ju} = A_{diff} \cdot C_j$. A_{diff} is the diffusion area between two unit transistors in the SOT array (Fig. 3.1 and Table 3.1), and C_j is the junction capacitance from source and drain area of a MOS transistor.

The time constant due to the intermediate diffusion areas can be calculated and is given by:

$$t_m = \left(C_{diff} + C_{ov_{MS}} + C_{ov_{MD}}\right) \cdot \left(r_S \,//\, r_D\right) \qquad 4.4.8$$

where $C_{ov_{MS}}$ and $C_{ov_{MD}}$ are the gate overlap capacitances of the MS and MD transistor, respectively, and r_S and r_D are the small signal total resistances seen at the intermediate diffusion (or at the junction capacitance C_{diff}).

It is worth noting that the resistance *r(x)* and the capacitance *c(x)* (equations 4.4.1 and 4.4.2) are inversely and directly proportional to the channel width (*W*), respectively. Then, even a TAT being a trapezoidal association ($W_D > W_S$ – section 3.2), the influence of varying width is canceled by the product $r(x) \cdot c(x)$, even if the resistance and capacitance varies continuously along the channel (as in equation 3.2.4).

$$W(x) = \begin{cases} W_S & (0 < x < L) \\ W_D & (L < x < 2L) \end{cases} \qquad 4.4.9$$

At this point, the TAT time constant using zero-value constant approximation and following the previous analysis for single transistor, can be calculated by:

$$t_{TAT} = \int_0^{2L} r(x) \cdot c(x) \cdot dx + t_m \qquad 4.4.10$$

where *r(x)* and *c(x)* are given by equations 4.4.1 and 4.4.2 replacing *L* by *2L*, leading to the following result for TAT time constant:

$$t_{TAT} = \frac{4t_0}{(i_F - i_R)^3} \int_{i_R}^{i_F} (i_F - i_i) \cdot (i_i - i_R) \cdot \left(\frac{\sqrt{1 + \frac{1}{2}\sqrt{i_i} + i_i}}{i_i + \frac{1}{2}\sqrt{1 + \frac{1}{2}\sqrt{i_i} + i_i}} \right) \cdot di_i + t_m \qquad 4.4.11$$

From the above result, the time constant of the TAT can be calculated for all region of operation. Following the same procedures done in [ENZ89], the asymptotic value of TAT time constant is given by:

$$t_{TAT_{WI}} \cong \frac{4}{3} t_o + t_m \quad \text{, in weak inversion} \qquad 4.4.12$$

$$t_{TAT_{cond}} \cong \frac{2}{3} t_o + t_m \quad \text{, in conduction} \qquad 4.4.13$$

$$t_{TAT_{SI}} \cong \frac{16}{15} t_o \frac{i_F + 3\sqrt{i_F i_R} + i_R}{\left(\sqrt{i_F} + \sqrt{i_R}\right)^3} + t_m \quad \text{, in strong inversion} \qquad 4.4.14$$

The results above are very similar to the result for a conventional transistor described in [ENZ89]. It is understandable because of the influence of intermediate diffusion was separated and the limits of channel integration was considered as *2L* (instead *L*), that is, TAT modeling follows essentially the original model [ENZ89], leading to 4 times of constant time t_0 of a single MOS transistor.

4.5 Noise Analysis

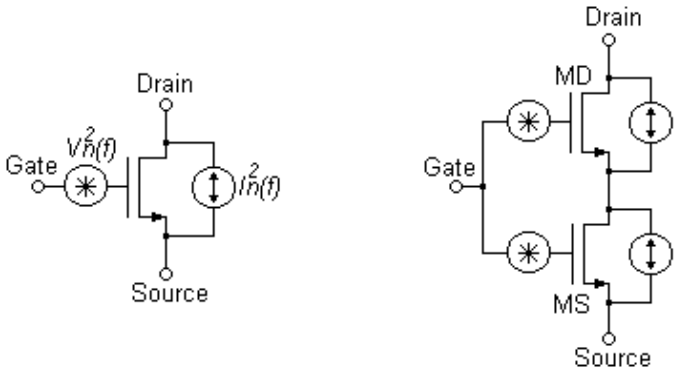
The dominant noise sources in any MOSFET transistors are flicker (*1/f*) and thermal noise (white noise) [BER79], [MIK82], [LAK94]. The flicker and thermal noise are modeled as a voltage source in series with the gate terminal and a current source in parallel with drain-to-source, respectively, as shown in Fig. 4.7a. The noise values are given, respectively, by [TSI88], [LAK94]:

$$V_n^2(f_k) = \frac{Kf}{W \cdot L \cdot C_{ox} \cdot f_k} \qquad I_n^2 = 4kT \cdot \left(\frac{2}{3}\right) \cdot g_m \text{(saturation)} \qquad 4.5.1$$

(a) (b)

where the parameter *Kf* is dependent on device characteristic, such as interface traps, fast states density, mobility variations with interface charged states, and can vary widely for

different devices in the same process. The k is the Boltszman constant, T is the absolute temperature, g_m is the transconductance and f_k is the *1/f* noise frequency corner. Important points to note here is that the flicker noise is inversely proportional to the transistor area WL and it typically dominates at low frequencies. Moreover, typically P type MOS devices have less noise than their N type devices since their majority carriers (holes) are less likely to be trapped. This important characteristic was also a decisive design parameter in the OTA design in chapter 6.



(a) (b)

FIGURE 4.7 - TAT transistor: (a) flicker and thermal noise model. (b) Noise sources.

The thermal noise expression of 4.5.1 is for the case that a MOS device is operating saturated. In this mode of operation, the channel requires integration since it is not homogenous, while in the linear region, the thermal noise is due to the channel resistance r_{ds} and it is simply given by $I_n^2(f) = \frac{4kT}{r_{ds}}$. For simplicity, the analysis will be approximated as follows: MS will be considered saturated, as far as if TAT is saturated, MS is onset to saturation (section 4.1).

In order to account the noise contribution of the TAT transistor, it is needed first quantify the noise contribution of each unit transistors associated with MD and MS, since digital-based devices are noisier. The transconductances of the MD and MS transistors are given by:

$$g_{mG_X} = \sqrt{\frac{2 \cdot \beta_X \cdot I_{D_X}}{n}} \qquad 4.5.2$$

where μ_o is effective electron mobility, and C_{ox} is gate oxide capacitance, as defined in 4.1.7. It worth noting that the transconductance of the transistor MS is smaller than transistor MD

(S_{MD} > S_{MS}). However, the transconductances of each unit transistor from MD and MS transistors are about the same order. The total drain current of TAT transistor is:

$$I_{D_{TAT}} = I_{D_{MD}} = I_{D_{MS}} = ND \cdot (I_{D_{MD}}\big|_u) = NS \cdot I_{D_{MS}}\big|_u \qquad 4.5.3$$

where the subscript *u* represent the unit transistor. Moreover, the MD and MS transistors W/L ratio are given by:

$$\left(\frac{W}{L}\right)_{MD} = ND \cdot \left(\frac{W}{L}\right)_u \qquad \left(\frac{W}{L}\right)_{MS} = NS \cdot \left(\frac{W}{L}\right)_u \qquad 4.5.4$$

hence, the transconductances of each unit transistors employed in the MD and MS transistors are given by:

$$g_{mG_X}\big|_u = \sqrt{\frac{2 \cdot b_u \cdot I_{D_X}\big|_u}{n}} = \sqrt{\frac{2 \cdot b_{MD} \cdot I_{D_X}}{n}} = \frac{g_{mG_X}}{Nu} \qquad 4.5.5$$

again, where the subscripts *u* represent unit transistor parameter and *Nu* can be ND or NS.

At this point, the total equivalent noise in TAT can be evaluated. Note that, the input voltage noise source can be referred to the output (or vice-versa) using $I_{n_{out}} = g_{mG} \cdot V_{n_{in}}$ ($I_{n_{out}}$ and $V_{n_{in}}$ is the output current and input voltage noise, respectively). Thus, the equivalent flicker noise at the input (gate) of each MD and MS transistors, shown in Fig. 4.7a, are given by:

$$V_{n_{fk}}^2\big|_X = Nu \cdot (V_{n_{fk}}^2\big|_u) \cdot (g_{m_X}^2\big|_u) = \frac{1}{Nu} \cdot V_{n_{fk}}^2\big|_u \qquad 4.5.6$$

where $V_{n_{fk}}^2\big|_u$ is flicker noise of the unit transistor. Note that, as expected, the *1/f* noise is lower for MD and MS transistor than an unit transistor by a reduction factor ND and NS, since *1/f* is inversely proportional to the gate area $ND \cdot (W \cdot L)_u$ and $NS \cdot (W \cdot L)_u$, respectively.

The same derivation can be made for the thermal noise. Then, the total equivalent thermal noise at the transistors MD and MS output $I_{n_{th}}^2\big|_X$ are expressed by:

$$I_{n_{th}}^2\big|_X = \left(\frac{8}{3}kT\right)\cdot g_{m_X} = \left(\frac{8}{3}kT\right)\cdot Nu\cdot(g_{m_X}\big|_u) = Nu\cdot\left(I_{n_{th}}^2\big|_u\right)_X \qquad 4.5.7$$

where $\left(I_{n_{th}}^2\big|_u\right)_X$ are the thermal noise of the MD and MS unit transistors, respectively, considering that MS is in saturation (ND >> NS - design oriented approximation for thermal noise for MS transistor).

It can be demonstrated that, while the (current) thermal noise density of the transistors MD and MS is, respectively ND and NS times larger, the input referred (equivalent voltage) thermal noise density is, respectively, $ND\cdot\left(g_{mG_{MD}}^2\big|_u\right)$ and $NS\cdot\left(g_{mG_{MS}}^2\big|_u\right)$ times smaller.

Therefore, the total equivalent noise referred to the input of the TAT transistor $V_{n_{TAT}}^2\big|_{in}$ can be approximated to:

$$V_{n_{TAT}}^2\big|_{in} = \left\{\frac{ND\cdot\left(g_{mG_{MD}}\big|_u\right)^2}{\left[NS\cdot\left(g_{mG_{MS}}\big|_u\right)\right]^2}+\frac{1}{NS}\right\}\cdot V_{n_{fk}}^2\big|_u + \left\{\frac{ND}{\left[NS\cdot\left(g_{mG_{MS}}\big|_u\right)\right]^2}\right\}\cdot\left(I_{n_{th}}^2\big|_u\right)_{MD} + \left\{\frac{NS}{\left[NS\cdot\left(g_{mG_{MS}}\big|_u\right)\right]^2}\right\}\cdot\left(I_{n_{th}}^2\big|_u\right)_{MS} \qquad 4.5.9$$

where the factor $NS\cdot\left(g_{mG_{MS}}\big|_u\right)$ is easily identified as the TAT transconductance $g_{m_{TAT}}$ (expression 4.3.5).

The expression 4.5.9 shows an important noise design characteristic. In the TAT transistor, each thermal and flicker noise contributions are lower than in unit transistors. Increasing TAT transconductance, the total noise is diminished, which is effectively realized increasing NS. Another very important point is that, the MD transistor is the major noise source in TAT. Hence, in order to improve (reduce) noise performance, one needs to make smaller MD transconductance and larger MS transconductance. Unfortunately, smaller MD and larger MS transconductances imply smaller ND and larger NS, respectively, which is a difficult task, since by definition *ND > NS*. Later, in next sections, will be shown that in TAT

devices the active area (W.L) is smaller than in single transistors resulting in that larger flicker noise for TATs.

Comparing previous TAT noise result with its equivalent single transistor, the total equivalent noise of the single transistor can be calculated approximately making $L_{Single} = k_1.L_u$ and $W_{Single} = k_2.W_u$, where k_1 and k_2 are constant parameter, positive and integer. Thus, the total input referred noise can be calculated related to the unit transistors of the MD and MS transistors:

$$V^2_{n_{Single}} = \frac{1}{k_1 \cdot k_2 \cdot g^2_{mG}\big|_u} \cdot \left(V^2_{n_{fk}}\big|_u\right) + \frac{\sqrt{k_1}}{g^2_{mG}\big|_u} \cdot I^2_{n_{th}}\big|_u \qquad 4.5.10$$

where $V^2_{n_{fk}}\big|_u$ and $I^2_{n_{th}}\big|_u$ are the flicker and thermal noise of an unit transistor, similar to the unit transistor of the MD and MS. Comparing the noises coefficients of 4.5.9 and 4.5.10 leads to the following important result: TAT transistor is noisier than its equivalent single transistor, that is, at low frequencies the flicker noise is larger, however the thermal noise is comparable to a single transistor.

4.6 TAT versus Single Transistors Comparisons: Simulation and Measurement

For comparison purposes, as well as investigation and validation of the TAT transistors, a number of different sizes of single (full-custom) transistors and their corresponding TAT transistor, listed in Table 4.1, were prototyped on a same silicon chip. Experimental plots for specific characteristic curves (I_DxV_D, $g_{ds}xV_D$, I_DxV_G, g_m/I_DxV_S) are depicted in Fig. A-1 for TAT-1 and Single-1; Fig. A-2 for TAT-2 and Single-2; and Fig. A-3 for TAT-3 and Single-3 (Appendix A). Moreover, Appendix A includes simulated and experimental comparisons. These comparison plots are shown in Fig. A-4 for TAT-2 *vs*. Single-2, and Fig. A-5 for TAT-3 vs. Single-3. Finally, Fig. A-6 show three experimental and three experimental *vs*. simulation g_m/I_DxV_G curve characteristics of the TATs *vs*. Singles

(TAT-1 *x* Single-1, TAT-2 *x* Single-2 and TAT-3 x Single-3) and TATs (TAT-1, TAT-2 and TAT-3), respectively.

Fig. A-1a, Fig. A-2a and Fig. A-3a are the measurement plots for the $I_D x V_D$ characteristics. The TAT measured characteristics show that the associations have larger drain current below 3V gate voltage bias than the single transistor, demonstrating the possibility of low voltage applications. The hard data plots show also that the output conductance, shown in Fig. A-1b, Fig. A-2b and Fig. A-3b, in the TAT devices is very close (or even higher, in saturation) to the single transistors, due to the cascode (self-cascode) effect.

TABLE 4.1 - Single and TAT transistors in 1.0µm digital CMOS technology.

Type	Method	W (mm)	L (mm)	W/L	ND	NS	Active Area Ratio	Area Ratio
P	Single-1	30	5	6	-	-	0.25	1.017
	TAT-1	30	-	6	12 x (2.5µm/1µm)	3 x (2.5µm/1µm)		
N	Single-2	30	5	6	-	-	0.25	1.017
	TAT-2	30	-	6	12 x (2.5µm/1µm)	3 x (2.5µm/1µm)		
N	Single-3	170	5	34	-	-	0.247	1.942
	TAT-3	168	-	33.6	16 x (10.5µm/1µm)	4 x (10.5µm/1µm)		

The linear characteristics of the devices $I_D x V_G$ are shown in Fig. A-1c, Fig. A-2c and Fig. A-3c. From the plots, it can be observed the effect of the large series resistances (section 4.2) in the TATs, that is, the drain current curves have smaller derivatives (g_m) with increasing gate voltages. Moreover, the TAT transistor is less sensible to the body effect (I_D curves are closer for each V_B) due to the presence of the middle diffusion and non-saturation of the MS transistor (sections 4.1 and 4.2). Thus, the voltage at source terminal of the MD transistor is clamped at a fraction of pinch-off voltage.

Data on the Fig. A-1d, Fig. A-2d and Fig. A-3d show a large threshold shift (less for P type TATs) from the longer channel L=5µm device to the associated TAT transistor. It is the technology shortcoming of the short channel effect. The linear region transconductance is reduced due to the series feedback and to the body effect present on MD transistor. The measurements of the characteristic $g_m/I_D x V_G$ (shown in Fig. A-6a, Fig A-6c and Fig. A-6e) demonstrate that the larger subthreshold slope and lower V_T of the TAT spread the transition

of the conduction to saturation region towards the left. This effect is due to the slow MD transition (conduction to saturation), depending on the drain voltage of the MS transistor that never saturates, but contributes to increase source terminal voltage of the MD transistor. However, the achievable g_m/I_D of the TAT is smaller (section 4.4 – equation 4.3.5) in comparison to the long channel devices.

Fig. A-1b, Fig. A-2b and Fig. A-3b compare the output conductance in strong inversion at three gate voltages, 1V, 3V and 5V (less 1V for P types), for the transistors with L=5µm and their respective TAT transistors with equivalent ratio W/L. The purpose of including the plots for 1V gate voltage is to show the low frequency noise (*1/f* - flicker) in subthreshold region. It is a consequence of the DC drain current variations (noise) even at fixed bias conditions. This drain variation is known as Random Telegraph Signal (RTS) effect [KIR89].

At higher gate voltage drive (3V and 5V) it is remarkable that the minimum-L TAT transistor achieves the same output conductance g_o in saturation region as the long channel (5µm drawn) length devices. At lower gate drive, the short channel effects of V_T reduction and Drain Induced Barrier Lowering (DIBL [TSI88]) combine to give a larger g_o both in conduction and saturation regions. The output conductance in saturated region is of the same order for the TAT with respect to its equivalent long channel at higher gate drive (V_G>3V).

The previous results demonstrate that while the output conductance is balanced in the TAT by this poor-cascode effect (section 4.3) to the equivalent single one, its driving capability and relative gain g_m/I_D can be well exploited for lower supply-voltage applications. This is particularly amenable to deeply scaled CMOS, in which transistor area is relatively inexpensive. In another vein, the behavior of the TAT at low drive is acceptable since for VLSI/ULSI a reduced supply voltage is necessary to operate the 0.15µm to 0.25µm devices in current digital CMOS technologies.

The saturation mode characteristic curves $I_D x V_S$ at same gate and drain voltage (diode mode) steps ($V_{D\text{-}G}$=0.8, 1.6, 2.4, 3.6, 4.0V) are shown in Fig. A-1e, Fig. A-2e and Fig. A-3e. The RTS effect in the subthreshod region for the single transistor is larger than in TAT-based device due to the short channel effects of the unit transistors. The experimental plots show again the drain current shift in the subthreshold region (short channel effects). Moreover, the leakage current (cut-off mode) in the TAT is smaller than in a single device. This effect is originated by the lateral and planar reverse diode effects (gate controlled diode – surface

effects [GRO67]) in MOSFET devices. The reverse diodes are the result of the junctions *np* or *pn* between diffusion implants *n+* and *p+* and substrate.

The linear matrix style arrangement of the unit transistors in the SOT array (section 3.1) have a fixed area (very small area by construction and technology constraint), shares drain and source terminals, and the gate-overlapped area of the unit transistors are less significant than in a single transistor. They are similar to the technique widely used in full-custom methodologies. A large device (very large channel width) commonly required in analog circuit is split and parallel connected (and/or interdigitized [ALE97], [ISM94]) transistors are used. The resulting effect is the reduction of the equivalent MOSFET channel drain and source area and perimeter, besides the advantage of silicon area reduction. Thus, the overall influences of the parasitic reverse diodes are minimized. In fact, the SOT array provides this advantage since a TAT transistor is a parallel association of unit transistors.

Fig. A-1f, Fig. A-2f and Fig. A-3f are plotting the ratio transconductance-current $g_m/I_D x V_S$ over all region of operation, which is helpful for analog circuit design. As expected, the ratio g_m/I_D for the TAT becomes smaller, demonstrating that at same current level a TAT achieves a lower transconductance than a single device, as shown in section 4.3 – equation 4.3.5.

Simulated and experimental comparisons were also included in this work for the N type TAT devices: TAT-2 *x* Single-2 in Fig. A-4; TAT-3 *x* Single-3 in Fig. A-5 and Figs. A-6b (TAT-1), A-6d (TAT-2) and A-6f (TAT-3). Simulated versus measured results comparison show the poor matching of the MOSFET model used by the HSpice simulator (Level 6, HSpice model with 1.0µm CMOS foundry-supplied parameters). The models level 3, 6 and 49, herein used and accessible from the foundries, do not represent the behavior of the real transistors. Observe the error magnitude on the output conductance (about 10 times) in Fig. A-4b and Fig. A-5b. There is a large disagreement on the drain current plots, shown in Fig. A-4a and Fig. A-5a. Finally, there is an over-estimated and/or non-predicted short-channel effects and body effect.

5 Implementing Analog Basic Subcircuits Using TAT Transistors

In this chapter, fundamental building blocks are designed based on g_m/I_D methodology [SIL96], [FLA97]. These blocks include a current mirror, single stage common-source amplifier with active load, track-and-latch comparator and operational transconductance amplifier (OTA) in both full-custom and SOT array methodologies. A good knowledge of these building blocks is critical to understanding many subjects of this work, and for analog IC design on any semi-custom gate arrays in general. Presently, test IC's containing these blocks, designed in 0.5µm CMOS technology, were fabricated and experimental results are presented at end of the chapter 6.

Here are also presented simulations with the purpose of validating and comparing SOT methodology using TAT transistors. Although the OTA in 1.0µm technology had been taken and designed as object of the analysis, it was discarded for the Sigma-Delta design in chapter 6. For the reason that, a higher performance and fully differential OTA is required, and technology updating has not been made. Nevertheless, a fully differential OTA in 0.5µm technology will be depicted in chapter 6.

5.1 Basic Current Mirror Technique

A simple CMOS current mirror is shown in Fig. 5.1, in which it is assumed that both transistors are under normal operation, i. e., in the saturation region. If the finite output impedances of the transistors are ignored, and it is assumed that both transistors are the same size, then M1 and M2 will have the same current since they both have the same gate-source voltage. However, when finite output impedance (non-zero output conductance) is considered,

whichever transistor has a larger drain-source voltage will also have a larger current. Additionally, the finite output impedance of the transistors will cause the small-signal output impedance of the current mirror to be less than infinite. This output impedance for single transistors is equal to $r_{ds_{M2}}$ and it is given by [ALE97], [ISM94], [TSI96]:

$$r_{ds_{M2}} = r_{o_{cm}} = \frac{1}{g_{ds_{M2}}} \qquad 5.1.1$$

where $r_{o_{cm}}$ represents the current mirror output impedance, $g_{ds_{M2}}$ is the output conductance of the M2 transistor.

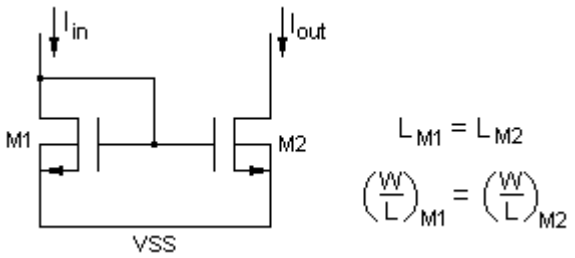


FIGURE 5.1 - CMOS current mirror, N type transistors.

The output impedance for the current mirror with TAT transistors (self-cascode in section 4.2) is given by:

$$r'_{ds_{M2'}} = r'_{o_{cm}} = \frac{1}{g'_{ds_{M2'}}} = \left\{ r_{ds_{MD}} \cdot \left[1 + r_{ds_{MS}} \cdot \left(g_{mS_{MD}} + g_{s_{MD}} \right) \right] \right\}_{M2'} \qquad 5.1.2$$

where $g_{ds_{MD}}$ is the body effect constant present on MD of the TAT transistor M2' and all variables are for the TAT transistor M2'.

Now, the current mirror output current deviation can be expressed in terms of differences on the drain voltages (in saturation) of the transistors and output impedance as follows:

$$\Delta I_{out} = \frac{\Delta V_{D_{M2}}}{r_{ds_{M2}}} \qquad 5.1.3$$

TABLE 5.1 - Single and TAT transistors examples for the current mirrors. CMOS technology at 1.0µm and 0.5µm (prime superscripts indicate TAT version).

					Transistor sizes	
Tech.	**Transistor**	**W(µm)**	**L(µm)**	**W/L**	**ND**	**NS**
1.0µm	M1-M2	84	3.0	28	-	-
	M1'-M2'	84	3.0	28	8x(10.5µm/1µm)	4x(10.5µm/1µm)
0.5µm	M1-M2	106	1.9	55.86	-	-
	M1'-M2'	106	1.9	55.86	20x(5.4µm/0.6µm)	9x(5.4µm/0.6µm)

TABLE 5.2 - Simulated mismatching in current mirrors (N-FET type), for 1.0µm and 0.5µm CMOS technology (prime superscripts indicate TAT version).

Technology	**Transistor**	I_{in} (mA)	$\mathbf{I_{out}}$ **(mA)**	**Mismatch (%)**
1.0µm	M1	0.1000	0.1030	+3.0
	M1'		0.1017	+1.7
0.5µm	M1	0.6000	0.5490	-8.5
	M1'		0.6000	0.0

The current mirroring technique above analyzed using both single and TAT transistors in both 1.0µm and 0.5µm CMOS technology have been performed throughout electrical simulations. The transistors were designed by means of the devices listed in Table 5.1. It has been demonstrated that the current mirroring mismatch is larger in 1.0µm technology.

On the other hand, the TAT version has presented better current matching, showing the predicted improvement on the output conductance. These simulation results are summarized in Table 5.2. The experimental investigations (chapter 6) were performed in order to confirm previous simulations and layout effects on the test-chips in 0.5µm technology.

5.2 Basic Single-Stage Common-Source Amplifier

A way to examine the performance of a circuit using a single TAT is the single stage common-source (CS) amplifier. This basic amplifier has been designed with a PMOS current source as the active load, as shown in Fig. 5.2a. A P-type transistor is used as an active load to supply the bias current for the drive transistor. By using an active load, a high-impedance output load can be realized without using excessively large resistors or large power supply voltages.

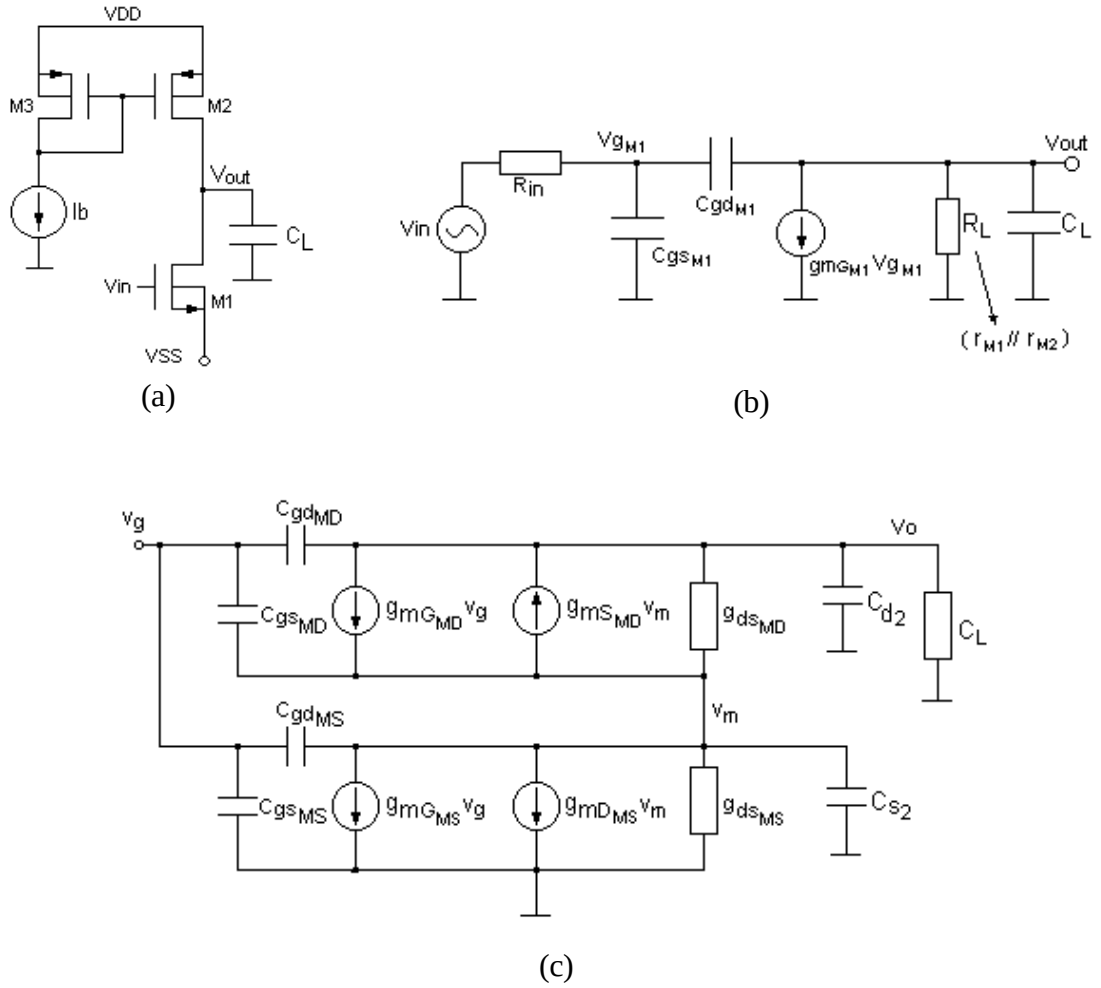


FIGURE 5.2 - (a) Single-stage CS amplifier with PMOS type current source. (b) Small-signal model for single version. (c) Small-signal model for TAT version.

A small-signal equivalent circuit for high-frequency analysis of the common-source amplifier is shown in Fig. 5.2b. In the figure, C_L concentrates drain-bulk capacitances of M1

and M2, any parasitic capacitances may have at output node and load capacitor, where typically, C_L dominates. Analyzing the circuit at high frequencies, the common-source amplifier gain is given by [LAK94], [TSI96], [JOH97]:

$$A_V(s) = \frac{v_{out}}{v_{in}} = \frac{-g_{m_{M1}} \cdot R_L \cdot \left(1 - s\frac{C_{gd_{M1}}}{g_{m_{M1}}}\right)}{1 + as + bs^2} \qquad 5.2.1$$

where R_{in} represents the output impedance of input voltage source, R_L is the parallel combination of the output impedances of M1 and M2 transistors, and the coefficients *a* and *b* are given by:

$$a = R_{in} \cdot \left[C_{gs_{M1}} + C_{gd_{M1}} \cdot \left(1 + g_{m_{M1}} \cdot R_L\right)\right] + R_L \cdot \left(C_{gd_{M1}} + C_L\right) \qquad 5.2.2$$

$$b = R_{in} \cdot R_L \cdot \left(C_{gd_{M1}} \cdot C_{gs_{M1}} + C_{gs_{M1}} \cdot C_L + C_{gd_{M1}} \cdot C_L\right) \qquad 5.2.3$$

After some simplifications, the gain can be approximated by the following expression:

$$A_V(s) \cong \frac{-g_{m_{M1}} \cdot R_L}{1 + s\left\{R_{in} \cdot \left[C_{gs_{M1}} + C_{gd_{M1}} \cdot \left(1 + g_{m_{M1}} \cdot R_L\right)\right] + R_L \cdot \left(C_{gd_{M1}} + C_L\right)\right\}} \qquad 5.2.4$$

and the dominant pole (at -3db frequency) is given by:

$$\omega_p \cong \frac{1}{R_{in} \cdot \left[C_{gs_{M1}} + C_{gd_{M1}} \cdot \left(1 + g_{m_{M1}} \cdot R_L\right) + R_L \cdot \left(C_{gd_{M1}} + C_L\right)\right]} \qquad 5.2.5$$

The DC gain of common-source amplifier is given by the expression 5.2.4 at low frequencies, that is: $A_{Vo} = -g_{m_{M1}} \cdot R_L$ (R_L indicated in Fig. 5.2b). As well-known, depending on the device sizes, currents, and the technology used, a typical gain for this circuit is in the range of -10 and -100 [ALE97], [LAK94].

TABLE 5.3 - Designed size for Amplif-1 and Amplif-2 (prime superscripts indicate TAT version).

Amplif-1: AMP_S1 (single) and AMP_T1 (TAT) - 1.0mm CMOS technology							
Xtor	**W (mm)**	**L (mm)**	**W/L**	**ND**	**NS**	**Active Area Ratio**	**Area Ratio**
M1	84	3	28	-	-	0.5	1.271
M1'	84	-	28	8x (10.5µm/1µm)	4x (10.5µm/1µm)		
M2-M3	180	3	60	-	-	0.5	1.451
M2'-M3'	180	-	60	8x (22.5µm/1µm)	4x (22.5µm/1µm)		

Amplif-2: AMP_S2 (single) and AMP_T2 (TAT) - 0.5mm CMOS technology							
Xtor	**W (mm)**	**L (mm)**	**W/L**	**ND**	**NS**	**Active Area Ratio**	**Area Ratio**
M1	106	1.9	55.8	-	-	0.46	1.431
M1'	106	1.9	55.8	20x (5.4µm/0.6µm)	9x (5.4µm/0.6µm)		
M2-M3	191	1.7	112.3	-	-	0.54	1.515
M2'-M3'	191	1.7	112.3	16x (11.7µm/0.6µm)	9x (11.7µm/0.6µm)		

TABLE 5.4 - Simulated total harmonic distortion in Amplif-1 and Amplif-2 for 1.0µm and 0.5µm CMOS technology.

Amplifier	**Total Harmonic Distortion (%) @ $2V_{p\text{-}p}$**
AMP_S1	3.975
AMP_T1	3.458
AMP_S2	4.555
AMP_T2	2.814

The same analysis can be realized with TAT transistors, using the equivalent TAT as a single device M1. However, intermediate node pole will not be accounted and a direct TAT version small-signal modeling analysis is not simple. Hence, the zero-value time-constant analysis method [JOH97] can be employed in order to estimate the dominant pole of the TAT system amplifier. Consider the amplifier small-signal model of the TAT version shown in Fig 5.2c. The concentrated capacitances C_{d1} and C_{S2} are given by:

$$C_{d2} = C_{db_{MD}} + C_L + C_{mir} \qquad 5.2.6a$$

$$C_{S2} = C_{db_{MS}} + C_{sb_{MD}} \qquad 5.2.6b$$

where C_{mir} is the total capacitances at current mirror output (drain of the TAT equivalent M2 in Fig. 5.2a). The estimated dominant pole of the system amplifier using TAT devices, after some tedious calculations, is given by:

$$w_P \cong \frac{1}{R_{in} \cdot \left[C_{gs_{MS}} + C_{gd_{MD}} + g_{mG_{MS}} \cdot R_2 \cdot \left(C_{gd_{MS}} + C_{gs_{MD}}\right)\right] + \left(C_{gd_{MD}} + C_{d2}\right) \cdot R_1 + C_{S2} \cdot R_2} \qquad 5.2.7$$

where the resistances R_1 and R_2 are given by:

$$R_1 = r_{ds_{MS}} \cdot r_{ds_{MD}} \cdot g_{mS_{MD}} \qquad 5.2.8a$$

$$R_2 = \frac{1}{g_{ds_{MS}} + \dfrac{g_{mS_{MD}} \cdot r_{ds_{MD}} + 1}{R_L}} \qquad 5.2.8b$$

The DC gain is effortless found with the output conductance and transconductance of the TAT from the equations 4.3.3 and 4.3.5 (or 4.3.4), respectively. The result is simply given by ($R_L = \infty$):

$$A_{Vo_{TAT}} \cong -r_{ds_{MD}} \cdot \left[\frac{g_{mG_{MD}} \cdot g_{mD_{MS}}}{g_{mD_{MS}} - g_{mS_{MD}}} + \frac{g_{mG_{MD}} \cdot g_{mS_{MD}}}{g_{ds_{MS}} + g_{mD_{MS}}}\right] \cong$$

$$\cong -g_{mG_{MS}} \cdot g_{mG_{MD}} \cdot r_{ds_{MS}} \cdot r_{ds_{MD}} \qquad 5.2.9$$

Table 5.3 lists the transistors size designed for both Amplif-1 and Amplif-2 in 0.5μm CMOS technology. The AMP_S1 and AMP_S2 are the full-custom versions and AMP_T1 and AMP_T2 are their equivalent TAT versions. Note the number of minimum-L transistors employed in the TAT versions in comparison to their equivalent full-custom ones. While there are only 3 devices in the full-custom, in the TAT versions have 24 (AMP_T1) and 54 (AMP_T2) transistors.

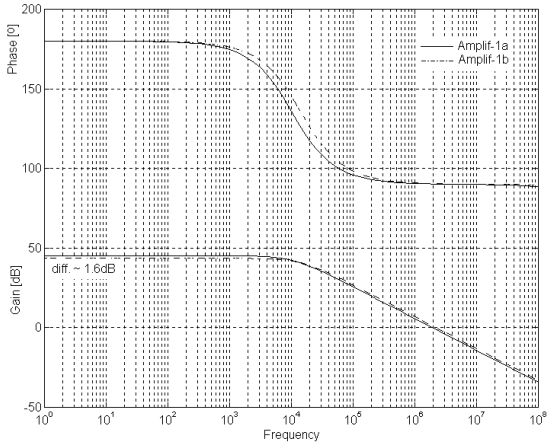


Figure 5.3

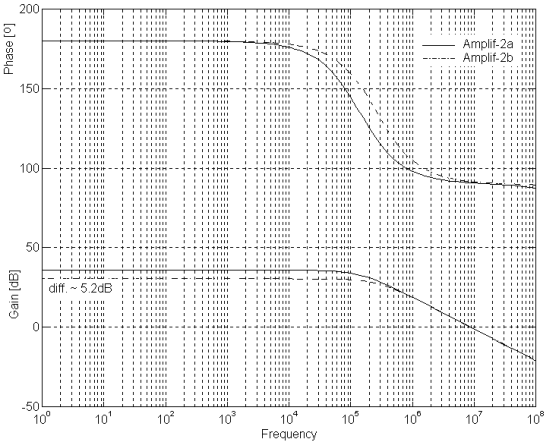


Figure 5.4

FIGURE 5.3 - (a) CS Amplif-1: gain and phase margin. Electrical simulation (HSpice, level 6) for 1.0µm CMOS technology. AMP_T1 (dotted) and AMP_S1 (solid). $(W/L)_{eq}$=84/3.0.

FIGURE 5.4 - CS Amplif-2: gain and phase margin. Electrical simulation (HSpice level 49) for 0.5µm CMOS technology. AMP_T2 (dotted) and AMP_S2 (solid). $(W/L)_{eq}$=106/1.9.

The simulated plots are shown in Fig. 5.3 and 5.4 [CHO2000b]. As expected, the TAT versions are working as an approximation to the cascode amplifier (as a self-cascode). The gain and phase are almost the same compared to the full-custom. The results demonstrated that the TAT output conductance is similar to the traditional cascode $g_{o_{TAT}} = \frac{g_{ds_{MD}} \cdot g_{ds_{MS}}}{g_{mS_{MD}}}$.

While in the traditional cascode stages, the top MD transistor output conductance is set at lower values (by convenient design of W/L), in the TAT version, MD is larger (trapezoidal) than MS, leading to high output conductance level for MD. The result is:

$$g_{o_{TAT\_satge}} > g_{o_{Cascode\_stage}} \qquad 5.2.10$$

Furthermore, in saturation mode the transconductance (proportional to square root of I_D) is higher than in conduction mode (directly proportional to V_{DS}). Thus, as the MS transistor is always in conduction, its transconductance $g_{mG_{MS}}$ is not much higher value, since it is directly proportional to the middle voltage V_m. The resulting performance is that the amplifier gain of the TAT version is the averaging resultants of the previous effects, which contribute to be comparable to the full-custom amplifier.

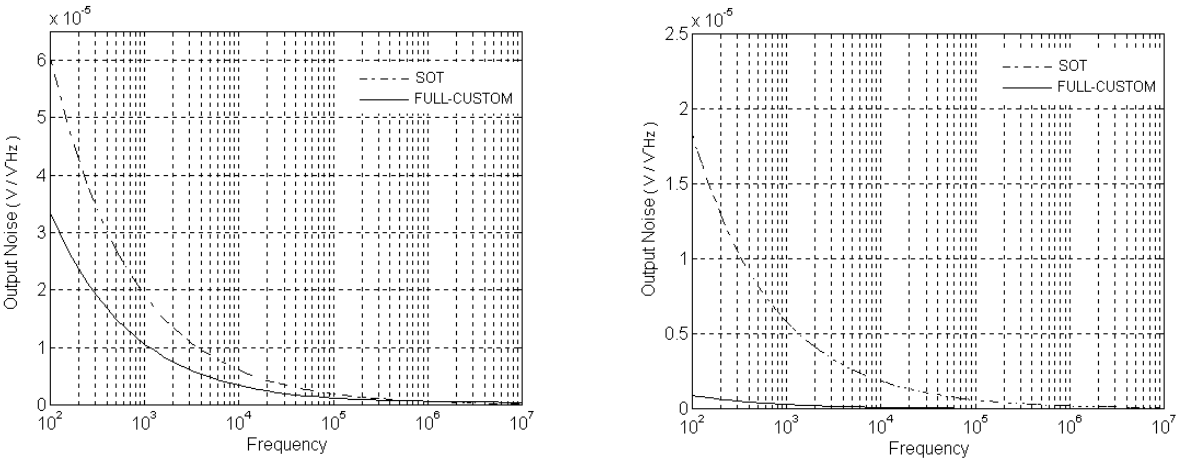


FIGURE 5.5 - Simulated output noise power spectrum for CS amplifiers (HSpice, levels 6 and 49). TAT (dotted) and single (solid) version. (a) Amplif-1 (1.0µm). (b) Amplif-2 (0.5µm).

The bandwidth is also not degraded by the additional intermediate node *m* (Fig. 3.3). The transistors MD and MS capacitances combination are of the same order of a single transistor. The gate-to-source capacitance of MS device is smaller compared to a single device, since MS width is smaller.

The total harmonic distortions and noise simulations are also addressed. Simulated total harmonic distortions, shown in Table 5.4, have shown better (smaller) in the TAT than in the single transistors. They were sized at exactly the same equivalent W/L ratio, L and W. It proves the better linearity for TAT versions. The simulated noises power, shown in Fig. 5.5a and 5.5b, are larger for the 1.0µm technology, compared to the 0.5µm technology common-source amplifiers. The reasons are that a larger number of unit transistors is employed in AMP_T1 than in AMP_T2, and the total gate capacitance is larger for the 0.5µm amplifiers [BER79]. The thermal noise in the circuit amplifiers, Amplif-1 (1.0µm) and Amplif-2 (0.5µm), is very low, as expected (section 4.4).

The flicker noise coefficient value *Kf*, required in the Spice model, was estimated since the KF spice coefficient in level 3, 6 and 49 (Bsim3) from the foundries is not available. To facilitate the realization of the noise simulations, an averaging and approximation of the coefficient values (coefficients that usually are real values for MOS transistors) were adopted. For comparison purposes, it is acceptable. Thus, the noise simulations presented here do not reflect the absolute noise performance, to be expected from fabricated devices.

5.3 Track-and-Latch Comparator

A comparator executes two important tasks in one-bit Sigma-Delta modulator: comparison, binary quantization adjusting the modulator output to a digital logic level. In order to guarantee a good global performance of the Sigma-Delta modulator, a comparator ought to offer high speed, low offset, low power consumption and reasonable output signal swing. The latter can be regulated by a level converter, such as a Set-Reset type latch.

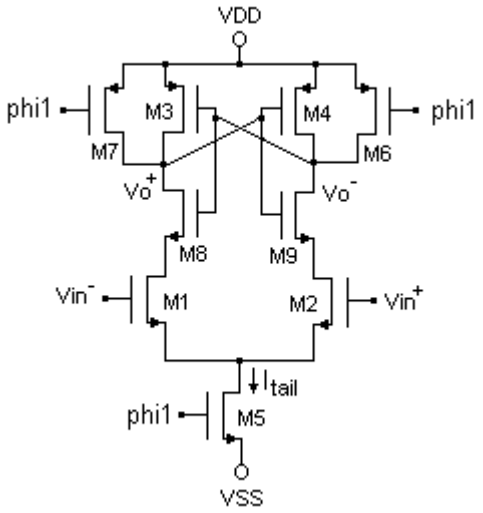
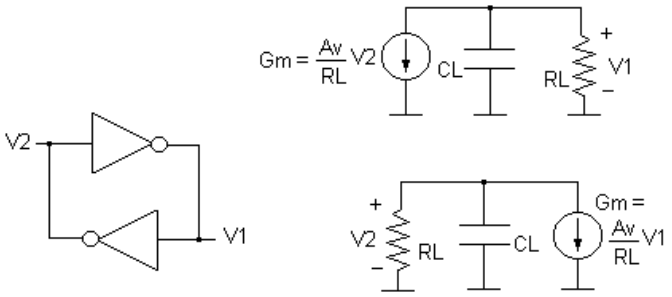


FIGURE 5.6 - Track-and-Latch comparator.

The track-and-latch comparator [CHO94], depicted in Fig. 5.6, is structured by the input differential drivers M1-M2, inverters M3-M8 and M4-M9 in positive feedback configuration, equalizer/pre-charger transistors M6-M7, and by the current source controlled (*phi1*) M5. In an instant before active semi-cycle *phi1*, the input signals V_{in}+ and V_{in}- have to be defined and stabilized to facilitate the regenerative comparison. Then, initiating at rising edge of the clock *phi1*, one of the outputs moves fast, except for a small delay, toward the lowest power supply, V_{SS} or ground. Both output nodes have been pre-charged to the V_{DD} in the equalization/pre-charge phase (inactive semi-cycle clock) in order to speed up the regenerative comparison. That is, throughout the inactive semi-cycle period, the current of M5 (I_{tail}) is turned off and input drivers and regenerative latch are reset and pre-charged to V_{DD}. The speed of this type of comparator is strongly dependent on the I_{tail} current, that is, speed is directly proportional to the current: increasing it, the speed increases [CHO94].

The time constant of the track-and-latch in latch mode, i. e., when in positive feedback phase, can be calculated by a simply structure consisting of two inverters as basic latch, illustrated in Fig. 5.7a [JOH97]. Consider that both output voltages are close to each other at the beginning of the latch phase and the inverters are in their linear range. Then each of the inverters can be modeled as a voltage-controlled current source driving a RC load, shown in Fig. 5.7b.



(a) (b)

FIGURE 5.7 - (a) Basic latch with two inverters. (b) A linearized model of the track-and-latch comparator in latch mode.

In Fig. 5.7b, the A_v is the low frequency gain of the inverters and the model for simplicity is linearized. Then, the time constant is given by [JOH97]:

$$t_{latch} = KA \cdot \frac{L^2}{m_n \cdot V_P} \qquad 5.3.1$$

where L is the channel length of the inverters, m_n is the NMOS transistor mobility, and KA is an independent constant (varies between 2 and 4). This expression is very useful in determining a rough estimate for the maximum clock frequency. The time constant is mostly affected by technology parameters (not controlled by design, such as minimum-L, V_P and C_L).

Finally, considering the voltage logic difference required to be recognized by succeeding digital circuit, the time necessary for latching is given by [JOH97]:

$$T_{latch} = \frac{C_L}{G_m} \cdot \ln\left(\frac{\Delta V_{logic}}{\Delta V_0}\right) = KA \cdot \frac{L^2}{m_n \cdot V_P} \cdot \ln\left(\frac{\Delta V_{logic}}{\Delta V_0}\right) \qquad 5.3.2$$

where, DV_{logic} is the logic voltage difference desired and DV_0 is the input voltage difference needed for comparison at the beginning of the latch phase. The well-known meta-stability can occur when DV_0 is very small and even in the case it is not (large enough), because of the presence of the circuit noise.

TABLE 5.5 - Designed single and TAT transistor sizes for the Comparator in both full-custom and SOT array (prime superscripts indicate TAT version).

Track-and-Latch Comparator (0.5µm CMOS technology)					
Transistor	**W(µm)**	**L(µm)**	**W/L**	**ND**	**NS**
M1-M2	72	1.2	60	-	-
M1'-M2'	108	-	60	20x(5.4µm/0.6µm)	10x(5.4µm/0.6µm)
M8-M9	30	0.6	50	-	-
M8'-M9'	32.4	-	54	6x(5.4µm/0.6µm)	-
M5	10	15	0.67	-	-
M5'	1.2	-	2	1x(1.2µm/0.6µm)	-
M3-M4	20	0.6	33.33	-	-
M3'-M4'	23.4	-		2x(11.7µm/0.6µm)	-
M6-M7	2.5	0.6	4.2	-	-
M6'-M7'	2.4	-	4	2x(1.2µm/0.6µm)	-

In this comparator design, the main concerns were the speed and power consumption as long as sensibility (offset voltage) and gain are reasonably uncomplicated achievable. Once the desired frequency of operation is reached, the power consumption is settled by the current I_{tail}. If it does not meet the specifications, it is re-done iteratively by changing simultaneously the width W of M1-M2, M3-M8 and M4-M9 [CHO94], until the desired performance is achieved, always checking the frequency defined in 5.3.2.

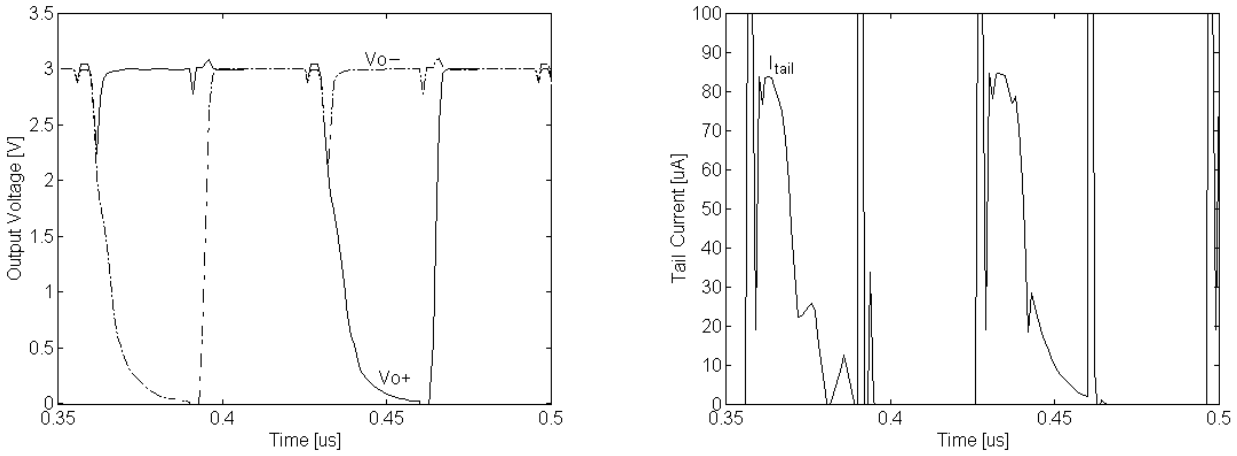
Designed transistor sizes (single) and association (TAT) of the track-and-latch comparator for both full-custom and SOT array methodology are summarized in Table 5.5. The full-custom comparator includes 28 single transistors and for its equivalent SOT version 41 unit transistors are used. Note that, the SOT version uses only the TAT transistors for the differential input pair (M1 and M2), because the others are only digital transistors. Thus, for the remaining devices the conversion process is only associating in parallel in order to get the desired equivalent width W using unit transistors available in the array.

TABLE 5.6 - Simulated comparator performance in 0.5µm CMOS technology.

	Design Methodology	
	Full-Custom	**SOT**
V_{DD} (V)	3	3
C_L (pF)	10	10
f_{max} (MHz)	70	40
Diff. Sensibility *DVin* (mV)	10	18
P_{diss} (mW) @ 14.3MHz	0.1	0.13
I_{tail} (mA)	~ 84	~ 93

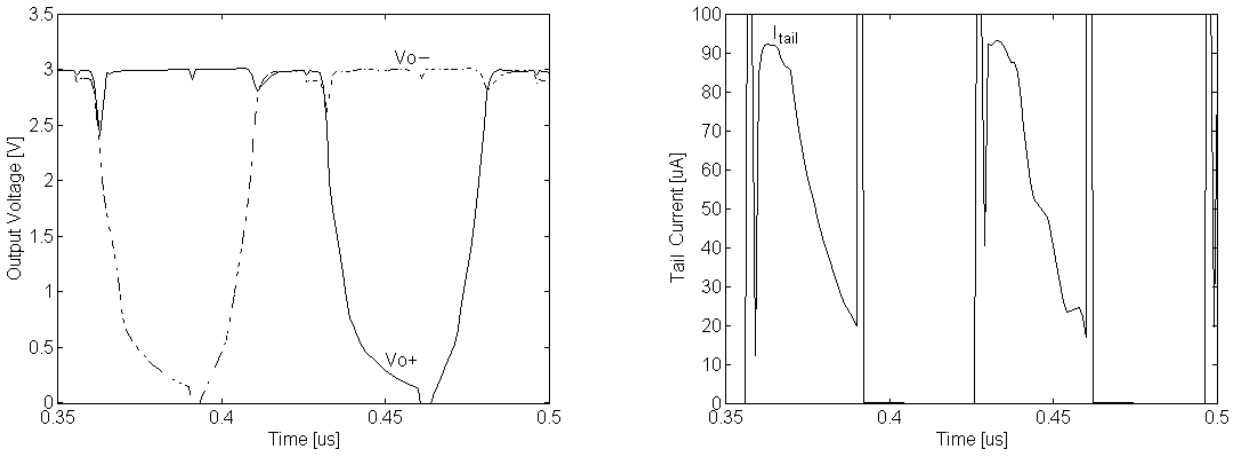
The plots in Fig. 5.8a, Fig .5.8b, Fig. 5.9a and Fig. 5.9b show the simulated comparator in full-custom and SOT array versions. Note the equalization phases described before, where both output are first equalized, then pre-charged to the V_{DD} and one of the output moving fast toward the lower supply rail. Moreover, standby current (period of *phi1* inactive semi-cycle) is near zero. Indeed, power consumption is very low in this type of comparator because currents just flow over the circuit in the semi-period preceding the latch mode.

Table 5.6 shows the simulated performance results. It is comparing the same comparator (described previously) in both full-custom (single transistors) and SOT array version using TAT transistors. The SOT version has shown similar performance to the full-custom design, except for the lower f_{max} and larger differential input sensibility (DV_{in}). The reason is that the comparator maximum frequency is strongly dependent on the current tail (I_{tail}) that feeds the differential pair and by the approximations realized in TAT transistors assembling, which are clear in Table 5.6. This comparator was fabricated (full-custom and SOT array) in 0.5µm CMOS technology from MOSIS foundry. The experimental results are in the chapter 6.



(a) (b)

FIGURE 5.8 - Simulated comparator performance (HSpice, level 49). Full-custom version for 0.5µm CMOS technology. (a) Output voltages Vo+ and Vo−. (b) Switched tail current in M5 transistor.



(a) (b)

FIGURE 5.9 - Simulated comparator performance (HSpice, level 49). SOT array version for 0.5µm CMOS technology. (a) Output voltages Vo+ and Vo−. (b) Switched tail current in M5 transistor.

5.4 CMOS Operational Transconductance Amplifier

The OTA shown in Fig. 5.10 is a differential-input single-ended output. It also has been implemented in full-custom [CHO97] and SOT array [CHO99c], [CHO2000b] methodologies in 1.0µm CMOS technology, in order to investigate the SOT version performance and TAT validation. This applicable folded-cascode OTA, here in analysis, had been extensively analyzed and designed previously in [CHO94]. Report this work for more design details.

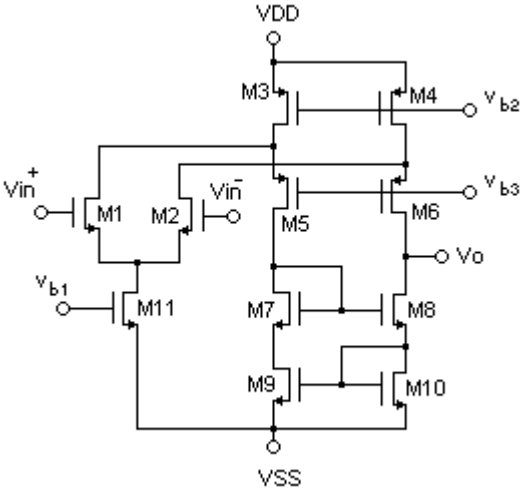


FIGURE 5.10 - Folded-cascode single-ended OTA.

The gain in folded-cascode OTAs is determined by mainly the input transconductance differential pair and is given by [ALE97], [LAK94], [JOH97]:

$$A_V(s) = \frac{g_{mG_{M1}} \cdot z_{out}}{1 + s(z_{out} \cdot C_L)} \qquad 5.4.1$$

where z_{out} is the output impedance of the OTA. Usually, this impedance is very high, on the order of $\frac{g_m}{2g_{ds}^2}$ or greater if output impedance enhancement is used other than designed in this OTA, for example a wide swing cascode current mirrors [JOH97].

For mid-band and high frequencies, the load capacitance dominates, and the expression 5.4.1 can be approximated as follows:

$$A_V(s) = \frac{g_{mG_{M1}}}{sC_L} \tag{5.4.2}$$

from which the unit-gain frequency (gain-bandwidth) of the OTA is found to be:

$$w_{unit-gain} = \frac{g_{mG_{M1}}}{C_L} = \frac{\frac{2 \cdot I_{D_{M1}}}{n \cdot V_{P_{M1}}}}{C_L} = \frac{2 \cdot I_{D_{M1}}}{n \cdot V_{P_{M1}} \cdot C_L} \tag{5.4.3}$$

Therefore, for large load capacitances, maximizing the transconductance of the input-differential pair (M1 and M2) maximizes the bandwidth, assuming the load capacitor is large enough so that unit-frequency is much less than the limit imposed by the second poles. The input transistors transconductance can be maximized by widen channel width devices, and ensuring that the bias current of the input pair (I_{M11}) is substantially larger than the bias current of the cascode transistors (M5-M6) and current mirrors (M7-M8 and M9-M10). In this approach, the DC gain also can be increased maximizing output impedance z_{out} (or decreasing output conductance). It can be done by biasing at lower current levels (for a given total power consumption) on all transistors connected to the output node.

A practical upper limit on the ratio between the bias currents of the input transistors and the currents of the cascode transistors might be around four times. If too high a ratio is used, the bias currents of the cascode transistors can not be well established since they are derived by current subtractions. Another advantage of having very large transconductances for the input devices is that the thermal noise due to this input pair is reduced. Thus, since much of the bias current in folded-cascode OTAs flows through the input differential pair, these OTAs often will have better thermal noise performance than other having same power dissipation.

Another important design parameter is the settling behavior of the OTAs, that is, slew rate. It is defined as the maximum rate at which the output changes when input signals are large and its expression is:

$$SR \equiv \frac{dV_{out}}{dt}\Big|_{\max} = \frac{I_{D_{M11}}}{C_L} = \frac{2 \cdot I_{D_{M1}}}{C_L} \tag{5.4.4}$$

Substituting the expression 5.4.3 into 5.4.4 and using the expression for the transconductance in saturation (remind that $g_m = (2 \cdot I_D)/(n \cdot V_P)$), another relationship for *SR* is now given by:

$$SR = \frac{2 \cdot I_{D_{M1}}}{\frac{2 \cdot I_{D_{M1}}}{n \cdot V_{P_{M1}}}} \cdot w_{unit-gain} = n \cdot V_{P_{M1}} \cdot w_{unit-gain} \qquad 5.4.5$$

From the above expression, it is obvious that in order to achieve a high slew rate and high GBW a P type transistor as the input differential pair is preferable rather than N type channel device. Saturation voltage for NMOS transistor $V_{D_{sat}}$ is higher than in PMOS devices because of PMOS threshold V_T is higher than for NMOS devices. Moreover, decreasing $V_{D_{sat}}$ increases the transconductance of the input stage. Although increasing $V_{D_{sat}}$ helps to minimize distortion, a lower transconductance in the first stage decreases the DC gain and increases the equivalent input thermal noise [ALE97], [JOH97].

Concerning the power consumption in OTA, there is a trade-off between standby current and desired SR. The low power in OTAs means, at least, low standby current, which is defined by tail current (M11) and current sources (M3 and M4), that bias input differential pair and the cascode branch, respectively. Nonetheless, the achievement of a good slew rate OTA with low current driving capability is not simple. It is required the use of a specific circuit configuration, such as class AB stages or a good design trade-off evolving SR and low power dissipation.

The transconductance of the differential pair can be increased by either increasing the aspect ratios of the transistors M1 and M2 or the tail current. On the other hand, the maximum available current from a differential pair can not exceed the tail current. The standby power consumption is related to the load capacitance and the desired slew rate by:

$$P_{diss} = V_{DD} \cdot C_L \cdot (SR) \cdot k_{OTA} \qquad 5.4.6$$

where k_{OTA} is a factor related to the type of OTA. For this OTA in particular (or for fully differential OTAs) this factor is 4. It is obvious that for high-speed switched-capacitor circuits (for example) this type of OTA, without any improvement technique, dissipates a large

standby power, particularly when driving a large load capacitor. Although, power consumption is the major concern in designing fully differential OTA in chapter 6, in this particular OTA it is not, since in that time the design focused only gain, speed and settling time.

In this type of OTA, the contribution of cascaded transistors to degenerate the input offset voltage and input-referred noise voltage is larger than in others. One must take care on the input pair M1-M2 for matching and between the pairs formed by M3-M4, M5-M6, M7-M8 and M9-M10 in order to minimize the input offset voltage. Additionally, if the transistors M7 to M10 are biased at the same current as the input devices, the input-referred flicker noise can be shown to be:

$$v_{eq\,fk}^2 = \frac{2\,Kf_n}{L_{M1}\cdot W_{M1}}\left[1+\frac{2\,Kf_p\cdot m_p}{Kf_n\cdot m_n}\left(\frac{L_{M1}}{L_{M4}}\right)^2+\left(\frac{L_{M1}}{L_{M10}}\right)^2\right]\cdot\frac{1}{f} \qquad 5.4.7$$

where Kf_n and Kf_p are the flicker noise coefficients for the NMOS and PMOS devices, respectively. From the above expression, it is obvious that by increasing channel lengths of the current sources M3-M4 and the input differential-pair area, flicker noise can be minimized [BER79].

Employing TATs instead of single transistors to this analysis, expression 5.4.1 at first moment makes obvious that the TAT version presents DC gain higher than the equivalent full-custom one. Experimentally, it is not always true because the transconductance for a TAT has a lower value than for its equivalent single transistor (chapter 4 – section 4.2). Hence, there is a compensation between the behavior of the two terms – tranconductance and output impedance – which set the DC gain, since output conductance in TAT is almost the same or higher compared to the equivalent single one (Chapter 4 – section 4.2). As a consequence, it is natural the slew rate (*SR*) for a TAT version to be lower in view of the fact that the dominant pole is lower than for a single one (under the same DC conditions for both).

With the purpose to investigate the previous analysis using TAT transistors, the OTA illustrated in Fig. 5.10 has been designed and implemented in both full-custom and SOT array methodology. The designed geometries W's, L's and W/L's of the OTA transistors are summarized in Table 5.7. Note that SOT version contains 100 unit transistors. The layouts and die photos of the folded-cascode OTA are shown in Fig. 5.11 and Fig. 5.12, respectively.

Table 5.8 shows different results and performances comparison from electrical simulations (for C_L=10pF) and experimental measurements.

TABLE 5.7 - Designed single and TAT transistor sizes for the OTA in full-custom and SOT array methodology (prime superscripts indicate TAT version).

Folded-Cascode OTA – 1.0mm CMOS technology							
Xtor	**W (µm)**	**L (µm)**	**W/L**	**ND**	**NS**	**Active Area Ratio**	**Area Ratio**
M1-M2	170	5	34	-	-	0.247	1.942
M1'-M2'	168	-	33.6	16x (10.5µm/1µm)	4x (10.5µm/1µm)		
M3-M4	63	10	6.3	-	-	0.095	1.883
M3'-M4'	52.5	-	6.6	21x (2.5µm/1µm)	3x (2.5µm/1µm)		
M5-M6	57	10	5.7	-	-	0.25	1.017
M5'-M6'	30	-	6	12x (2.5µm/1µm)	3x (2.5µm/1µm)		
M7-M8	42	10	4.2	-	-	0.113	1.585
M7'-M8'	42.5	-	4.5	17x (2.5µm/1µm)	2x (2.5µm/1µm)		
M9-M10	42	10	4.2	-	-	0.113	1.585
M9'-M10'	42.5	-	4.5	17x (2.5µm/1µm)	2x (2.5µm/1µm)		
M11	15	10	1.5	-	-	0.05	3.049
M11'	5	-	1.7	2x (2.5µm/1µm)	1x (2.5µm/1µm)		

From measured data, it is clear that, the OTA in SOT version has similar DC gain, while simulations (shown in Fig. 5.11a) have demonstrated higher gains but similar values. Additionally, SOT version has higher bandwidth (GBW normalized at C_L=50pF) accordingly to the simulations, as larger as almost 1.8 times. Measured slew-rates are very closer to the simulation results (see Fig. 5.11b), however SR performances of the OTAs are very low due to the low tail current (M11). The offset voltage in SOT version is smaller than in full-custom version, demonstrating the better matching due to good intrinsic layout pattern. That is, naturally TAT transistors are very similar to the interdigitizing technique, which is widely used in full-custom layout design (section 2.4).

TABLE 5.8 - Experimental and Simulated OTAs performance in 1.0μm digital CMOS technology (GBW_{NZ}=Normalized).

	Simulation		Measurement	
	Full-custom	SOT	Full-custom	SOT
Supply Voltages (V)	±2.5	±2.5	±2.5	±2.5
A_V (db)	106	92.4	64.5	62.9
GBW(MHz) @ C_L(pF)	4.5 / 10	7.7 / 10	0.186 / 82.4	0.514 / 53.5
GBW_{NZ} (MHz) @ C_L=50pF	0.9	1.54	0.307	0.550
SR (V/μs) @ C_L(pF)	3.46 / 10	5.89 / 10	0.42 / 82.4	1.10 / 53.5
PM (^{o})	80	76.2	79.4	51.7
$\|V_{os}\|$ (mV)	24	0.83	30	15
$V_{o\ max}$(V)	+2.2 / -1.3	+1.6 / -1.4	+1.1 / -0.7	+0.9 / -0.9
P_{diss} (mW)	0.50	2.78	0.87	1.38
SNR(dB) @ 500KHz/1MHz	-	-	99.1 / 97.9	94.1 / 92.8
THD (%)	-	-	5.9	9.8

Attempt to the power consumption for both versions. The measured results are almost in agreement to the theory (expression 5.4.6) and an important disadvantage for the SOT approach is the higher power consumption in comparison to the full-custom version. Then, the importance of the single-to-TAT transistors assembling process (section 3.3), since the bias currents in SOT versions might be larger.

The load capacitances for measurement column in Table 5.8 are estimated values from the output currents that are expected at nominal C_L. and measured slew-rates of unknown real capacitances at the chip targeted output pin. Hence, estimated C_L can be expressed by:

$$C_{L_{estim}} = \frac{I_{o_{sim}}}{SR_{meas}} = \frac{SR_{sim} \cdot C_{L_{nom}}}{SR_{meas}} = C_{L_{nom}} \cdot \frac{SR_{sim}}{SR_{meas}} \qquad 5.4.8$$

Higher estimated load capacitances are due mostly to the parasitic capacitances present in the chip packages and cables from the measurement devices. It explains partly the measured low bandwidth in the OTAs. It is worth noting that the OTA with TAT transistors has similar (or higher) gain-bandwidth product. Indeed, it is expected since the TAT transistor act like a cascode stage (self-cascode – section 4.2).

TABLE 5.9 - Measured noise performance. Several test-IC samples containing folded-cascode OTA in 1.0µm CMOS technology. (a) Full-custom version. (b) SOT array version.

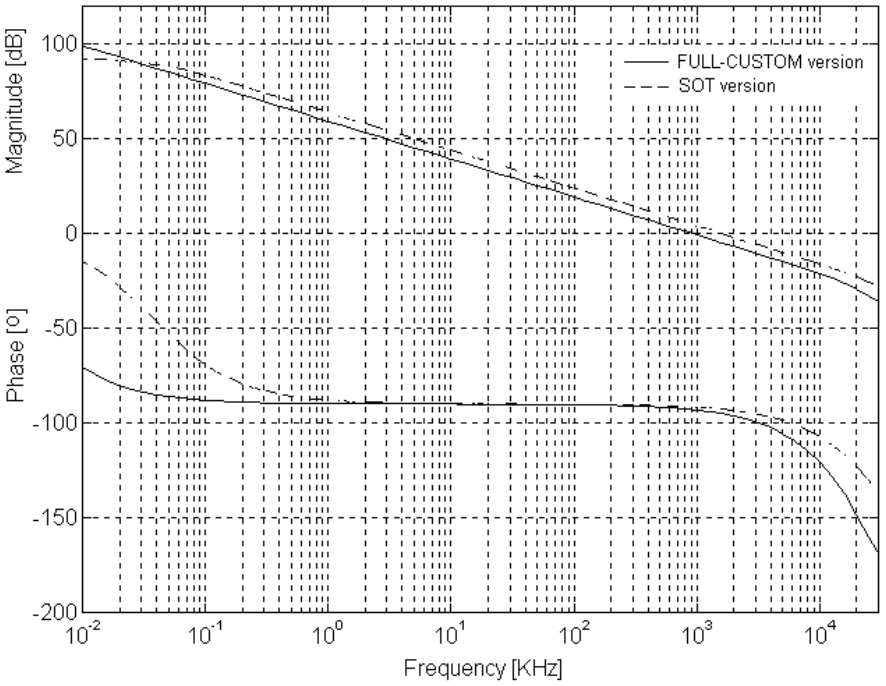
	Sample-1	**Sample-2**	**Sample-3**	**Sample-4**	**Sample-5**
SNR (dB) @ 0.5/1MHz	95.4 / 87.7	98.7 / 96.7	94.3 / 96.4	105 / 103	102 / 106
Thermal noise (nV/√Hz) @0.5/1MHz	31 / 53	25 / 45	29 / 47	35 / 45	20 / 50
1/f noise (µV/√Hz)@1KHz	0.42	1.21	0.31	0.89	0.59
1/f corner (KHz)	290	286	272	314	274
THD (%)	6.31	2.15	6.93	4.87	9.28

(a)

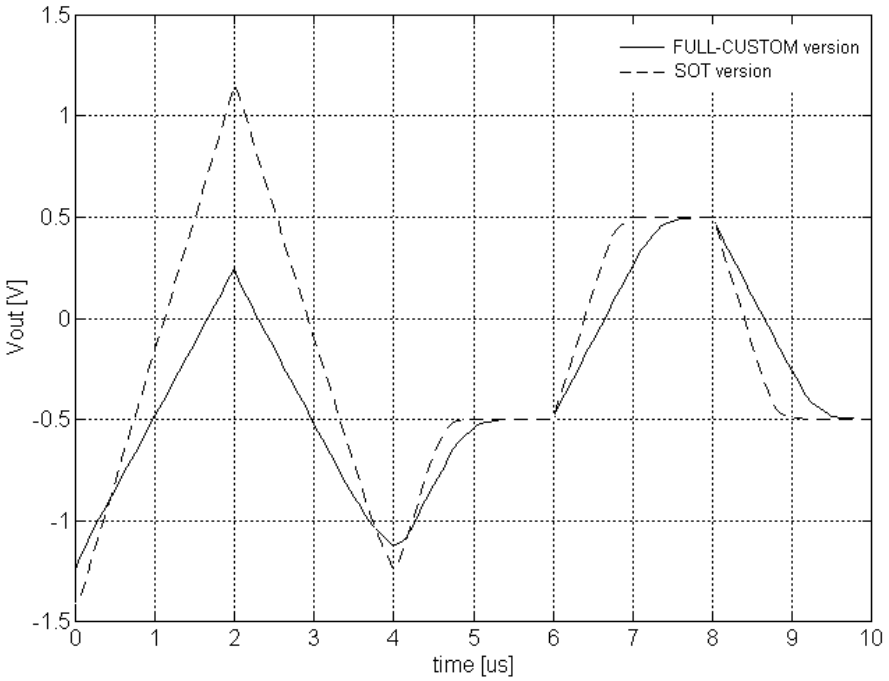
	Sample-1	**Sample-2**	**Sample-3**	**Sample-4**	**Sample-5**
SNR (dB) @0.5/1MHz	95.7 / 94.4	102 / 97.6	86.3 / 87.7	95.5 / 94.6	90.8 / 89.5
Thermal (nV/√Hz) @ 0.5/1MHz	27 / 55	23 / 47	28 / 41	25 / 46	28 / 63
1/f noise (µV/√Hz)@1KHz	2.83	1.72	1.63	2.83	2.03
1/f corner (KHz)	456	426	420	486	416
THD (%)	11.11	15.21	6.72	9.89	5.99

(b)

The noise performance of the OTAs has also been investigated. The results are summarized in Table 9a and Table 9b, where are shown measured noise for 5 samples of each OTA version. In appendix B, experimental noise power spectral densities measured at the OTAs output are depicted in Figs. B-1a, B-1b, B-1c, B-1d and B-1e (Appendix B). The results show that the flicker noise in both versions is large due to dependence on input differential-pair geometry-area (L and W) – section 4.3. In this OTA design, the differential-pair has small geometry-area (M1-M2 in Table 5.7), since the design objective was just for test purposes. Regarding the thermal noise, in SOT version is almost similar (or slightly higher) to the equivalent full-custom version. The total harmonic distortion has been performed in order to check the total amount of non-linearity present in the OTAs, also shown in Table 9a and 9b. The results manifested that in some SOT versions present larger THD than in full-custom versions. One can minimize non-linearity in SOT methodology by careful mapping of the full-custom to their equivalent TAT associations (section 3.3) and biasing level currents in cascode devices (decreasing V_{DSsat}).

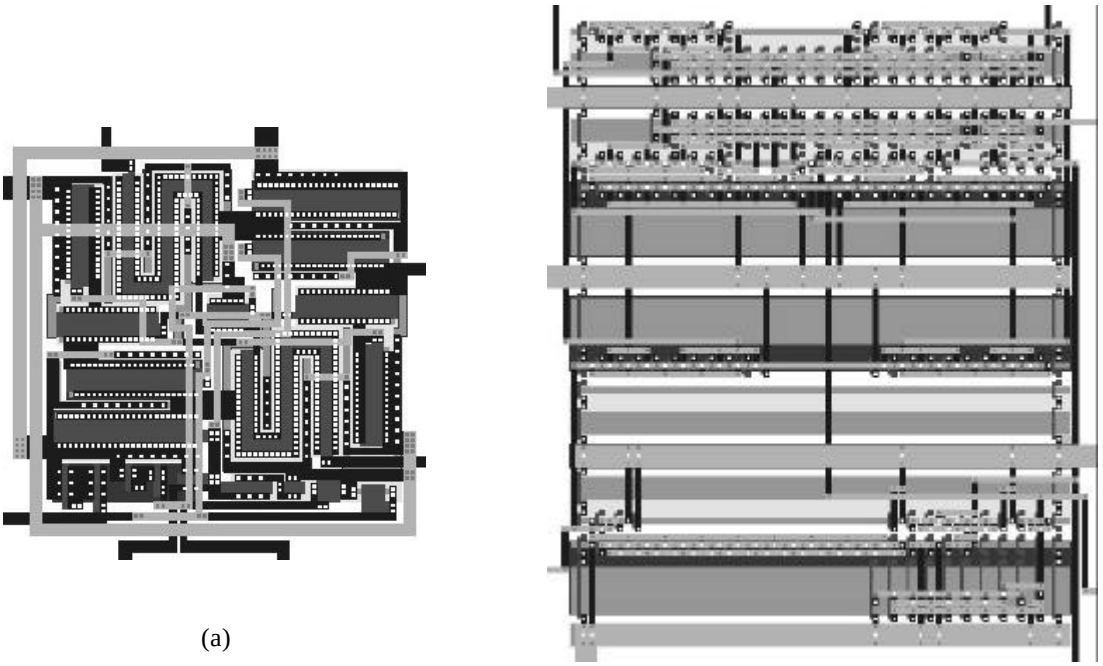


(a)



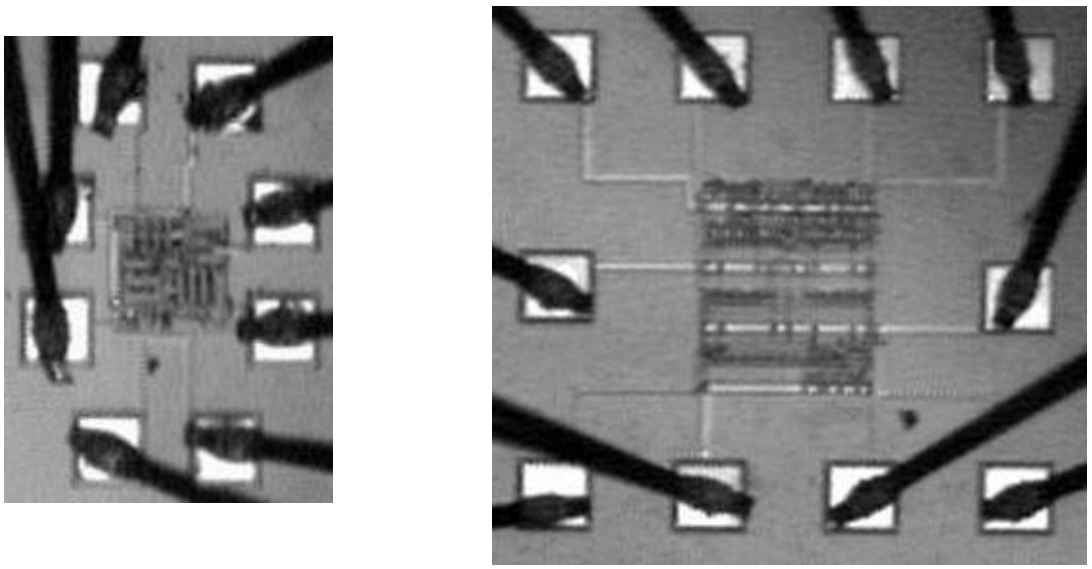
(b)

FIGURE 5.11 - Simulated OTA performance. Full-custom and SOT array version for 1.0µm CMOS technology at C_L=50pF. (a) Gain and phase. (b) Transient response (buffer config.).



(a) (b)

FIGURE 5.12 - Layouts of the folded-cascode OTA (1.0µm CMOS technology): (a) Full-custom. (b) SOT array.



(a) (b)

FIGURE 5.13 - Die photos of the folded-cascode OTA (1.0µm CMOS technology). (a) Full-custom. (b) SOT array.

6 Sigma-Delta Modulator Implementation on SOT Array Using TAT

This chapter is dedicated to the design of Sigma-Delta (SD) modulator for GSM system application. The main concerns in this design are power consumption and signal-to-noise ratio (SNR) of the SD modulator, which is degraded by non-linearity in the integrators. Due to non-linear feedback, non-accurate prediction of noise leakage and distortions, the SD modulator evaluation is not effortless and requires electrical level time-domain simulations [BOS88], [CHO94]. For these reasons, the analysis was done with behavioral simulation (Simulink, MatLab) at system level design. Before demonstrating the modulator and chip-tests design in full-custom and on pre-diffused SOT array, it worth first get an overview on the general SD modulator.

6.1 Sigma-Delta Modulator Overview

In recent times, oversampling A/D and D/A converters have become popular due to their high resolution for medium-to-low speed applications, such as high-quality digital audio, voice-band communications and others. The major reasons for their popularity are: firstly, oversampling converters relax the requirements put on the analog circuitry at the expense of more complicated digital circuitry. This trade-off becomes more desirable for modern sub-micron technologies with 3V (or lower) power supply voltages where complicated high-speed digital circuitry is easily realized in less area. However, the realization of high-resolution analog circuitry is complicated because of low supply voltages and poor output impedance of the transistors caused by short-channel effects. By means of oversampling data converters,

analog components have reduced requirements on matching tolerances and amplifier gains. A second advantage is that, it simplifies the requirements placed on the analog anti-aliasing filters for A/D converters and smoothing filters for D/A converters. Usually only a first-order anti-aliasing filter is required, which can often be realized on-chip or at worse case very inexpensively off-chip. Moreover, a sample-and-hold is not required at the input of switched-capacitor SD A/D converters.

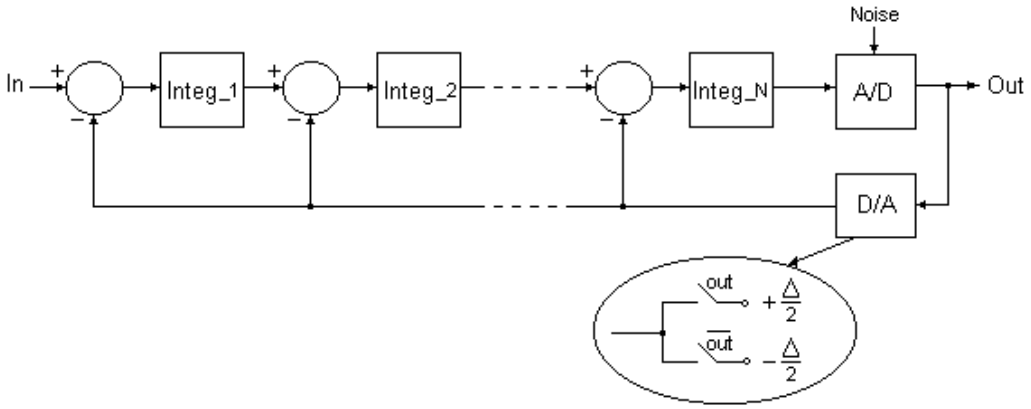


FIGURE 6.1 - Basic N[th]-Order Sigma-Delta modulator.

The ideal performance of a SD modulator – Fig. 6.1 – can be characterized by means of dynamic range (useful signal range) and in-band noise power. Generally, for a given order *N* of a general SD modulator, the dynamic range DR is given by [JAN93], [MAL99]:

$$DR = \frac{3}{2} \cdot \left(\frac{V_{in_{\max}}}{\Delta} \right)^2 \cdot \frac{2N+1}{p^{2N}} \cdot OSR^{2N+1} \cdot \left(2^B - 1\right)^2 \qquad 6.1.1$$

where *B* is the number of bits of the D/A converter, $V_{in_{\max}}$ is the maximum peak-to-peak input voltage signal amplitude, Δ is quantization step (from reference voltages $\pm\frac{\Delta}{2}$), and *OSR* is oversampling ratio. Although, the overall performance of a SD modulator by improving the ratio $\frac{V_{in_{\max}}}{\Delta}$ or increasing *OSR*, the expression 6.1.1 clearly shows that the higher is the order *N*, the better is the performance. Nonetheless, it often means cascading more integrators in the feedback loop. Therefore, it increases phase shifting, thus increasing the possibility of overall instability [CAN85], [BOS88], [UCH88]. However, the feedback performs an important role

in an oversampling converter. Filtering feedback around low-resolution quantizer (1-bit in this case) has the effect of shaping the spectrum of quantization noise.

Therefore, a high resolution SD modulator is put forward here that utilizes multistage noise-shaping (Mash) technique. The Mash approach allows higher orders of SD modulator by means of lower orders of SD modulators structured in parallel instead of cascading. It eliminates the feedback loop instability problem caused by multiple-order integrators in a single feedback and it reduces required linearity for D/A circuits. The disadvantage is the block components (example, gain) mismatches between stages that affect the SNR. Additionally, previous characteristics show that oversampling techniques are suitable for analog-digital implementation by means of VLSI CMOS digital technologies.

6.2 A 4th Order 2-2 A/D Sigma-Delta Modulator Design

The A/D converter herein presented is the Sigma-Delta project developed by the Analog VLSI group at The Ohio State University. The focus of the design is a system that fills a specific requirement, that is, a programmable multi-standard A/D system for wireless communication applications. The general architecture is schematized in Fig. 6.2. Initially, the main wireless communication standards targeted were for GSM (890-960MHz of frequency spectrum) and DECT (1881-1897MHz) with bandwidth of 100KHz and 700KHz, respectively – shown in Table 6.1. A higher dynamic base-band system, a Sigma-Delta converter, was chosen thanks to its robustness and tolerance with respect to the mismatch effects in analog components. Moreover, it shows superiority to other converters when low voltage and high dynamic-range operation are required.

A Mash structure of a 4th-Order A/D SD modulator is shown in Fig. 6.3. It utilizes a configuration using two noise-shaping converters of 2nd-Order SD modulator. Exchanging resolution by speed, this Sigma-Delta is perfect for multi-standard applications. Maintaining unaltered the circuit, a higher resolution can be obtained by lowering data rate. Alternatively, increasing sampling frequency at fixed bandwidth, higher resolution is also obtained (or fixing sampling frequency at higher bandwidth) – Table 6.2.

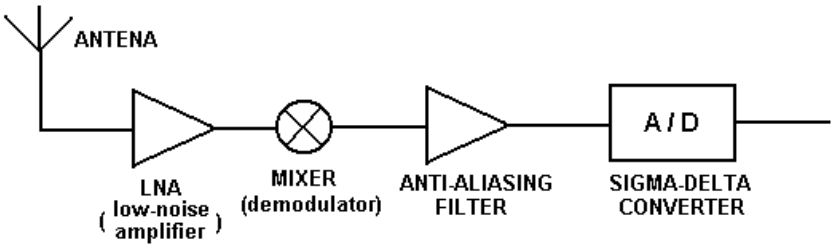


FIGURE 6.2 - General architecture of a wireless receiver system.

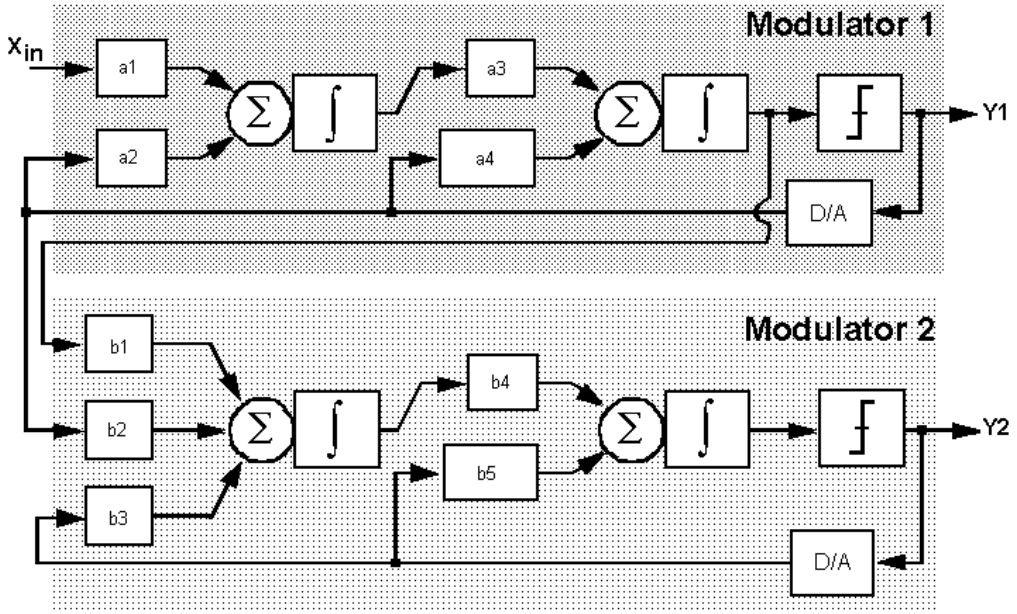


FIGURE 6.3 - 4th-Order Sigma-Delta modulator diagram with gain per filter.

Consequently, a programmable SD system can be achieved and implemented using individual or combination of the following strategies:

1. Capacitors array selection;
2. Reference voltage scaling (automatic gain control function);
3. Dynamic biasing: slew rate programmability;
4. Doubling sampling frequency (f_s) to increase SNR;
5. Sampling rate adjustment;
6. Multi-bit digital-to-analog converter, instead 1-bit.

The appropriate approach is decided depending on the system specification and requirement. The above approaches are better observed from the expression 6.1.1. The item 2

changes dynamically the SD modulator characteristics by scaling the ratio between the input signal and reference voltages ($\frac{V_{in_{\max}}}{\Delta}$). This technique is called as voltage gain control and it is required an additional circuitry, which is a disadvantage. The item 3 is realized adjusting the OTA output current, that is, as power consumption is directly proportional to the circuit bias currents and low current means low SR, the output current is increased as it required. Hence, maximum frequency operation can be increased and further increasing sampling frequency and oversampling ratio, with the advantage of maintaining low power consumption. Obviously, an extra – and complex circuitry is needed.

TABLE 6.1 - Different standards for wireless communication systems.

Parameters		GSM	E-GSM	DECT	PCS1900
RF Frequency range (MHz)	(Tx)	890-915	880-915	1.88-1.897	1.85-1.91
	(Rx)	935-960	925-960		1.93-1.99
Channel-spacing (KHz)		200	200	1728	200
Sensitivity (dBm)		-102	-102	-83	-102
Input noise (dBm)		-120.8	-120.8	-112.3	-120.8
Noise figure (dB)		9.8	9.8	19	9.8
IM3 (dBm)		-118	-118	-100.3	-118
IP3 (dBm)		-13.5	-13.5	-14.6	-13.5
Baseband dynamic range (dB)		80-100	80-100	60-80	80-100
Baseband signal bandwidth (KHz)		100	100	700	100
Resolution (n^{o} of bits)		13-16	13-16	10-13	13-16

Doubling or adjusting sampling frequency – item 4 and 5 – in order to increase SNR is limited to maximum speed of the Comparators and OTAs or SC Integrators. Finally, the last approach – item 6 – is similar to the traditional A/D converters. Increasing D/A converter number of bits, less noise is introduced in the system, then improving overall performance. However, the main drawback is that, an n-bits D/A converter requires circuit auto-calibration and precise trimming to obtain the required linearity, while for a 1-bit D/A converter is not needed. It is inherently linear, since two output values characterize two points that define a straight line.

Therefore, although some disadvantages, the strategy implemented in this SD modulator is the first technique. Several unitary capacitors are linearly set in an array and switches select the required capacitors values in order to adjust the filter (integrator) coefficients, and then transforming the SD modulator into a new behavior/characteristic

performance. The major drawback is the noise degradations, increasing power consumption and larger silicon area.

TABLE 6.2 shows different combinations of sampling frequency and oversampling ratio required for different SD modulator architectures, given a dynamic range (resolution).

TABLE 6.2 - Different Sigma-Delta A/D modulator architectures requirement for GSM and DECT standards.

Sampling Rate for Bandwidth of 100kHz (GSM Family)							
Resolution – *DR*		*N=1*	*N=2*	*N=3*	*N=4*	*N=5*	*N=6*
8bits – 50db	$f_{s\,(MHz)}$	12.8	6.4	3.2	1.6	1.6	1.6
	OSR	60-64	17-32	10-16	8-8	6-8	5-8
10bits – 62db	$f_{s\,(MHz)}$	51.2	6.4	3.2	3.2	3.2	1.6
	OSR	151-256	29-32	15-16	10-16	8-16	6-8
12bits – 74db	$f_{s\,(MHz)}$	102.4	12.8	6.4	3.2	3.2	3.2
	OSR	380-512	50-64	22-32	13-16	10-16	8-16
14bits – 86db	$f_{s\,(MHz)}$	204.8	25.6	6.4	**6.4**	3.2	3.2
	OSR	956-1024	87-128	32-32	**18-32**	13-16	10-16
16bits – 96db	$f_{s\,(MHz)}$	819.2	51.2	12.8	6.4	6.4	3.2
	OSR	2400-4096	152-256	48-64	25-32	17-32	12-16

Sampling Rate for Bandwidth of 700kHz (DECT)							
Resolution – *DR*		*N=1*	*N=2*	*N=3*	*N=4*	*N=5*	*N=6*
8bits – 50db	$f_{s\,(MHz)}$	89.6	44.8	22.4	11.2	22.4	11.2
	OSR	60-64	17-32	10-16	8-8	6-8	5-8
10bits – 62db	$f_{s\,(MHz)}$	358.4	44.8	22.4	22.4	22.4	11.2
	OSR	151-256	29-32	15-16	10-16	8-16	6-8
12bits – 74db	$f_{s\,(MHz)}$	716.8	89.6	44.8	**22.4**	22.4	22.4
	OSR	380-512	50-64	22-32	**13-16**	10-16	8-16
14bits – 86db	$f_{s\,(MHz)}$	1433.6	179.2	44.8	44.8	22.4	22.4
	OSR	956-1024	87-128	32-32	18-32	13-16	10-16

In bold style are indicating the SD modulator architectures required for GSM and DECT standards, according to their performance specifications shown in Table 6.1. The resulting 4^{th}-Order 2-2 SD modulator is schematized in Fig. 6.4. This structural design consists in two stages in parallel, employing 2^{nd}-Order SD modulators, translated from the block diagram of Fig. 6.3.

The reference voltages (1-bit D/A), indicated in Fig. 6.4, are settled on V_{ref+}=+2.5V and V_{ref+}=+0.5V (V_{DD}=3V) that consists on the maximum input signal-swing pointed by

system-level specifications. The integrator gain mismatching must be less than 2% and comparator offset less than 20mV (section 5.3 – Table 5.6).

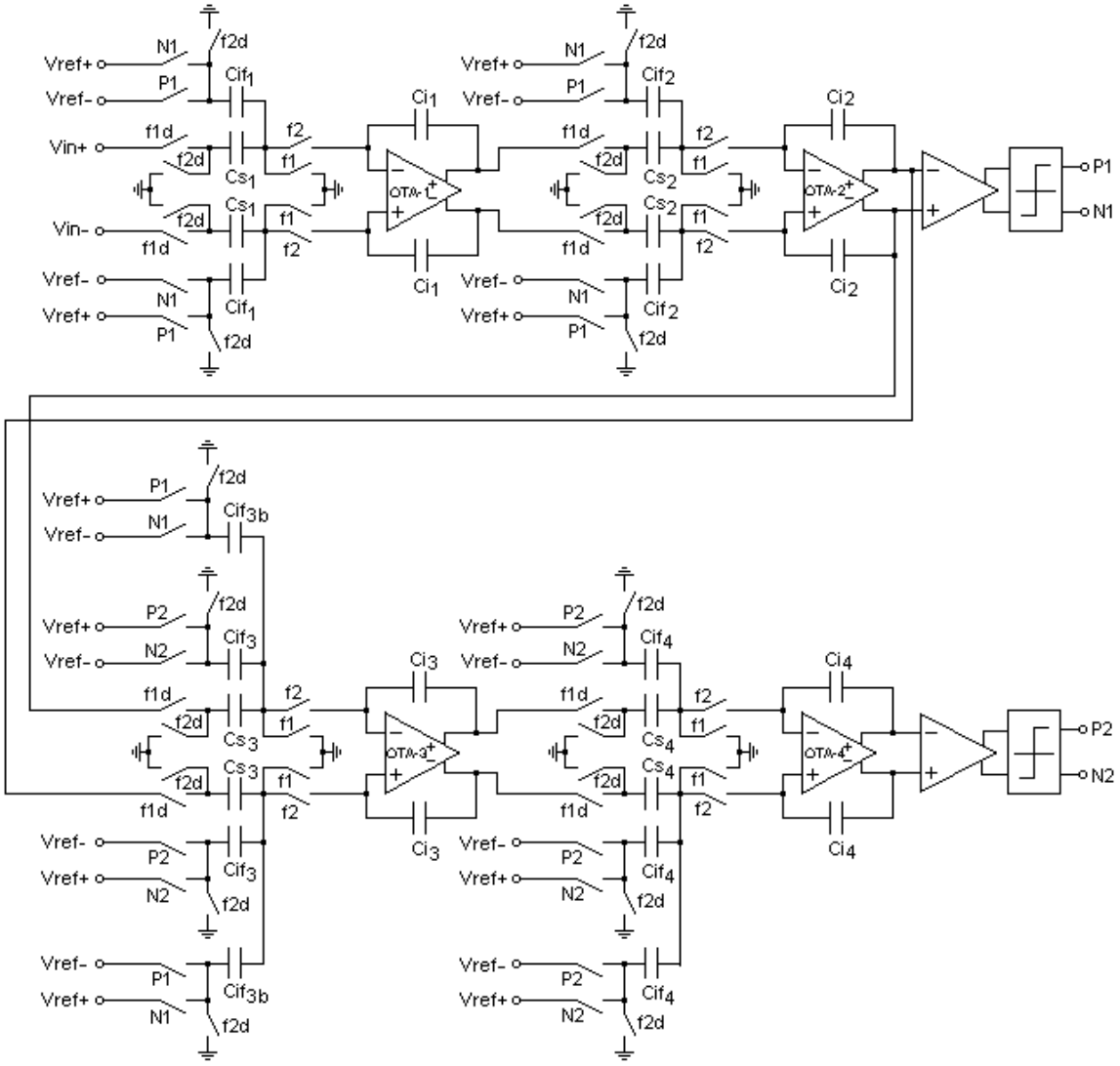


FIGURE 6.4 - A 4th-Order 2-2 Sigma-Delta A/D Modulator.

The track-and-latch comparator is the same designed in previous chapter (chapter 5 – Fig. 5.6 and Table 5.6). In order to hold and increase output fan-out, the signal compared and memorized during sampling time, the comparator outputs are followed by a latch type D (not shown here).

The gain coefficients of each stage also control the signal amplitude overloading. They have been defined by behavioral simulations, at system level, using Simulink, MatLab. The purpose of the behavioral simulations is to find the optimum gain coefficients. So that, integrators must have small signal swings in order to lead to higher dynamic range and further

achieve highest SNR; to minimize the noise quantitization due to flicker noise, thermal noise, noises accumulated in the capacitances (*kT/C*); to specify the OTAs requirements (gain, slew-rate, output swing and settling time), and to determine the sensitivity of the integrators and feedback coefficients.

6.3 Minimizing Noise Sources in SD Modulator

Accounting the problem of noise sources in the SD modulator, shown in Fig. 6.4, it can be expressed generally by:

$$N_{Total}^2 = N_Q^2 + N_{OTA-1}^2 + N_C^2 + N_{OTA-2}^2 + N_{SW}^2 + N_o^2 \qquad 6.3.1$$

where the terms represent the total noise of each block component. N_Q is quantization noise, $N_{OTA\text{-}1}$ and $N_{OTA\text{-}2}$ is the major noise contribution of each operational amplifier, N_C is capacitors *KT/C* noise, N_{SW} is the noise from switches, and finally N_o accounts the random noise sources contribution. From Table 6.1, it is clear that in order to meet noise figure and input noise, the N_{Total} must be set at minimum as possible. Among other noise sources that cannot be controlled by the designer, one can overcome mainly by careful designing first and second OTA and switches, since quantization noise is intrinsically improved (reduced) choosing a specific SD modulator architecture – Table 6.2.

Noise in CMOS switches that are employed in this design, is relatively easy to be controlled. The major noise sources are the charge injection (clock-feedthrough) from gate to source-drain during clock transitions, which is minimized using minimum transistors size, slow clock transition (trapezoidal-shape) and using fully-differential architecture [CHO94], [ALE97]. Hence, the strategy to minimize noise sources in SD modulators reduces to the OTAs design (noise expression 5.4.7 or 6.3.2).

Noise in folded-cascode OTA can be minimized by increasing geometry W and L of input pair and current sources (equation 5.4.7), which can be understood better separating the contribution of each component for the equivalent noise (flicker or thermal):

$$N_{OTA}^2 = N_{pair}^2 + \left(\frac{g_{m_{CurS\,1}}}{g_{m_{M\,1}}}\right)^2 \cdot N_{CurS_n}^2 + \left(\frac{g_{m_{CurS\,2}}}{g_{m_{M\,1}}}\right)^2 \cdot N_{CurS_p}^2 \qquad 6.3.2$$

where N_{pair} is the input pair noise contribution, N_{CurSn} and N_{CurSp} are noise contribution of the current sources $\left(\propto \frac{1}{L_{CurS}^2}\right)$, g_m is the OTA transconductance, and g_{mCurS1} and g_{mCurS2} is N and P type, respectively, transconductances of the current sources. The above equation demonstrates that one must design carefully input pair geometry area (section 5.4), making as small as possible the transconductances and/or increasing channel lengths of the current sources.

TABLE 6.3 - Designed transistor sizes for CMOS switches. Single and TAT versions for 0.5µm CMOS technology (prime superscripts indicate TAT version).

CMOS Switches (0.5µm CMOS technology)			
Transistor	**W(µm)**	**L(µm)**	**W/L**
NMOS	10	0.6	16.67
NMOS'	2x(5.4)	0.6	18
PMOS	20	0.6	33.33
PMOS'	2x(11.7)	0.6	39

6.4 Defining Correct OTA Constant-Time and Settling-Time for the SD Modulator

In order to model and determine the OTA unit-gain frequency, the definition of a constant-time t_{OTA} is introduced simultaneously with the feedback factor fd (defined in section 6.5). Then f_T can be modeled as follows:

$$f_T = \frac{g_m}{C_L} = \frac{\sqrt{(2 \cdot b \cdot I_{bias})/n}}{C_L} = \frac{1}{2p \cdot fd \cdot t_{OTA}} \qquad 6.4.1$$

Non-predictable OTA settling-time [YAN90], [GRE86] variations aiming system behavior modeling, an exponential dependency with input signal amplitude was assumed, that

is, $V_{out}(t) = V_i \cdot (1 - k_3 \cdot V_{out-swing}^2)$ instead of ideal model $V_{out}(t) = V_i \cdot (1 - e^{-(t_s/t_{OTA})})$. This approximation is not accurate, but attempt to model variations of settling-time with output voltage swing, which is not simple.

In order to guarantee correct settling-time and further overall system stability, the minimum slew-rate time was defined as one-fourth part of active semi-cycle of the sampling frequency, assuring proper sampling signal due to clock jitters and non-linearity effects. Thus, the minimum OTA slew-rate can be determine, resulting in the following expression:

$$SR_{\min} = \frac{\Delta V_{OTA_{\max-swing}}}{t_{slew}} = \frac{\Delta V_{OTA_{\max-swing}}}{T_s/8} = 8 \cdot f_s \cdot \Delta V_{OTA_{\max-swing}} \qquad 6.4.2$$

where $\Delta V_{OTA_{\max-swing}}$ is the OTA maximum output voltage swing, t_{slew} is slew-rate time, and $\frac{1}{f_s} = T_s$ is sampling period.

6.5 Switched-Capacitor Integrator for the SD Modulator

For the classical two-stage OTA the unit-gain frequency remains relatively constant for varying load capacitances. However, for the folded-cascode and current mirror amplifiers are strongly related to their load capacitance [GRE86]. Hence, their settling-time performance is affected by both feedback factor β as well as effective load capacitance.

In order to determine *fd* in SC integrator and further total capacitance at OTA output, consider the general case shown in Fig. 6.5. The C_P represents parasitic capacitance present at the input of OTA (large transistor pair) and from any switch capacitance. The C_c is the compensation capacitance that might be added in order to maintain a sufficient phase margin. Thus, the feedback network is due to capacitances C_S, C_i and C_P, which *fd* is given by:

$$fd = \frac{C_i}{C_S + C_P + C_i} \qquad 6.5.1$$

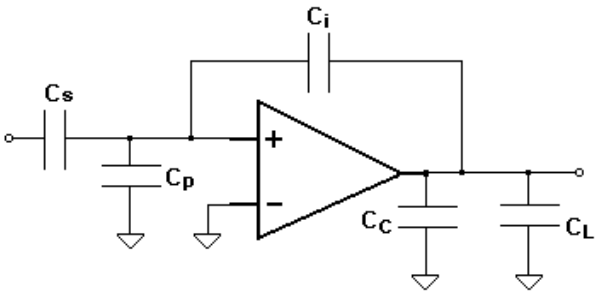


FIGURE 6.5 - A general SC Integrator for determining total load capacitance.

TABLE 6.4 - Capacitors values for the SC Integrators shown in Fig. 6.4.

	Ci (pF)	Cs (pF)	Cif (pF)
Integ-1	2	6.8	1.4
Integ-2	0.5	1	0.2
Integ-3	0.25	0.5	0.05
Integ-4	0.5	0.5	0.1

The effective load capacitance seen by the OTA output is given by the parallel combination of C_c and C_L, as well as that seen looking into C_i. The capacitance seen looking into C_i is equal to the series combination of C_i together with C_S+C_P, then resulting in:

$$C_{L_{TOTAL}} = C_L + C_c + \frac{C_i \cdot (C_S + C_P)}{C_S + C_P + C_i} \qquad 6.5.2$$

The capacitors value that defines the integrator (filter) gain are summarized in Table 6.4. For values equal or less than 0.1pF were resized in order to avoid the inaccuracies caused by small capacitance (process undercutting, edge effects, etc) during the fabrication process when laid out onto the chip. To minimize non-linearity and undercutting problems in MOS capacitors the well-known unit capacitors technique [ALE97], [CHO94], [GRE86] is used.

6.6 Fully Differential OTA for SC Integrator

In order to design fully differential SC integrators that achieve the performances required from specifications and defined by system level simulations, a fully differential folded-cascode operational amplifiers is required. The OTA and bias circuit implemented are shown in Fig. 6.6a and Fig. 6.6b with the designed transistors size listed in the Appendix C in Table G-1 and Table G-2, as well as the performance of each OTA is listed in Table 6.5. All four OTAs have same topological structure, but each OTA design and sizing adjustment are different to meet specifications for each integrator.

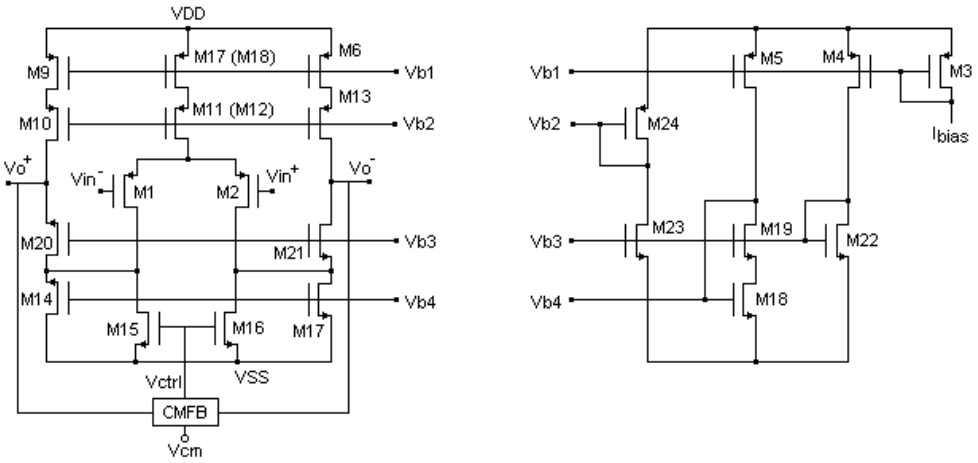


FIGURE 6.6 - (a) Fully differential folded-cascode OTA. (b) Bias circuit.

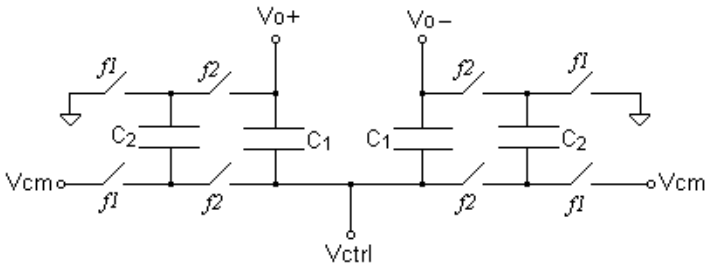


FIGURE 6.7 - Switched-capacitor common-mode feedback circuit.

Note that, the first OTA has higher performance since it is the front-interface, which accumulates forward and feedback signal. Moreover, it is responsible for amplifying the

signal, and because of feedback path, it cannot introduce more noise and non-linearity in the system. Hence, a special design attention on the first OTA is needed. The second OTA has (slight) relaxed performance in relation to the first one, while the third and fourth OTAs have the same characteristics, in view of the fact that the signals were already filtered by the first OTA.

TABLE 6.5 - Simulated performance of the fully differential folded-cascode OTAs in 0.5µm CMOS technology.

	OTA-1	**OTA-2**	**OTA-3**	**OTA-4**
Supply voltage (V_{DD})	+3.0	+3.0	+3.0	+3.0
DC Gain (dB)	80	78	55	55
Unit Gain Freq. (MHz)	110	80	5.3	5.3
Phase Margin (°)	>50	75	90	90
Settling time (ns)	31 (0.01%)	12 (1%)	-	-
Slew-rate (V/ms)	90	50	34	34
Current Consumption (mA)	1450	360	140	140
***1/f* noise (nV/√Hz @ 1KHz)**	42	-	-	-
Thermal noise (nV/√Hz @ 1MHz)	5	-	-	-
Diff. Output swing (V)	2.6	2	2	2

Simulated plots in Fig. C-1a shows the DC gain, bandwidth and phase margin maximum variations of ±3% for three different temperatures (-40°C, 27°C, 100°C). The worst case of simulated noise, shown in Fig. C-1b, is below that required by the specification (sensitivity in Table 6.1). Simulated settling-time (section 6.4) is shown in Fig. C-2b. The results are demonstrating the transient response (slew-rate) on the OTA differential output and on each output. Another important OTA characteristic is the variation of the DC gain with output voltage variation. The simulation result is shown in Fig. C-3.

Often fully differential amplifiers even in a feedback application do not affect the common-mode voltages. Then, a circuit must be applied to the outputs to bring them to a common mode. The CMFB (common-mode feedback) circuit, employed here is based on the switched-capacitor circuits, shown in Fig. 6.7, since the integrator is switched-capacitor and

this approach are generally preferred over their continuous-time counterparts due to a larger output signal swing.

TABLE 6.6 - Designed transistor sizes for OTA-3 and OTA-4. Full-custom versions in 0.5µm CMOS technology.

OTA-3 and OTA-4 (0.5µm CMOS technology)			
Transistor	**W(µm)**	**L(µm)**	**W/L**
M1,M2	110	1.25	88
M3,M4	10	3	3.33
M5	20	3	6.67
M6,M7,M8,M9	60	3	20
M10,M11,M12,M13	60	1	60
M14,M17	40	4	10
M15,M16	20	4	5
M18	10	4	2.5
M19	10	2	5
M20,M21	35	2	17.5
M22,M23	4	4	1
M24	8	4	2

Usually, the C_2 capacitor is set one-forth to one-tenth of C_1 capacitor [JOH97]. In this circuit, the values are (C_1=10C_2) C_1=1pF and C_2=0.1pF. The switched-capacitor CMFB performance was plotted in Fig. C-2a. The simulation results show both output are moving toward common-mode voltage (1.5V in this case) with no signal applied at the inputs and after some time a pulse signal at the inputs. Note the OTA differential output sustains at zero at the same time as both output signals are settling to the middle-point.

Furthermore, as the SD converter is for wireless-communication applications, power consumption was also a concern. In the OTAs design, bias currents were limited as low as possible (regarding minimum SR requirement) and settled to operate at low supply voltage, compatible to a portable system, which is constrained by the technology at V_{DD}=3V.

6.7 Test-chips: Full-custom vs. SOT of 2nd-Order SD Modulator and Block Components

The previous designed analog subcircuits and Sigma-Delta A/D modulators were also implemented with SOT array methodology in a 0.5µm double poly CMOS technology, from AMI company. All full-custom and SOT array layouts design were hand designed, with no assistance in the layout automation. As a result, the SOT array layouts are not well optimized in area, as well as not optimized for maximum SOT occupation and circuit symmetry, as shown in the layouts presented in Appendix D. The full-custom layouts have better geometrical placement and optimization in silicon area than the SOT version. The OTA-1 and OTA-2 in particular have not been optimized for minimum area.

In order to have fair comparisons, the SOT versions have been generated via direct conversion of each single transistor into TAT transistor (section 3.3). The converted equivalent TAT versions are listed together with their single transistor versions in Table 5.1 for the current mirrors, Table 5.3 for the Amplif-1 and Amplif-2, Table 5.5 for the comparators, Table 6.3 for the switches, Table C-1 and Table C-2 for the OTA-1 and OTA-2, respectively.

Comparing the total number of transistors employed to assemble each OTA, the full-custom version of OTA-1 and OTA-2 have 24 MOSFET transistors, while the SOT array versions using TAT transistors have 685 and 278 unit transistors, respectively. Additionally, the SR type buffer-latch required in the comparator (section 5.3) and the clock generator circuit are not accounted and not shown here, since they are digital circuits. Nonetheless, these SR latch and clock generator circuits were implemented in the test chip. The clock generator circuit provides the clocking phases required for the block components of the SD modulator, which has basically 2 complementary clock signals with their delayed signals, resulting in the bus clock of 8 phase signals.

The IC package type from MOSIS (American foundry) is a DIP40 (40 pins) for AMI and HP 0.5µm CMOS technology (double poly, triple metal), with total die size of 1500µm x 1500µm, including pad frame. The total silicon area, without the pad frame, available for IC layout design is only 1100µm x 1100µm . This has proven to be a severe design constraint for the SOT array versions that were designed. Actually, this constraint was the main reason for the implementation of only the Modulator-1 (2^{nd}-Order SD converter), shown in Fig. 6.3 and

Fig. 6.4. The electrical simulated performance of the Modulator-1 is plotted in Fig. D-1. Observe the integrators output. The noise shape can be verified. The first noise-shaping format is linear and the second one is quadratic, as expected [CAN85], [CHO94].

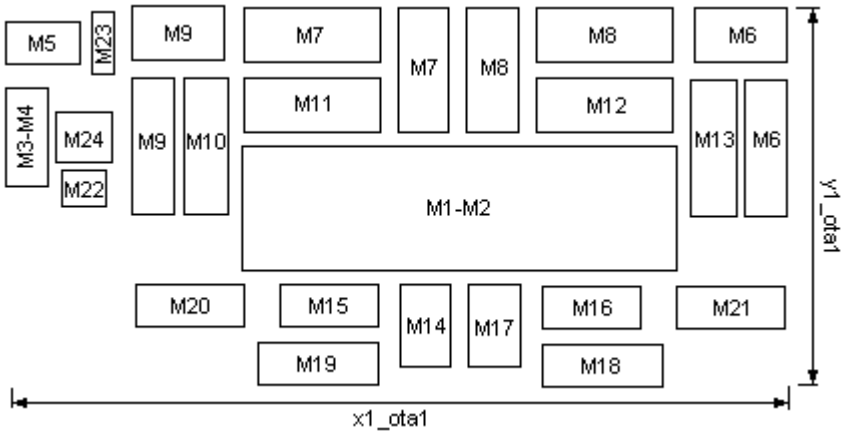
TABLE 6.7 - Full-custom and SOT array layout area sizes of the OTA-1, OTA-2, Comparator+Buffer and single-stage CS Amplifier in 0.5µm CMOS technology.

	Full-custom		**SOT array**		**Total Area ratio A_2/A_1**
	x1 (µm)	y1 (µm)	x2 (µm)	y2 (µm)	
OTA-1	~ 620	~ 320	~ 820	~ 390	1.612
OTA-2	~ 265	~ 165	~ 290	~ 450	2.985
Comparator	~ 255	~ 78	~ 480	~ 210	5.068
CS Amplifier	~ 90	~ 66	~ 180	~ 82	2.485

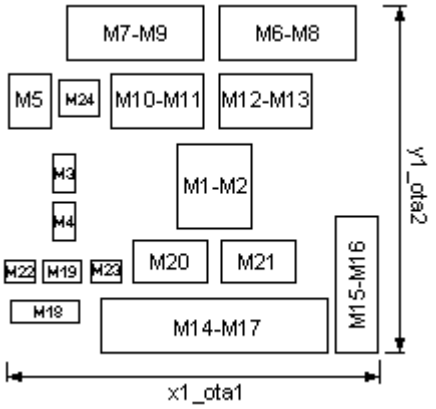
Figures 6.8a, 6.8b, 6.9a and 6.9b show the layout floorplanning designed and implemented in full-custom and SOT methodology for the first (OTA-1) and second (OTA-2) operational amplifiers of the Modulator-1. The corresponding layouts of OTA-1 and OTA-2 are in appendix D (Figs. D-9 and D-8, respectively). In Fig. 6.8a and Fig. 6.8b, each rectangle represents a transistor pair in a linear matrix of the SOT array described in Fig. 3.1. In comparison to their full-custom layouts counterparts, in the SOT array the devices are not symmetrical placed, since the TAT transistors are not symmetrical geometry and they are arranged in a linear matrix. Nevertheless, the matching can be maintained putting together and interdigitizing the transistors pairs [ISM94], [JOH97], as illustrated by the layout schematics in the figures. The layout area for the OTA-1, OTA-2, comparator and common-source amplifier are listed in Table 6.7 with approximate sizes.

For the comparators, the SOT version is larger in area since the full-custom layout was designed as minimum area as possible. Although the full-custom versions of the OTAs were not customized at minimum area as possible, illustrated in Fig. 6.8a, Fig. 6.8b, Fig. 6.9a and Fig. 6.9b, the SOT versions have larger silicon area. This is due to the unused transistor gates in the array. It is worse when is needed only minimum transistors for associations ($PMOS_{min}$ or $NMOS_{min}$ shown in Fig. 3.1 and Table 3.1). Non-minimum transistors between these minimum transistors are wasted and large area is unused, as shown in Appendix D - Fig. D-5 (current mirror SOT and full-custom layouts) and Figs. D-8b and D-9b (OTA-1 and OTA-2

SOT layouts. In addition, note the interdigitizing and common-centroid geometry techniques used in the full-custom and SOT layouts for silicon area saving and matching.



(a)

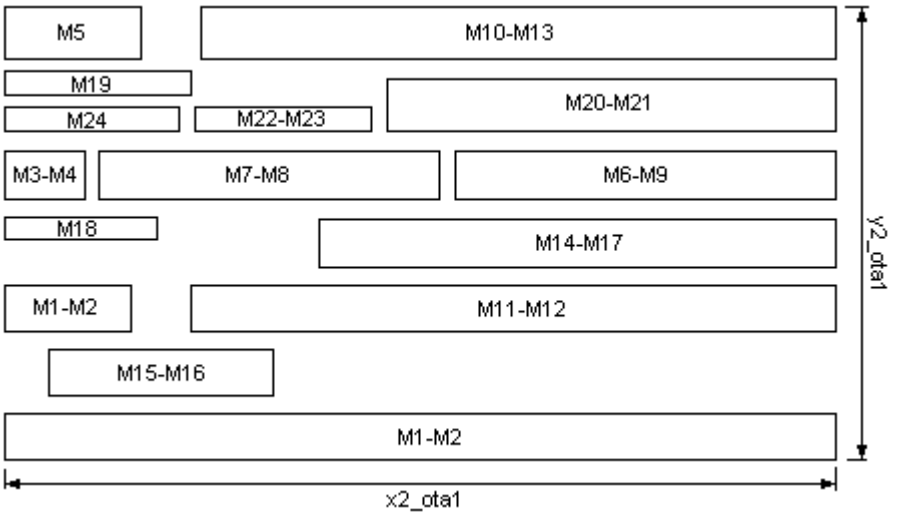


(b)

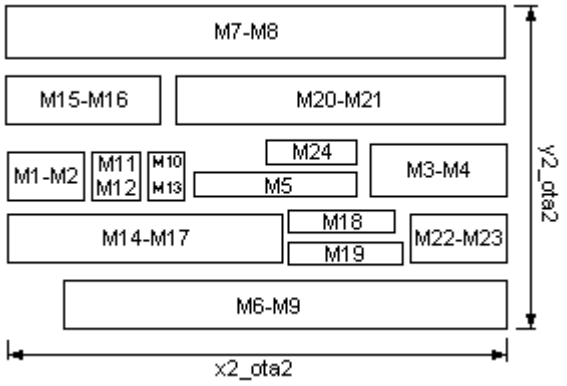
FIGURE 6.8 - Full-custom layout illustration for: (a) OTA-1 and (b) OTA-2.

For TAT transistors, the common-centroid geometry technique is not possible to apply because of drain and source terminals of MD transistors are independent. Only in MS transistors is possible. A simple idea used for matching MD pairs is interlacing a proper number of associated minimum transistors, as shown in Figs. D-5, D-7, D-8 and D-9 for TATs implementing current mirrors, differential pairs and matched branches for OTAs. The good results for this matching technique are shown in section 6.8.

Observe a very large number of transistors employed in TAT differential pairs of OTA-1 and OTA-2 shown in SOT layouts of Figures D-8b, D-9b and 6.9 (M1-M2 listed in Tables G-1 and G-2, Appendix C), which causes a large routing area, large unused transistors in the array and large silicon area.



(a)



(b)

FIGURE 6.9 - SOT array layout illustration for: (a) OTA-1 and (b) OTA-2.

An important AMI process feature is the construction of the passive devices, such as capacitors employed in SC integrators. In this process, the better capacitor is obtained between poly-poly layers (poly1-poly2), with effective capacitance value of 0.9*f*F/μm^2 ±11%, which leads to 10.6μm x 10.6μm of minimum area for 0.1*p*F capacitance (employed in this design). The minimum capacitance of 100*f*F is the preventive value usually used by VLSI designers in order to avoid the process undercutting that can affect the poly layer perimeter and then change the capacitance value.

Three IC chips have been fabricated in 0.5μm CMOS technology. The first test-chip, die photo shown in Fig. D-2 (Appendix D), contains transistors structures, OTA-1 and track-and-latch comparator (section 5.3) in both full-custom and SOT array methodologies. The aim is to investigate each SOT array version of analog circuit performance against its full-custom

version. The fair comparison results are improved as long as the circuits are placed side-by-side on same chip, to minimize die-to-die process variations.

The second (full-custom) and third (SOT array) test-chips, die photos shown in Figures D-3 and D-4 (Appendix D), respectively, contain a 2nd-Order SD modulator. The full-custom and SOT versions of this SD Modulator could not be placed together, as the result of the economic limitation on the silicon area, previously mentioned. Hence, a third one was necessary in order to implement the equivalent counterpart of the Modulator. Additionally, together with the SD modulator, CS amplifiers has been included (section 5.2 – Amplif-1 and Amplif-2) in the second test-chip (die photo of Fig. D-3) and current mirrors (M1-M2 and M1'-M2' – section 5.1) in the third test-chip. Each analog circuit with detailed layout in both full-custom and SOT array methodologies are depicted in Fig. D-5 (current mirrors), Fig. D-6 (common-source amplifiers), Fig. D-7 (comparator), Fig. D-8 (OTA-2) and Fig. D-9 (OTA-1). From the layout style, it can be observed that, a smaller area is occupied by the circuits in all full-custom versions in comparison to the SOT array methodology, as shown in Table 6.7.

6.8 Experimental Results: Test-Chips in 0.5mm Technology

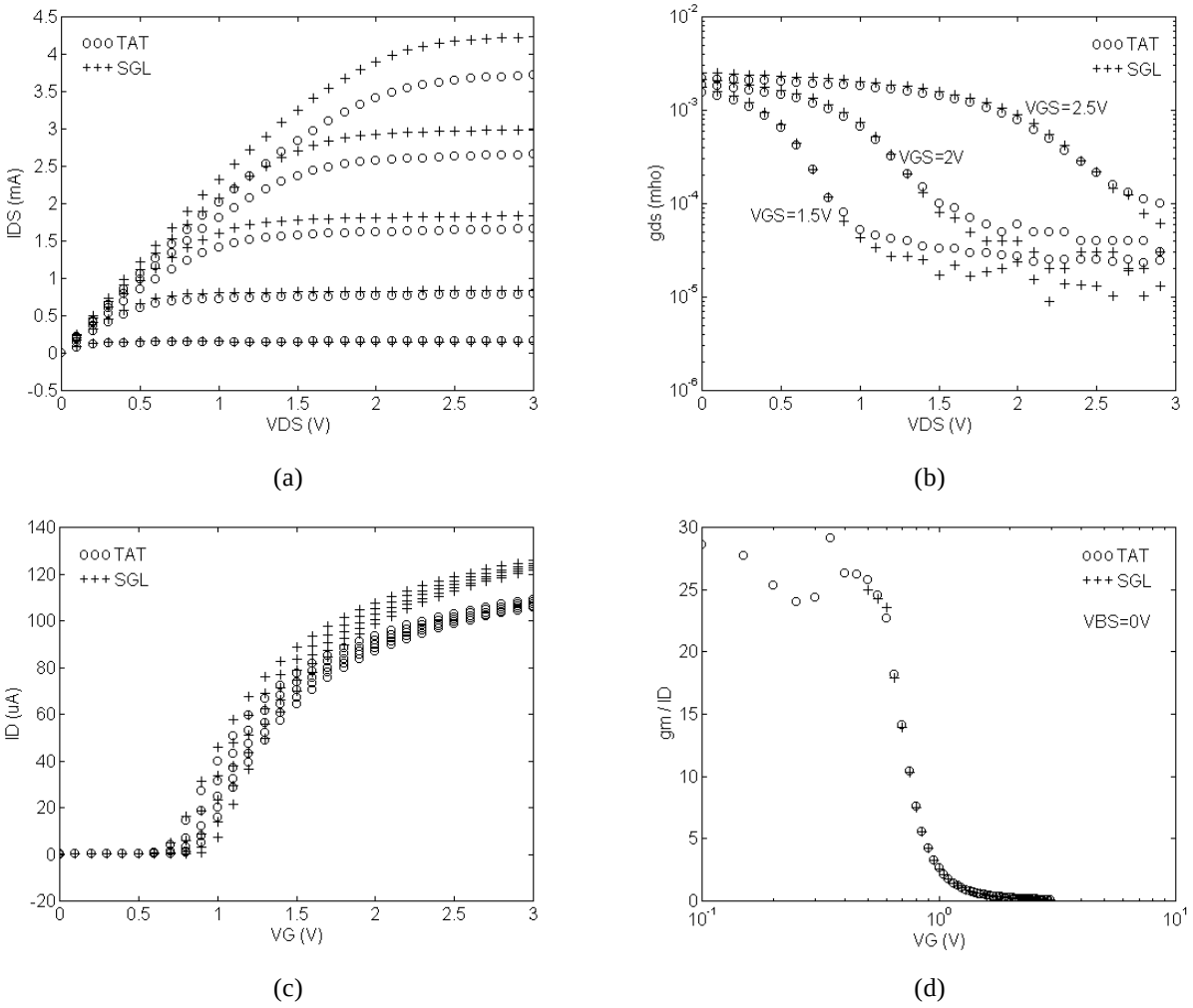


FIGURE 6.10 - Experimental curves characteristics of single and TAT transistors in 0.5µm technology: W/L=51µm/1.2µm, ND=10, NS=10, $(W/L)_u$=5.4µm /0.6µm. Average of 5 test-chip samples.

All the experimental results presented in this section are an average of several IC test samples. For investigation and validation of the TAT transistors in 0.5µm technology, a structure of short channel of single (full-custom) and its corresponding TAT transistors were fabricated. Experimental plots for specific characteristic curves are shown in Figs. 6.10a ($I_D x V_D$), 6.10b ($g_{ds} x V_D$), 6.10c ($I_D x V_G$) and 6.10d ($g_m/I_D x V_D$). The results confirm the conclusions for 1.0µm technology shown in section 4.6. This AMI 0.5µm technology has shown much better control of short channel effects than that of the ES2 1.0µm technology, as can be seen in Fig. 6.10d, when comparing L=1.2µm single transistor with the TAT with L=0.6µm (drawn length).

All analog building blocks of previous sections have been tested and validated. Experimental performance comparing full-custom and SOT versions of the current mirrors, common source amplifiers and comparators for 0.5µm technology are summarized in the Table 6.8, Table 6.9 and Table 6.10, respectively.

TABLE 6.8 - Comparing measured and simulated current mismatches in current mirrors (nFET) for 0.5µm CMOS technology. C. Mir_1: L=1.2µm, W=102µm, ND=9, NS=9 (5.4µm/0.6µm). C. Mir_2: L=6µm, W=102µm, ND=45, NS=5 (1.2µm/0.6µm). Average of 7 test IC samples.

Methodology	**Simulated Mismatch (%)**		**Experimental Mismatch (%)**	
	C. Mir_1 (L=1.2µm)	C. Mir_2 (L=6µm)	C. Mir_1 (L=1.2µm)	C. Mir_2 (L=6µm)
Full-custom	3.22	0.02	4.88	4.26
TAT version	14.42	1.38	5.31	-0.43

TABLE 6.9 - Experimental CS amplifiers performance comparing full-custom and TAT versions, for 0.5µm CMOS technology. Average of 9 test IC samples.

Common-source Amplifier		
	Full-custom	**SOT**
V_{DD} (V) / C_L (pF)	3 / 1200	3 / 1200
A_v (dB)	33.0	29.9
f_T (KHz)	318.5	268.2
PM (o)	86.4	83.9
SR (V/µs)	0.114	0.086
V_o max (V)	2.2 / 0.7	2.0 / 0.8

TABLE 6.10 - Experimental track-and-latch comparator performance comparing full-custom and TAT versions, for 0.5µm CMOS technology. Average of 9 full-custom and 5 SOT test IC samples.

Track-Latch Comparator		
	Full-custom	**SOT**
V_{DD} (V)	3	3
f_{max} (MHz)	41.1	30.5
Sensibility (mV)	7.33	14.2

Note the comparison between simulated and measured current mismatches in Table 6.8: the predicted (simulation) mismatches are larger for the TAT simulations. However, both agree for full-custom and TAT versions and showing that the matching for TAT technique is

slightly worse due to short-channel effects and body effect (in MD transistor) present in minimum-L transistors on the SOT array.

TABLE 6.11 - Fully diff. Folded-cascode OTA-1: Experimental performance of the TAT versions, for 0.5µm CMOS technology. Average of 5 test IC samples.

Folded-Cascode Fully Diff. OTA	
	SOT version
V_{DD} (V)	3
C_L (pF)	82
A_v (dB)	59.0
f_T (MHz)	1.167
PM (o)	148
SR (V/µs)	1.177
V_{os} (mV)	9.2
V_o max (V) / V_o min (V)	2.1 / 1.1

TABLE 6.12 - Experimental 2nd-order SD performance for TAT version in 0.5µm CMOS technology. Average of 4 test IC samples.

2nd-order SDM / OSR=64 (SOT version)	
Input signal & Sampling freq.	**SNR (dB)**
Sine 5KHz / f_s = 6.9MHz	75.1
Sine 7KHz / f_s = 6.9MHz	69.1
Sine 1KHz / f_s = 1.7MHz	63.4

As expected, the performance of TAT version of the CS amplifier is poorer than the single one – Table 6.9. The DC gain is similar for both techniques and the cut-off frequency is lower. Again, measured and simulated performance is similar showing that predicted performance is correct. Similar comparison results are true for track and latch comparators – Table 6.10. Maximum switching clock frequency for TAT version is approximately 25% lower and sensibility is twice larger. However, comparing simulated (Table 5.6) and measured performance, electrical simulation had less optimistic (higher) sensibility values and super-estimated speed. The latter, due to non-realistic estimation of the parasitic effects (capacitances and resistances).

Table 6.11 and Table 6.12 show the performance results for the fully differential OTA and Second-order Sigma-Delta modulator. The performance comparison between design methodologies was hindered due to unavailable results for the full-custom version. There were

layout design errors in the full-custom version that was fabricated in 0.5µm. Layout errors were found in full-custom OTA and integrators that made these analog blocks not to work. Nonetheless, the experimental results show good performance using TAT transistors on the SOT array.

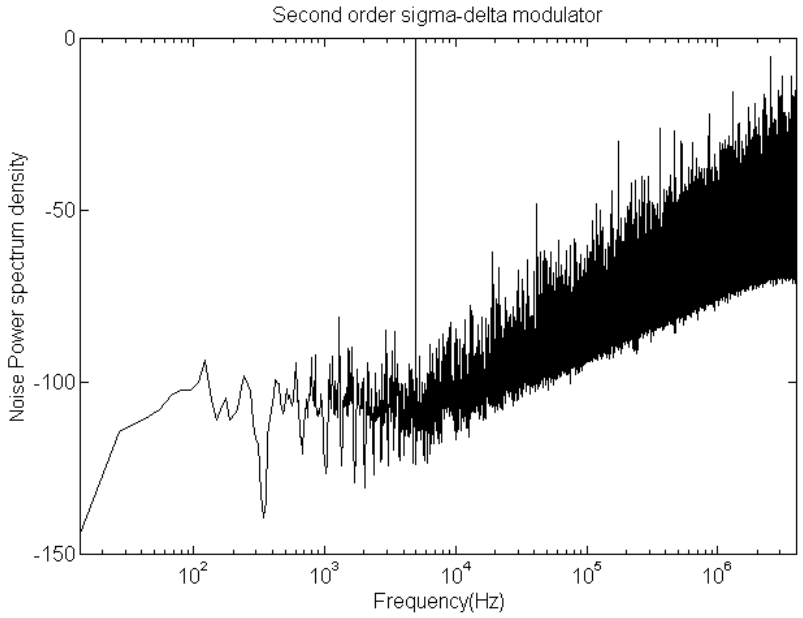


FIGURE 6.11 - Experimental Noise power spectrum density of 2nd order SDM for TAT version in 0.5µm CMOS technology. Input signal: sine wave at 5KHz; f_s=6.9MHz and OSR=64. Average of 4 test-chip samples.

The measured performance for SOT version of the fully differential OTA-1 is shown in Table 6.11. Both simulation and measurement used the externally-set bias current (I_{bias}) set to 50µA. Note that the measured DC gain is 21dB below the simulated value of poor AC parameter modeling for the simulation, by comparing Table 6.5 and Table 6.11 (experimental data). The output swing is measured as approximately 1V, which is a restriction due to the TAT topology and the bias currents set at the differential input pairs and at the folded output branches. Comparisons of f_T and slew rate are not done due to high load capacitance present in the measurement that affected overall OTA performance.

Finally, the validation of the TAT technique for analog and mixed-signal design on SOT array is shown in Table 6.12. It shows the good performance reached for the Second Order SDM in SOT methodology. Despite some parasitic effects in the measurement, the signal-to-noise ratio provides approximately 11 bits to 12 bits of resolution. The noise power spectral density is shown in Fig. 6.11. In the band-signal, the rms noise power is approximately -110dB.

7 Conclusion

This work has investigated an innovative technique for mixed-signal analog-digital design on a pre-diffused semi-custom digital array, demonstrating that the TAT approach is a good alternative for analog semi-custom ASIC applications. The use of TAT arrays and the mapping of conventional full-custom transistors to TAT are relatively straightforward. The theoretical large-signal, small-signal and noise analysis have been compared to the electrical simulations and experimental measurements. The resulting comparisons have demonstrated a good matching between the theoretical, predicted values and the TAT performance. These results have been published in several conference papers, such as [CHO99c], [CHO99b], [CHO99a], [CHO2000b], [CHO2000a], [CHO2001].

With the intention of getting better and straight insight on the TAT transistor in emulating its equivalent single transistor, a number of MOSFET devices were fabricated and tested. Test chips were fabricated with transistor structures having different TAT geometries (L, W, W/L) and their equivalent single (full-custom) MOSFETs, both in 0.5μm and 1.0μm CMOS technology. The encouraging results obtained for the TATs have shown that they are a good emulation of the single ones. Another important advantage of the TAT is that the improvement on the TAT characteristics is achieved with respect to the output conductance (section 4.3), thus warranting the use of minimum channel-length transistors for designing analog semi-custom circuits. The simulated current matching in CMOS current mirrors, shown in section 5.1, is also a sign of better output conductance control in TATs, due to statistical averaging among dozens of unit transistors.

The transconductance reduction in conduction and saturation regions (section 4.3 – equation 4.3.5) of the TAT can be accounted for by proper design of the equivalent W/L (MS ratio). The short channel effects (section 4.2 and section 4.5) can be put to advantage for low supply-voltages operation of an analog block in a semi-custom digital VLSI/ULSI. The most important concern about TAT device is the noise performance (section 4.4 and section 5.4). One has to deal with the demonstrated noise sources of the TAT transistor. It is noisier than its equivalent single transistor counterpart, since its inherent minimum-L transistors are being

employed in the association. However, by using larger numbers of ND or NS in the MD and MS association, respectively, the bad TAT characteristics with respect to noise can be compensated, while keeping the same equivalent ratio W/L. For low noise applications, large area associations of tens or possibly few hundreds unit transistors are required. Although, the total noise power is larger and some natural limitations exist (body effect, minimum-L and large silicon area), TAT transistors on SOT array have presented good performance.

Several analog circuits (current mirrors, single stage amplifiers, track-and-latch comparators, folded-cascode OTAs) have also been designed and fabricated. In chapter 5 and 6, the folded-cascode OTA implemented on SOT array (1.0µm and 0.5µm) points toward a good TAT performance and implementing fully semi-custom analog circuits employing only TAT devices.

The TAT gains and phase margins (section 5.2 and 6.8) were stable for the experimental loads, even in the presence of additional intermediate internal node. The parasitic capacitances in TAT devices are similar to the equivalent single one. The combinations of the main capacitances that influence the TAT AC performance are the MS gate-to-source, MS gate-to-drain, MD gate-to-source and MD gate-to-drain capacitances. The TAT amplifier gain, as result of the cascode effect, can be made larger than the single transistors amplifier by adjusting to higher values the MD output conductance and MS transconductance. The restriction is that the MD and MS parallel associations of unit transistors must be kept trapezoidal: MD larger than MS.

No major penalties prevent the mixed-signal and analog systems on a digital array, whose main disadvantages were addressed in this thesis. The principle of the TAT has shown to have a good trade-off, for a given application, between performance, cost, and prototyping time turnaround. Additionally, as already shown herein, it is not restricted only to pre-diffused arrays, i. e., it can be applied advantageously even in analog full-custom methodology. That establishes the fast analog layout design (fast prototyping) and the most important advantage is the very inexpensive mixed-signal analog-digital design with low cost digital technology.

Next steps of this work will be: (1) parameters extraction for comparison between simulation and experimental of the TAT and single transistor; (2) experimental noise analysis in the single TAT; (3) RF modeling of the TAT; (4) full-custom versions design of Sigma-Delta modulator and OTA; and (5) development of automatic generator for TAT and layout (positioning & routing on the SOT array).

Appendix A Experimental Measurements: MOS Transistors

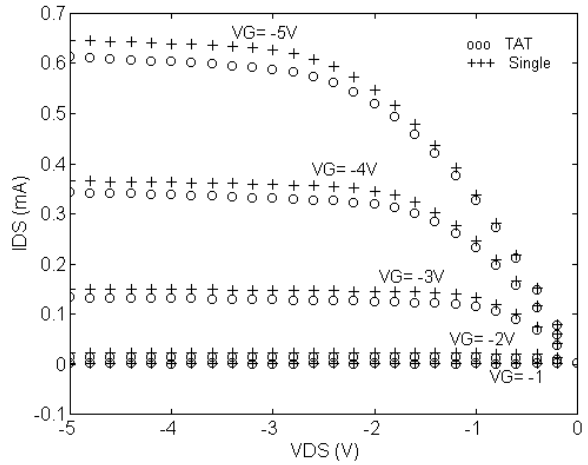
Experimental plots presenting TAT versus single transistors and comparisons performed on Transistor test-structure chips containing TAT and single transistors of Table 4.1.

The plots are for N and P type transistors for the following device characteristics:

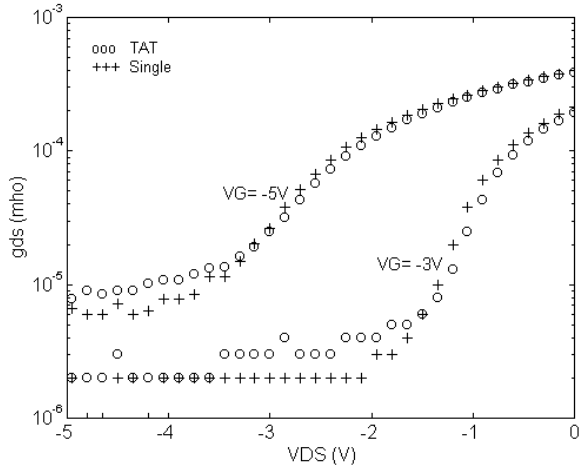
- Drain current ID x VD and Output conductance gds x VD
- Drain current ID x VG and SQRT(ID) x VG
- Drain current ID x VS and Current-transconductance ID/gm x ID
- TAT comparisons: Simulated x Measured

The data in this appendix is taken from samples in the following run:

- Technology: 1.0μm digital CMOS from ES2 foundry
- Number of Test-chips: 9 samples
- Number of transistors per chip: 4 TATs and 4 singles
- Number of P type: 2 TATs and 2 singles
- Number of N type: 2 TATs and 2 singles



(a)



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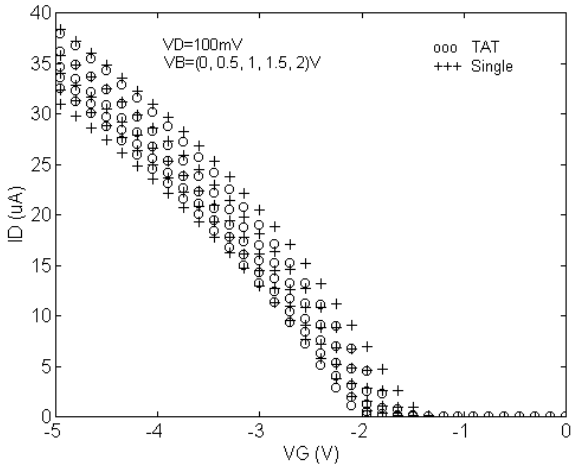

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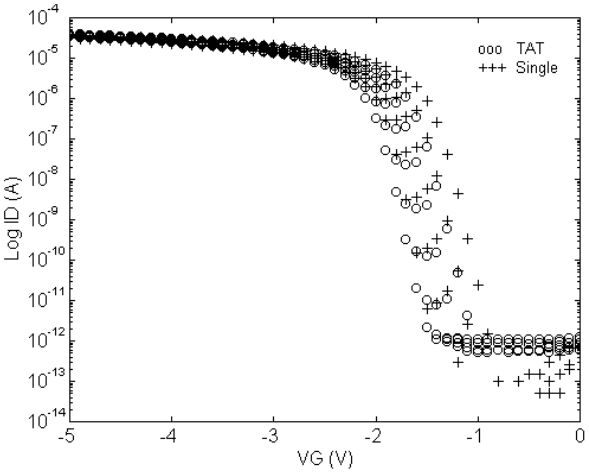
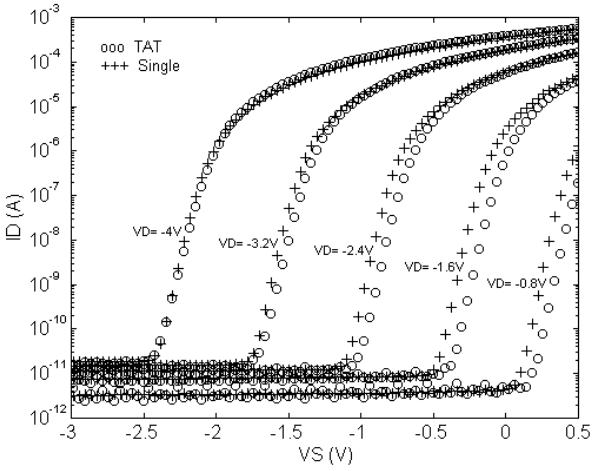
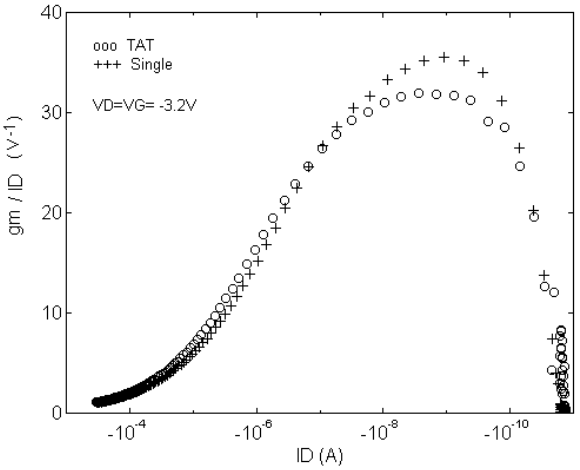


(d)

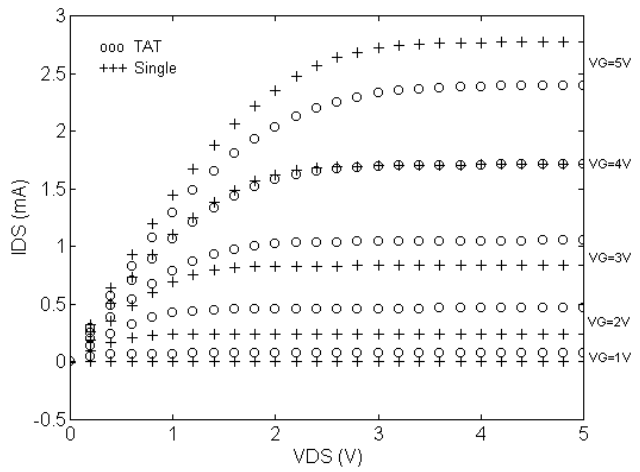


(e)

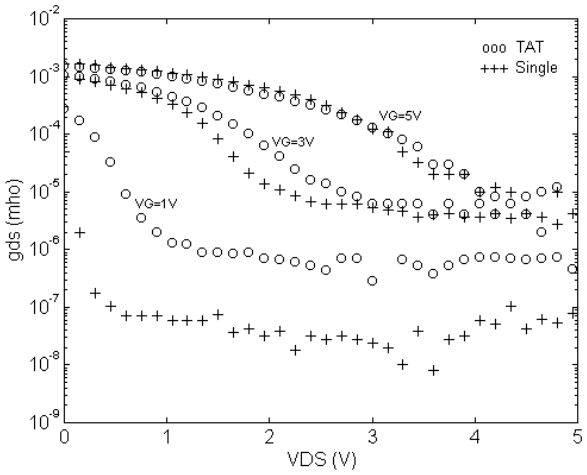


(f)

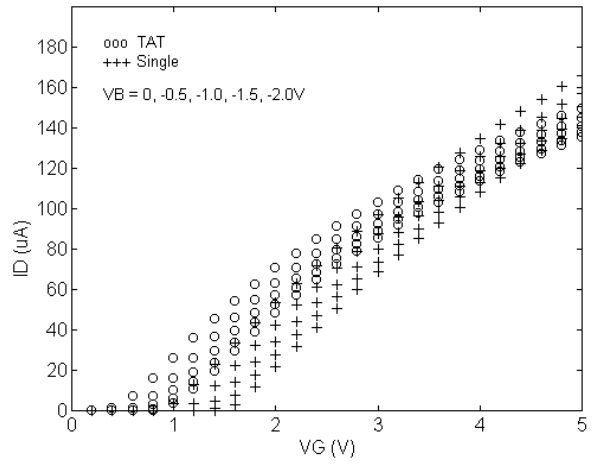
FIGURE A-1 - Experimental Single-1 (W/L=30/5) vs. TAT-1 (Table 4.1) PMOS transistors comparison in 1.0µm technology. (a) IDxVD characteristics (VB=0V). (b) Output conductance at VG=3V and 5V. (c) IDxVG characteristics with fixed VD=-100mV and substrate voltage VB varying from 0V to 2V (step -0.5V). (d) log (ID)xVG. (e) Saturated IDxVS characteristics at VD=VG=-0.8,-1.6..,-4V. (f) gm/IDxID at VD=VG=-3.2V.



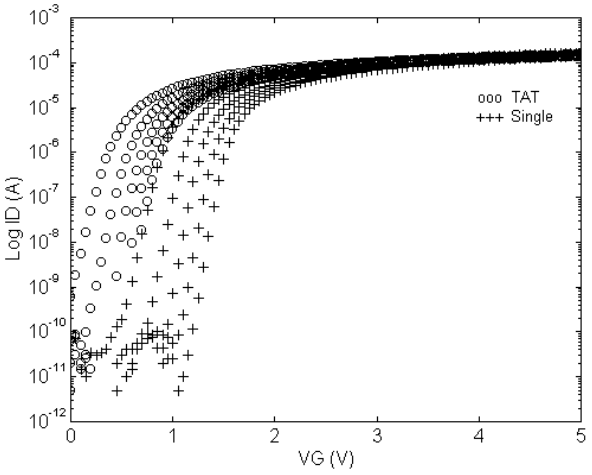
(a)



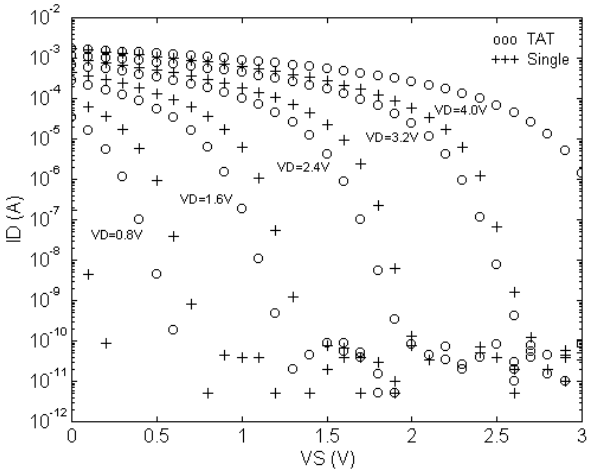
(b)



(c)



(d)



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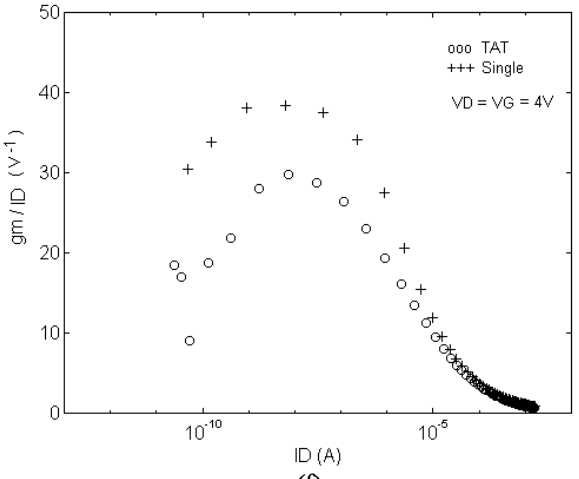


(f)

FIGURE A-2 - Experimental Single-2 (W/L=30/5) vs. TAT-2 (Table 4.1) NMOS transistors comparison 1.0µm technology. (a) IDxVD characteristics (VB=0V). (b) Output conductance at VG=1, 3, 5V. (c) IDxVG characteristics with fixed VD=100mV and substrate voltage VB varying from 0V to -2V (step 0.5V). (d) log(ID)xVG. (e) Saturated IDxVS characteristics at VD=VG=0.8, 1.6,..,4V. (f) gm/Idx ID at VD=VG=4V.

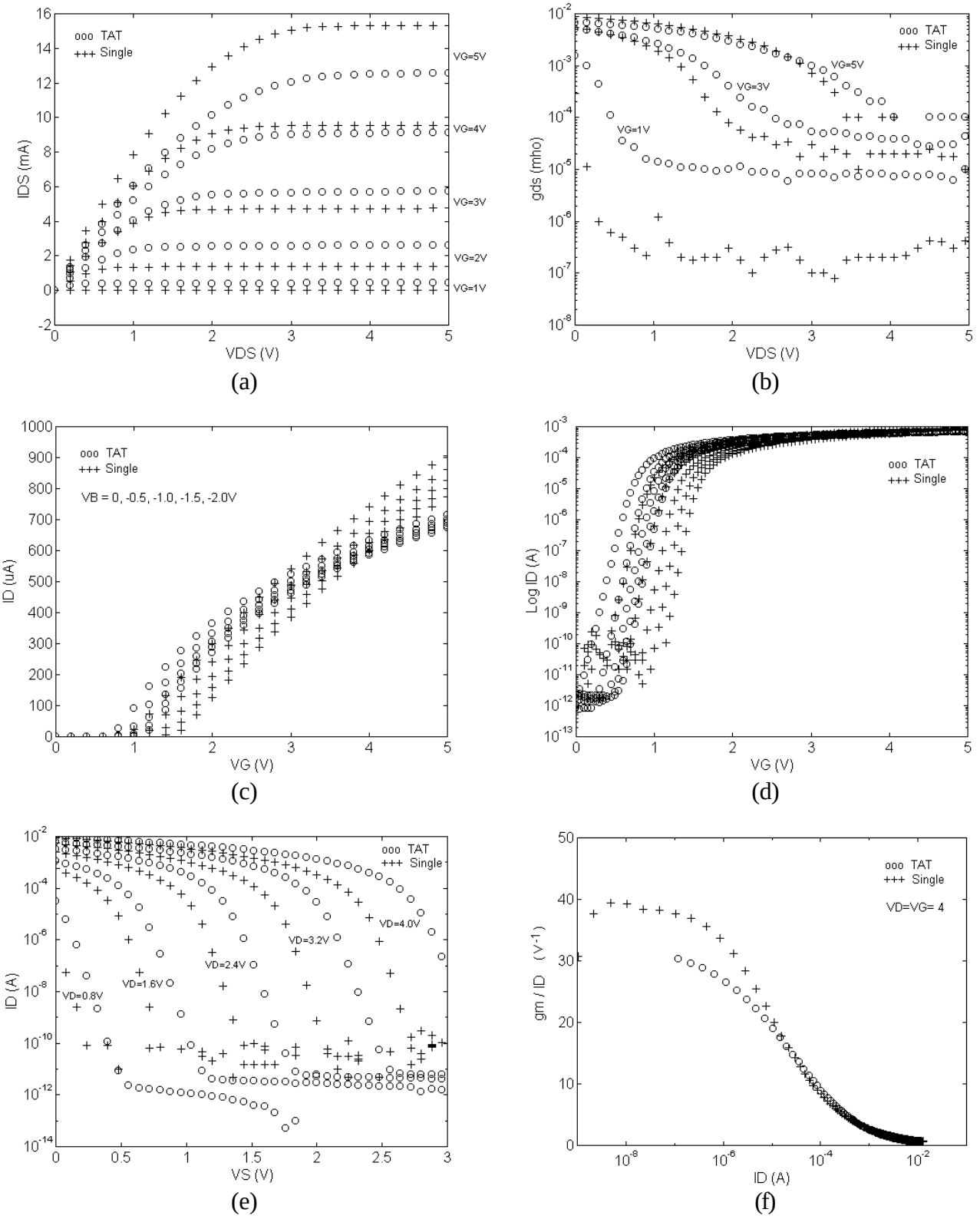


FIGURE A-3 - Experimental Single-3 (W/L=170/5) vs. TAT-3 (Table 4.1) NMOS transistors comparison 1.0µm technology. (a) IDxVD characteristics (VB=0V). (b) Output conductance at VG=1, 3, 5V. (c) IDxVG characteristics with fixed VD=100mV and substrate voltage VB varying from 0V to -2V (step 0.5V). (d) log(ID)xVG. (e) Saturated IDxVS characteristic at VD=VG=0.8, 1.6,…, 4V. (f) gm/IDxID at VD=VG=4V.

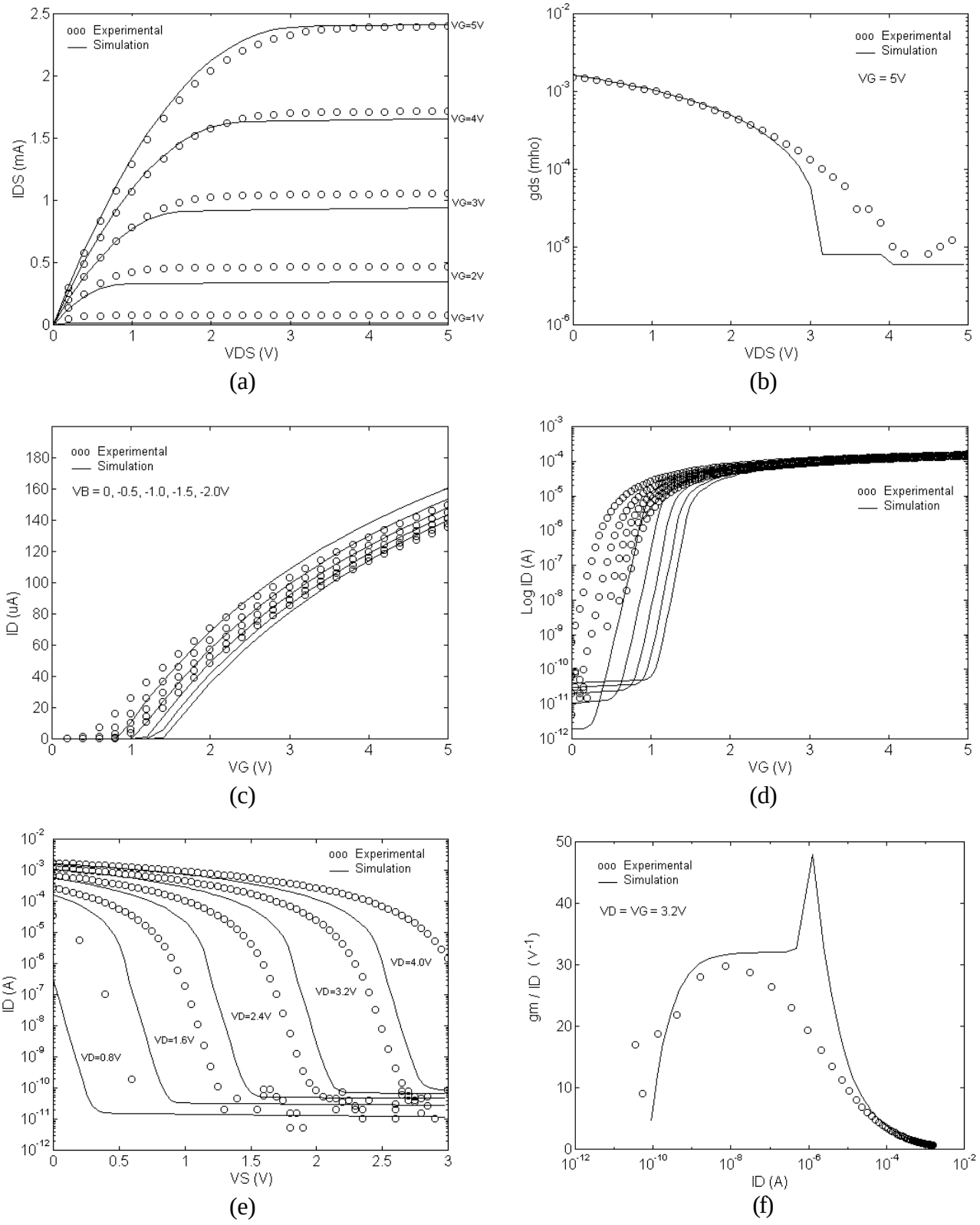


FIGURE A-4 - Experimental vs. Simulation (HSpice, level 6). TAT-2 NMOS transistor (effective W/L=30/5). (a) IDxVD characteristics (VB=0V). (b) Output conductance at VG=5V. (c) IDxVG characteristics at fixed VD=100mV. (d) (*log* ID)xVG. (e) IDxVS characteristics (VD=VG). (f) gm/IDxID at VD=VG=3.2V.

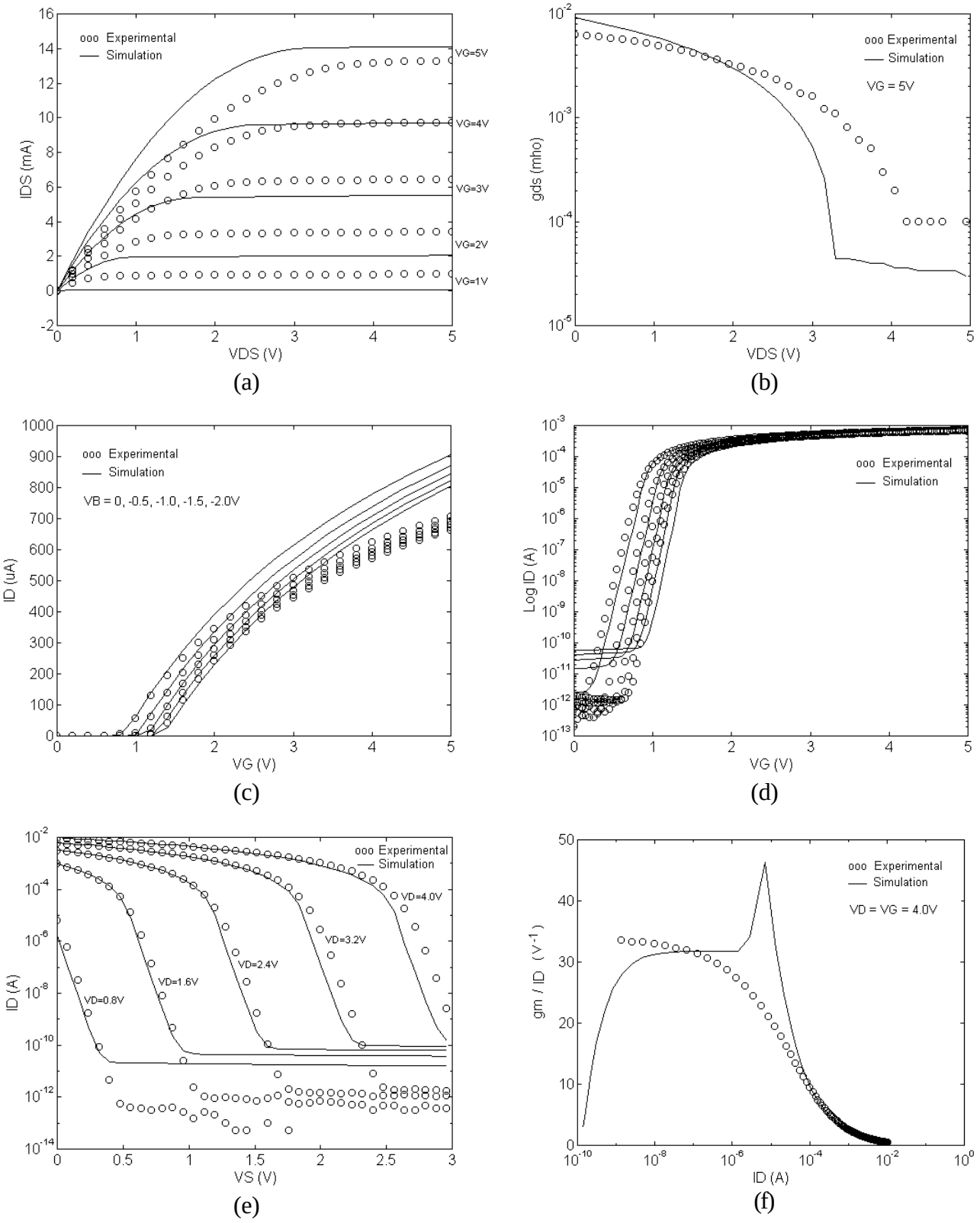


FIGURE A-5 - Experimental vs. Simulation (HSpice, level 6). TAT-3 NMOS transistor (effective W/L=170/5). (a) IDxVD characteristics (VB=0V). (b) Output conductance at VG= 5V. (c) IDxVG characteristics at fixed VD=100mV. (d) (*log* ID)xVG. (e) IDxVS characteristics (VD=VG). (f) gm/IDxID at VD=VG=4V.

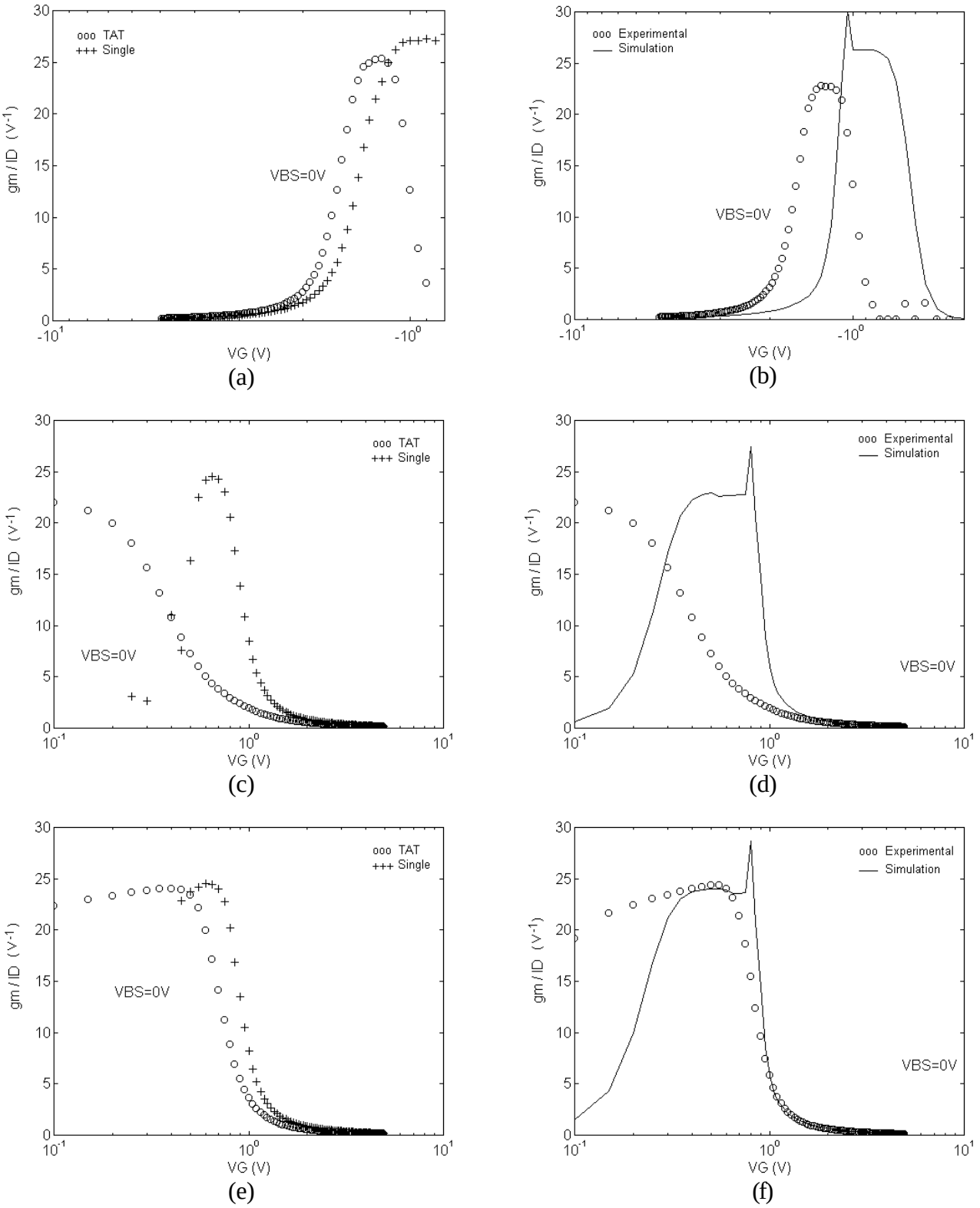
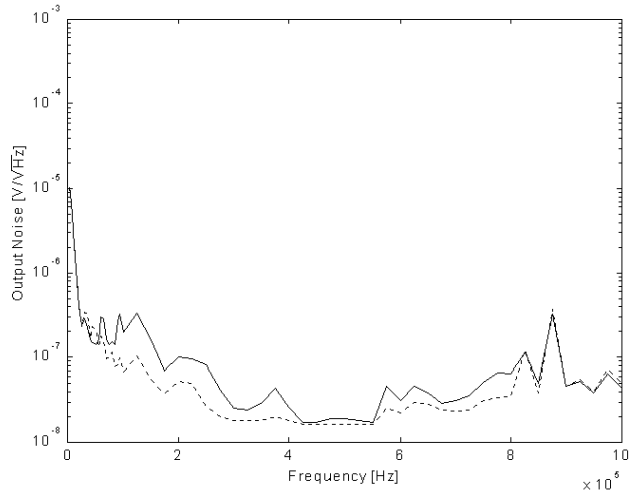


FIGURE A-6 - gm/IDxVG characteristics comparison with fixed VD=100mV and VB=0V for 1.0µm technology. For PMOS transistors: (a) Experimental Single-1 (W/L=30/5) vs. TAT-1, (b) Experimental vs. Simulation TAT-1. For NMOS transistors: (c) Experimental Single-2 (W/L=30/5) vs. TAT-2, (d) Experimental vs. Simulation TAT-2. (e) Experimental Single-3 (W/L=170/5) vs. TAT-3, (f) Experimental vs. Simulation TAT-3.

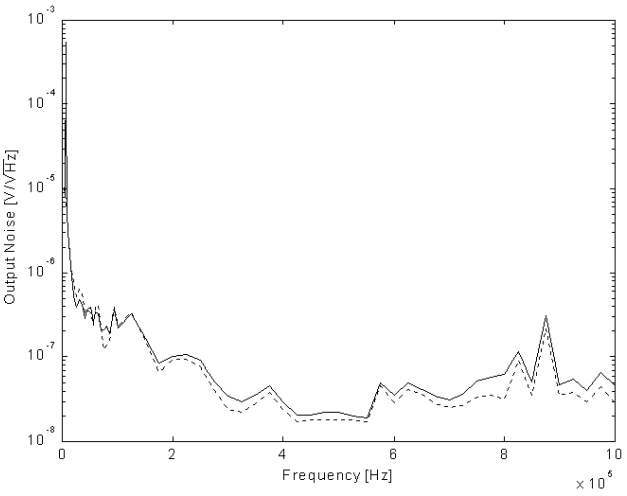
Appendix B Experimental Noise Power in Folded-cascode OTA

Output noise power measured in OTAs implemented in both SOT and Full-custom methodology.

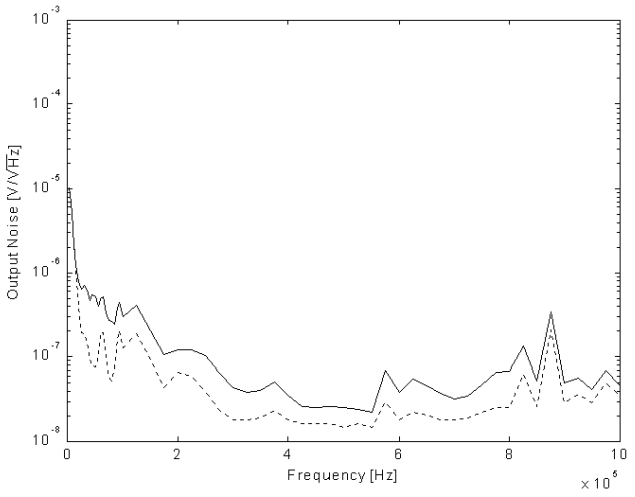
- Technology: 1.0μm digital CMOS from ES2 foundry
- Analog circuit: folded-cascoded single-ended CMOS OTAs
- Number of test-chips: 5
- Number of OTAs in SOT array: 5
- Number of OTAs in Full-custom: 5



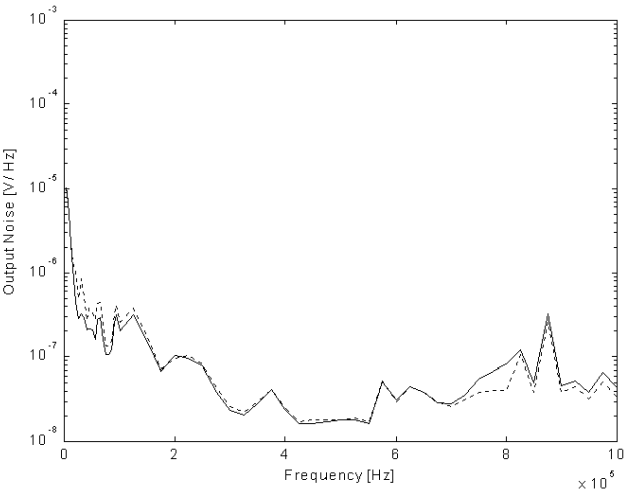
(a)



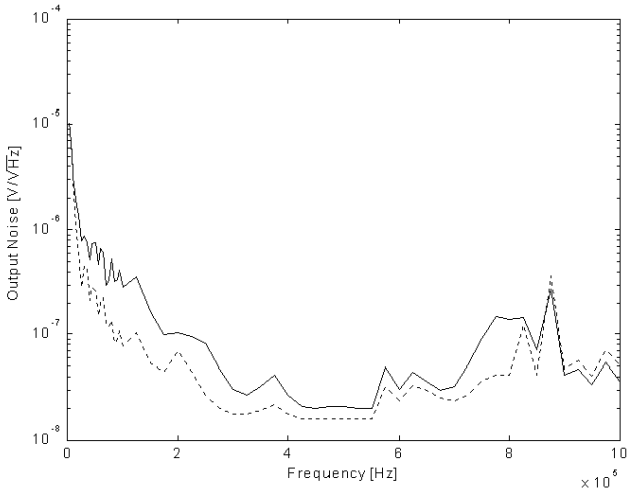
(b)



(c)



(d)



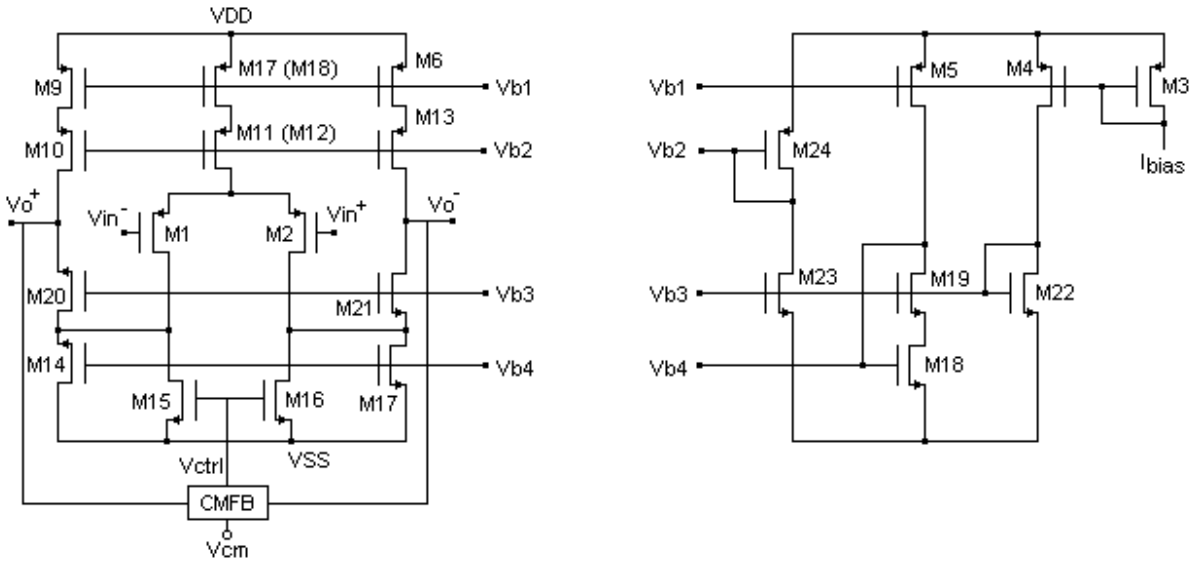
(e)

FIGURE B-1 - Experimental output noise power in OTA. Full-custom (solid) and SOT (dotted). a) Sample-1. b) Sample-2. c) Sample-3. d) Sample-4. (e) Sample-5.

Appendix C Fully-Differential Folded-Cascode OTA

Sized and simulated OTA-1 and OTA-2 in both SOT and Full-custom methodology:

- Technology: AMI 0.5µm CMOS double poly, triple metal from MOSIS foundry
- OTA schematic
- OTA-1 and OTA-2 sized transistors: Singles and TATs
- Electrical simulations (Pspice): DC gain, Noise power, Common-mode feedback and DC gain variation vs. Ouput swing



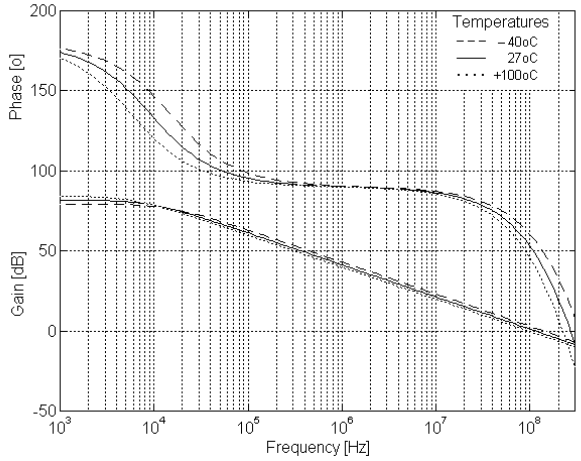
Fully differential OTA and bias circuit schematics (same of Fig. 6.6 – section 6.6).

TABLE C-1 - Designed single and TAT transistor sizes for the OTA-1 in full-custom and SOT array methodology (prime superscripts indicate TAT version). Values for L_{eq} and $(W/L)_{eq}$ are the electrical equivalent length for the TAT associations.

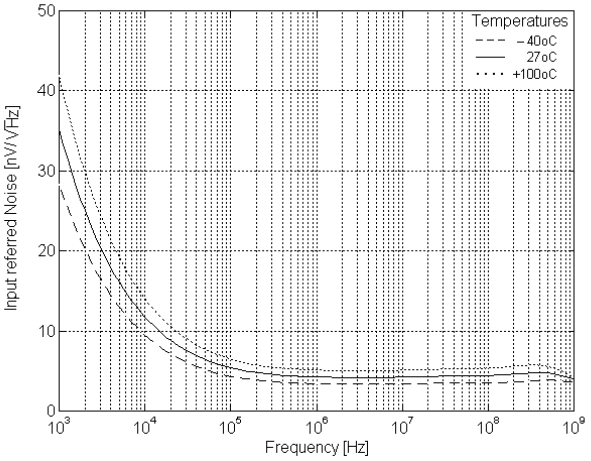
OTA-1 (0.5µm CMOS technology)				**Transistor sizes**	
Transistor	**W(µm)**	**L(µm) or L_{eq} (µm)**	**W/L or $(W/L)_{eq}$**	**ND**	**NS**
M1,M2	1100	1.25	880	-	-
M1',M2'	1162	1.32	880.3	99x(11.7µm/0.6µm)	83x(11.7µm/0.6µm)
M3,M4	100	3	33.33	-	-
M3',M4'	93.6	3	31.2	8x(11.7µm/0.6µm)	2x(11.7µm/0.6µm)
M5	200	3	66.67	-	-
M5'	187.2	3	62.4	16x(11.7µm/0.6µm)	4x(11.7µm/0.6µm)
M6,M7, M8,M9	600	3	200	-	-
M6',M7', M8',M9'	608.4	3	202.8	52x(11.7µm/0.6µm)	13x(11.7µm/0.6µm)
M10,M11, M12,M13	600	1	600	-	-
M10',M11', M12',M13'	719.2	1.2	599.3	63x(11.7µm/0.6µm)	60x(11.7µm/0.6µm)
M14,M17	400	4	100	-	-
M14',M17'	409.6	4.1	99.9	76x(5.4µm/0.6µm)	13x(5.4µm/0.6µm)
M15,M16	200	4	50	-	-
M15',M16'	213.6	4	53.4	39x(5.4µm/0.6µm)	7x(5.4µm/0.6µm)
M18	100	4	25	-	-
M18'	102	4	25.5	85x(1.2µm/0.6µm)	15x(1.2µm/0.6µm)
M19	100	2	50		
M19'	99.7	2	49.85	18x(5.4µm/0.6µm)	8x(5.4µm/0.6µm)
M20,M21	350	2	175	-	-
M20',M21'	350.6	2	175.3	64x(5.4µm/0.6µm)	28x(5.4µm/0.6µm)
M22,M23	12	4	3	-	-
M22',M23'	13.5	4	3.38	11x(1.2µm/0.6µm)	2x(1.2µm/0.6µm)
M24	24	4	6	-	-
M24'	27.1	4	6.77	22x(1.2µm/0.6µm)	4x(1.2µm/0.6µm)

TABLE C-2 - Designed single and TAT transistor sizes for the OTA-2 in full-custom and SOT array methodology (prime superscripts indicate TAT version). Values for L_{eq} and $(W/L)_{eq}$ are the electrical equivalent length for the TAT associations.

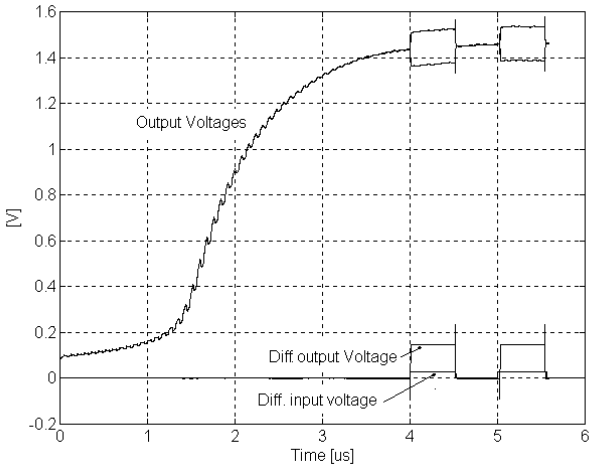
OTA-2 (0.5µm CMOS technology)				**Transistor sizes**	
Transistor	**W(µm)**	**L(µm) or L_{eq} (µm)**	**W/L or $(W/L)_{eq}$**	**ND**	**NS**
M1,M2	100	1.25	80	-	-
M1',M2'	93.9	1.29	72.8	8x(11.7µm/0.6µm)	7x(11.7µm/0.6µm)
M3,M4	10	3	3.33	-	-
M3',M4'	12	3.6	3.33	10x(1.2µm/0.6µm)	2x(1.2µm/0.6µm)
M5	20	3	6.67	-	-
M5'	24	3.6	6.67	20x(1.2µm/0.6µm)	4x(1.2µm/0.6µm)
M6,M7, M8,M9	60	3	20	-	-
M6',M7', M8',M9'	62.8	2.1	29.9	52x(1.2µm/0.6µm)	21x(1.2µm/0.6µm)
M10,M11, M12,M13	30	0.6	50	-	-
M10',M11', M12',M13'	42.1	0.6	70.2	-	3x(11.7µm/0.6µm)
M14,M17	40	4	10	-	-
M14',M17'	40.8	4	10.2	34x(1.2µm/0.6µm)	6x(1.2µm/0.6µm)
M15,M16	22	2	11	-	-
M15',M16'	22.2	2	11.1	18x(1.2µm/0.6µm)	8x(1.2µm/0.6µm)
M18	10	4	2.5	-	-
M18'	13.5	4	3.38	11x(1.2µm/0.6µm)	2x(1.2µm/0.6µm)
M19	10	2	5		
M19'	11.1	2	5.54	9x(1.2µm/0.6µm)	4x(1.2µm/0.6µm)
M20,M21	35	2	17.5	-	-
M20',M21'	33.6	2	16.8	28x(1.2µm/0.6µm)	12x(1.2µm/0.6µm)
M22,M23	4	4	1	-	-
M22',M23'	6.68	4	1.67	5x(1.2µm/0.6µm)	1x(1.2µm/0.6µm)
M24	8	4	2	-	-
M24'	13.5	4	3.38	11x(1.2µm/0.6µm)	2x(1.2µm/0.6µm)



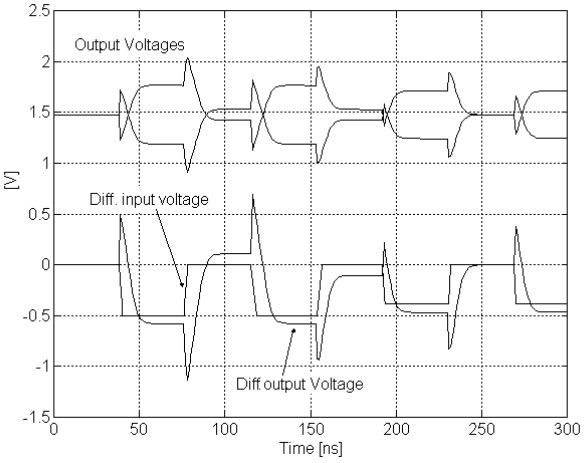
(a)



(b)



(c)



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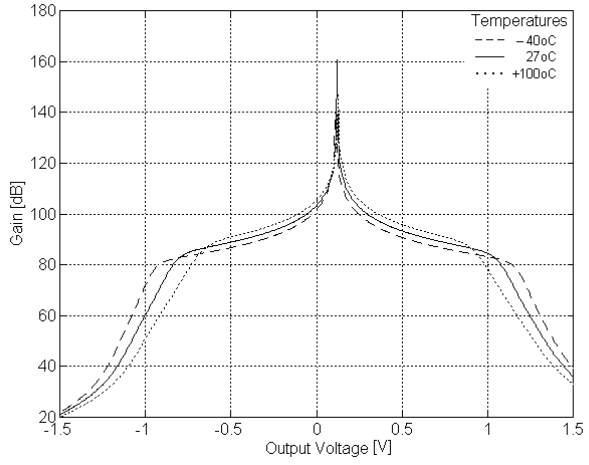
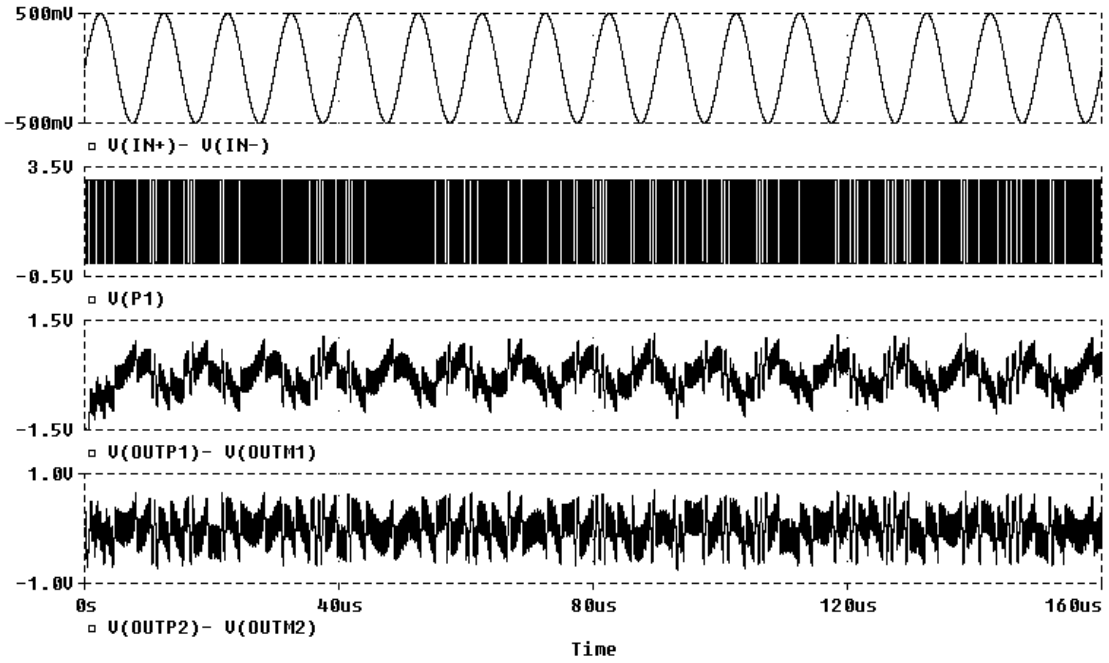


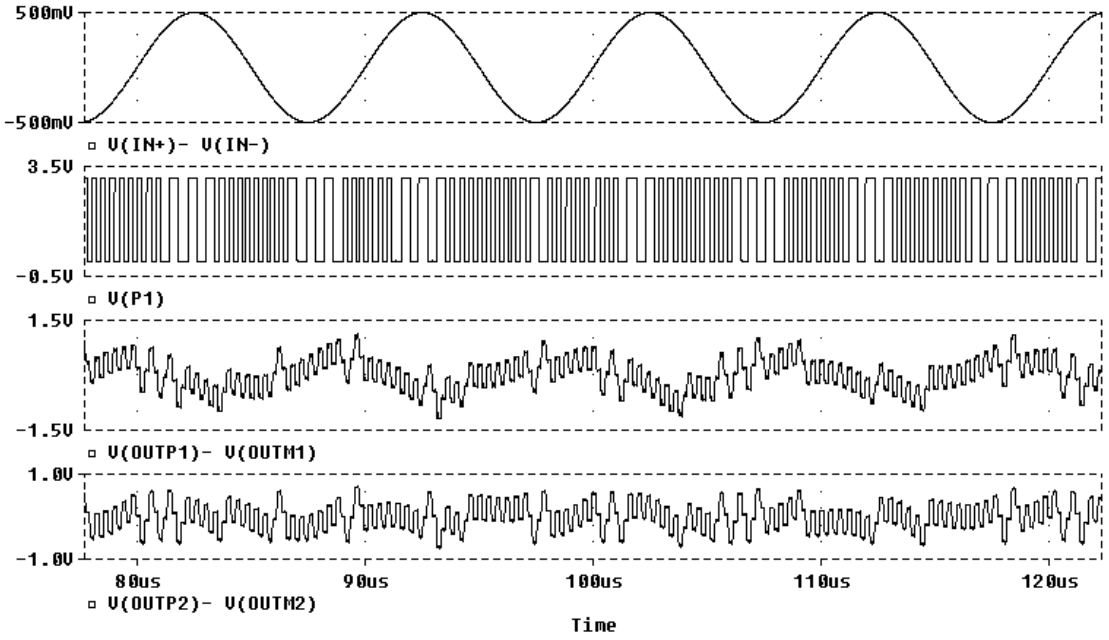
(e)

FIGURE C-1 - Simulated performance of OTA-1. Fully-differential folded-cascode OTA in full-custom for 0.5µm CMOS technology. a) DC gain and phase. b) Total input referred noise. c) Common-mode feedback. Differential input and output voltages. V_{cm}=1.5V, V_{DD}=3V. d)Transient response. e) DC gain variation with output voltage swing.

Appendix D SD Modulator Simulation and ICs (Full-custom vs. SOT)



(a)



(b)

FIGURE D-1 - Simulated transient performance of the 2nd-Order SD modulator. (a) *V(IN+)-V(IN-)*= diff. input, *V(P1)*= digital output, *V(OUTP1)-V(OUTM1)*= first integ. diff. output, *V(OUTP2)-V(OUTM2)*= second integ. diff. output. (b) Zoom-in of Fig. D-1a.

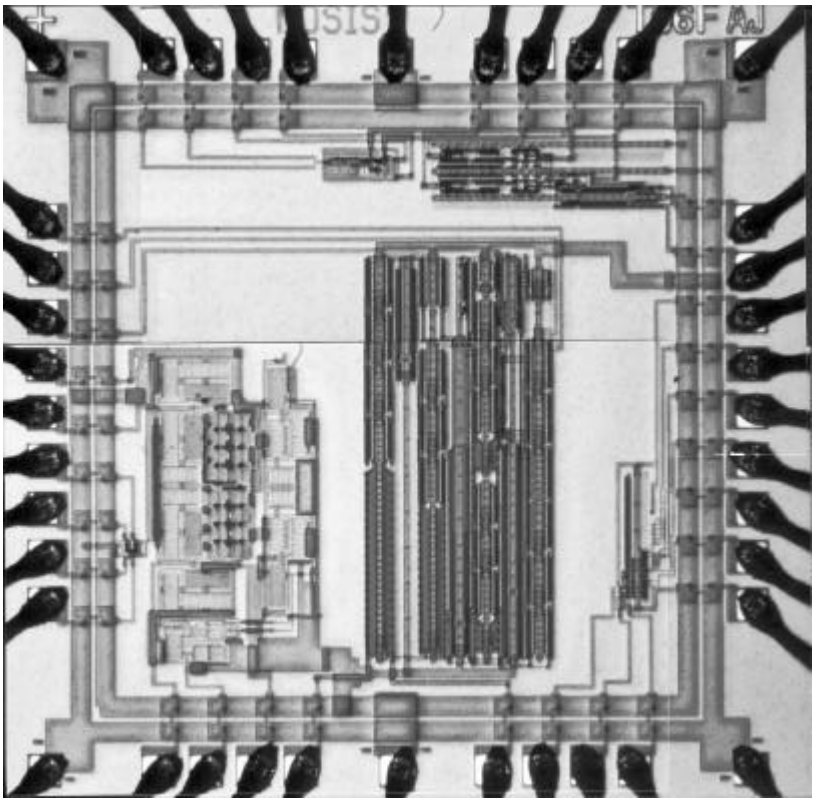


FIGURE D-2 - Die photo: Test-chip1 (0.5µm technology); full-custom and SOT array versions of the OTA-1, Comparator and Transistor-structures.

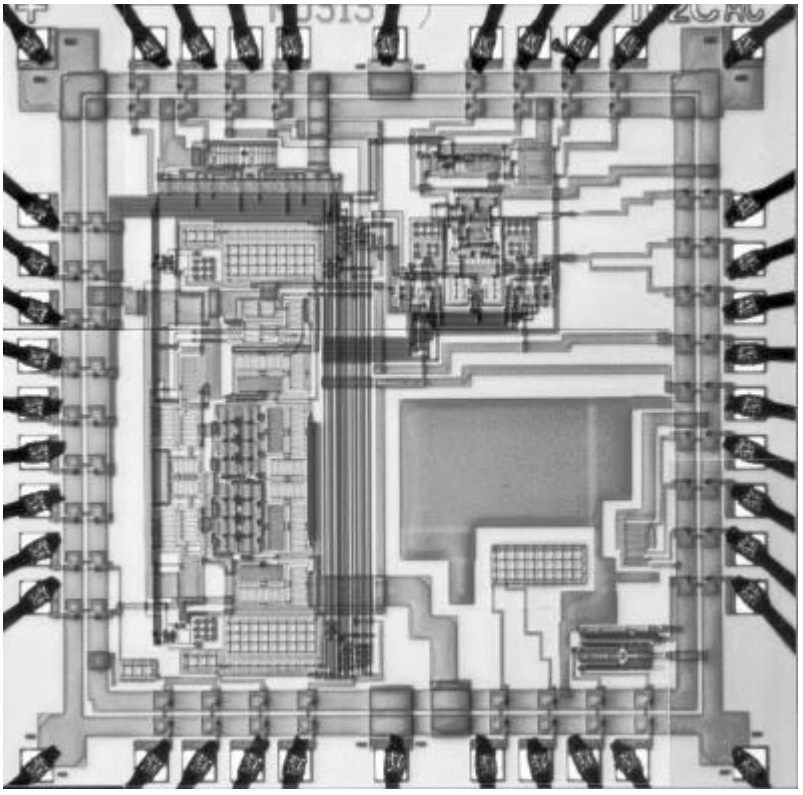


FIGURE D-3 - Die photo: Test-chip2 (0.5µm technology); full-custom version of 2nd-Order Sigma-Delta modulator and Common-source amplifier.

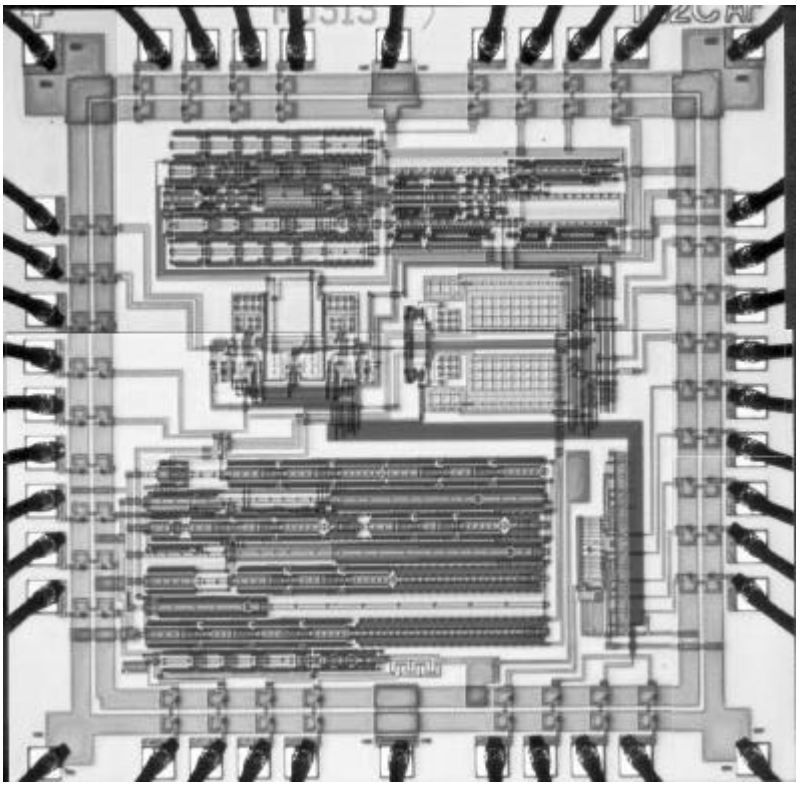


FIGURE D-4 - Die photo: Test-chip3 (0.5µm technology); SOT array version of 2nd-Order Sigma-Delta modulator and Current mirrors.

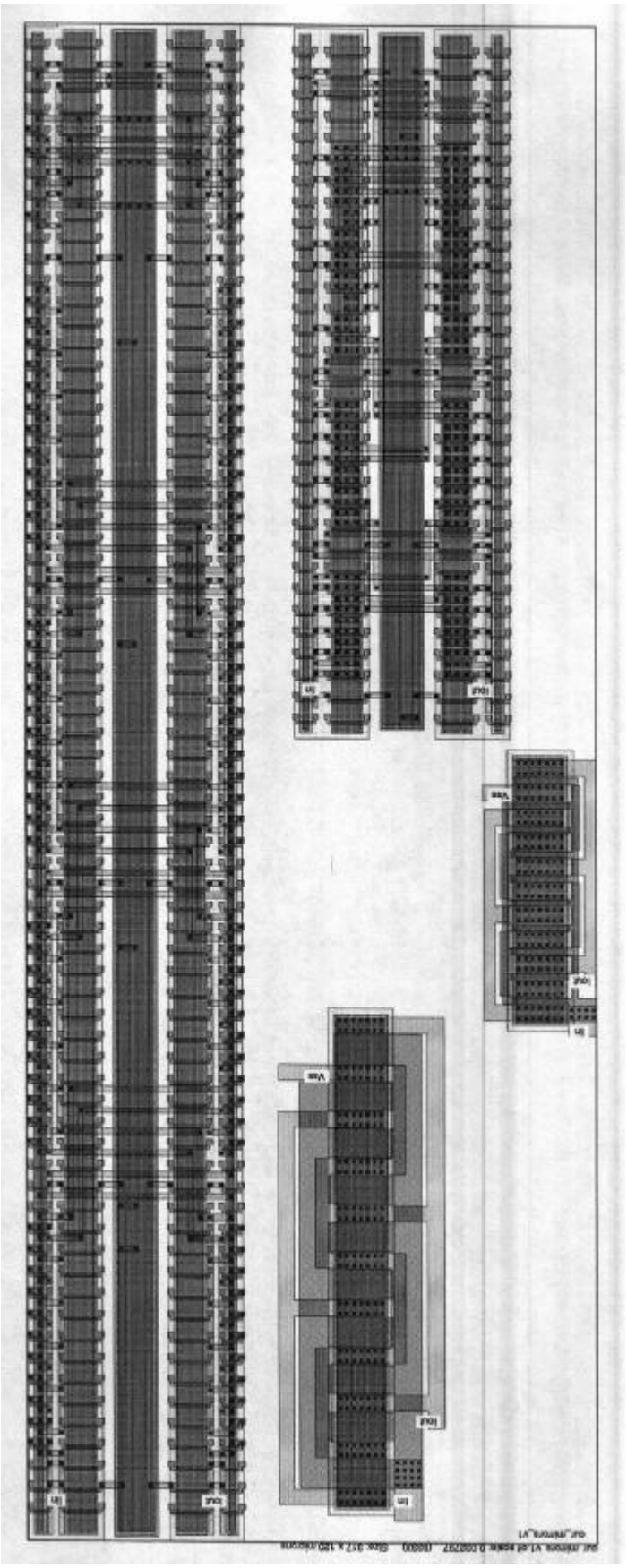


FIGURE D-5 - Current mirrors: full-custom and SOT layout (0.5µm technology).

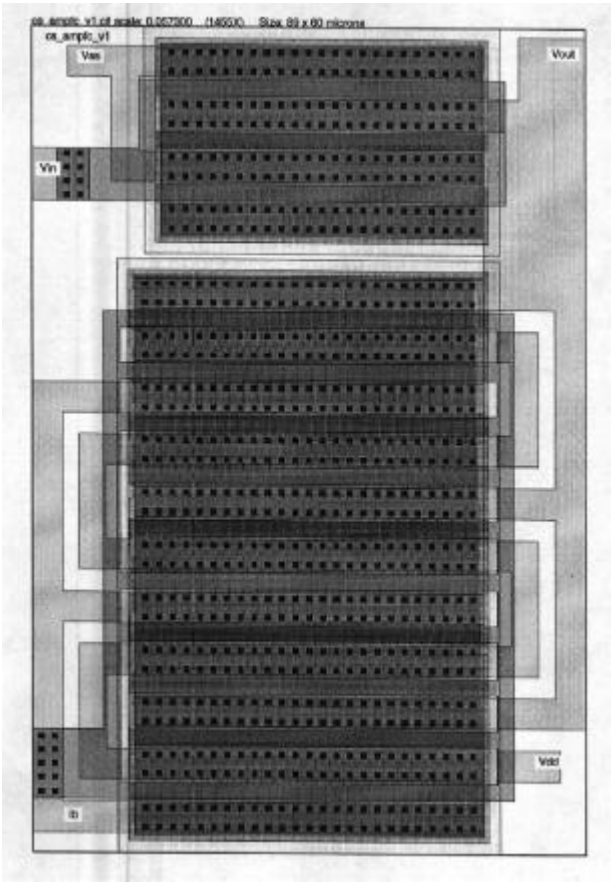
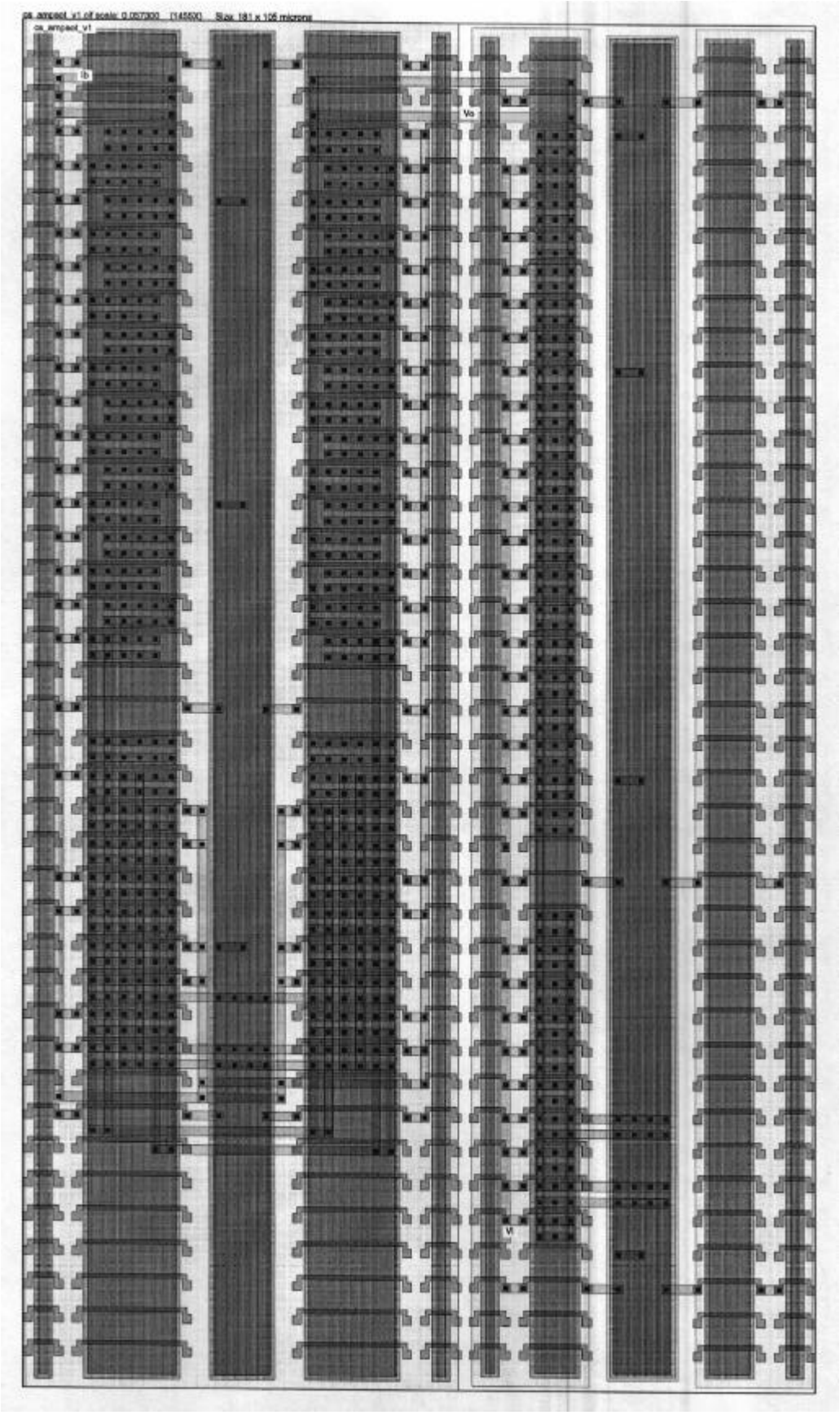


FIGURE D-6 - CS amplifier layout (0.5µm technology): (a)full-custom (b)SOT array.



(b)

Figure D-6: SOT array layout.

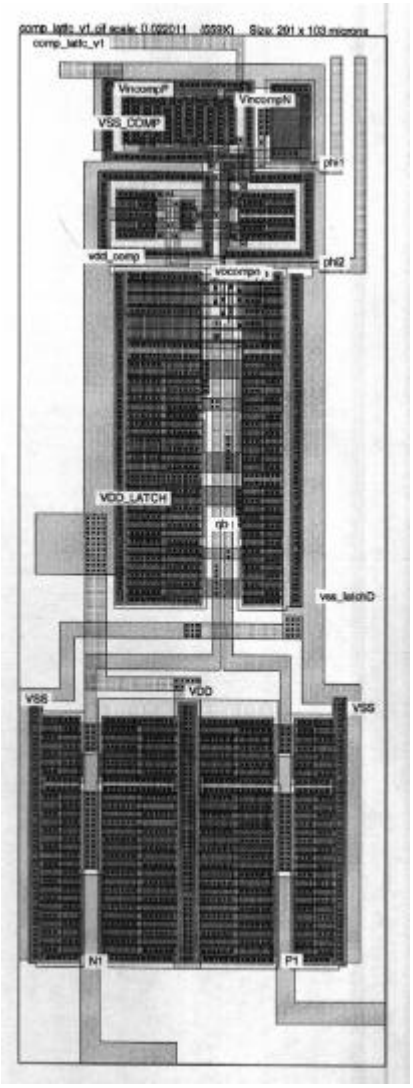
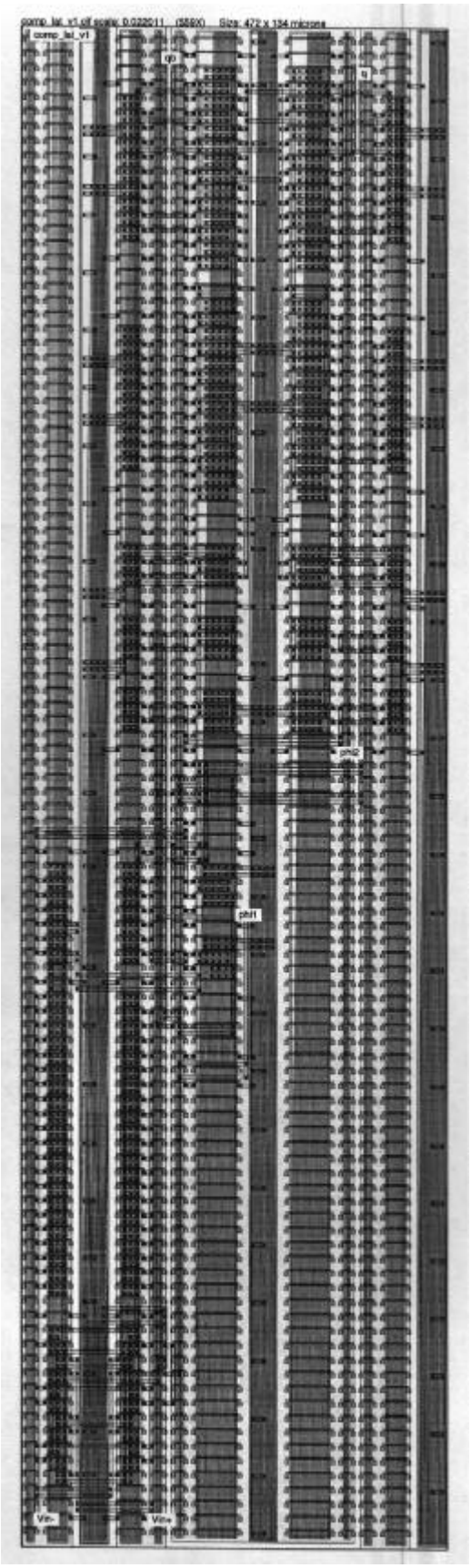


FIGURE D-7 - Comparator layout (0.5µm technology): (a)full-custom (b)SOT array.



(b)

Figure D-7: SOT array layout.

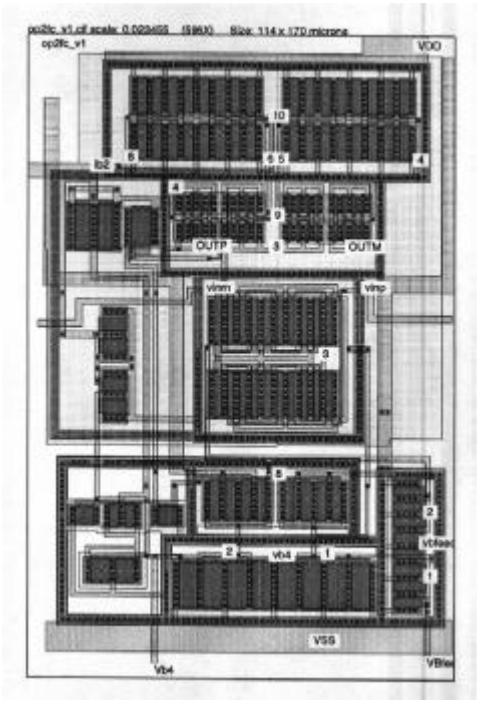
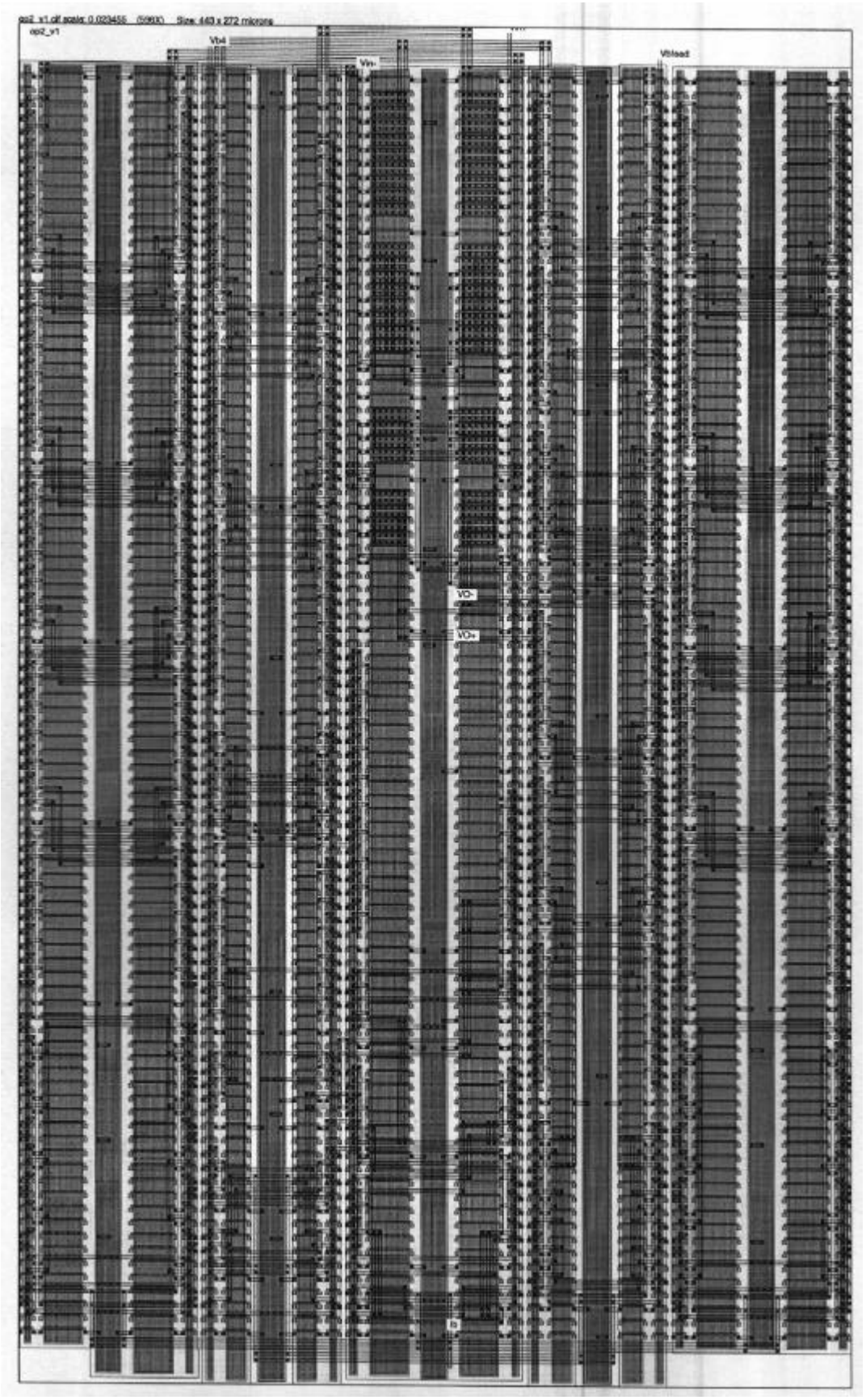


FIGURE D-8 - OTA-2 layout (0.5µm technology): (a)full-custom (b)SOT array.



(b)

Figure D-8: SOT array layout.

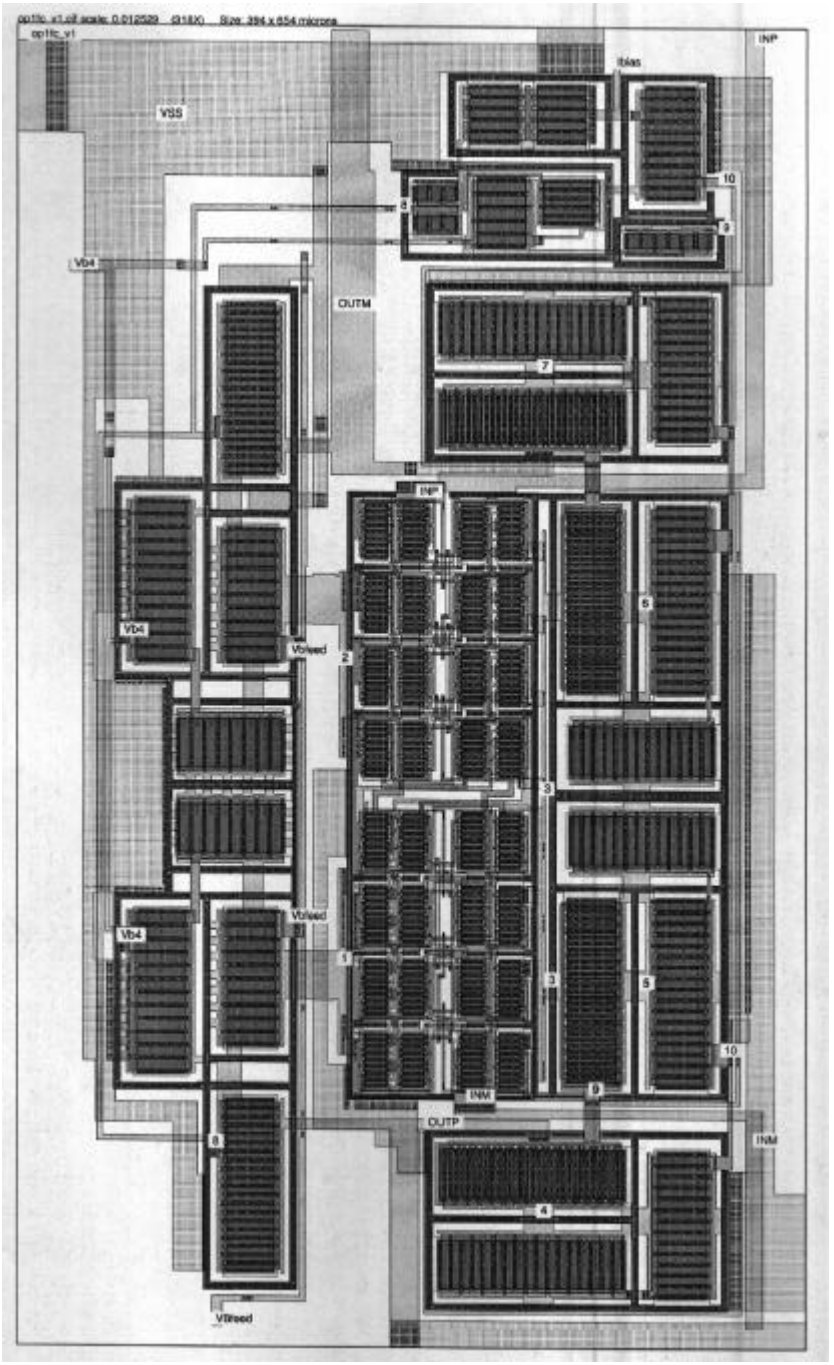
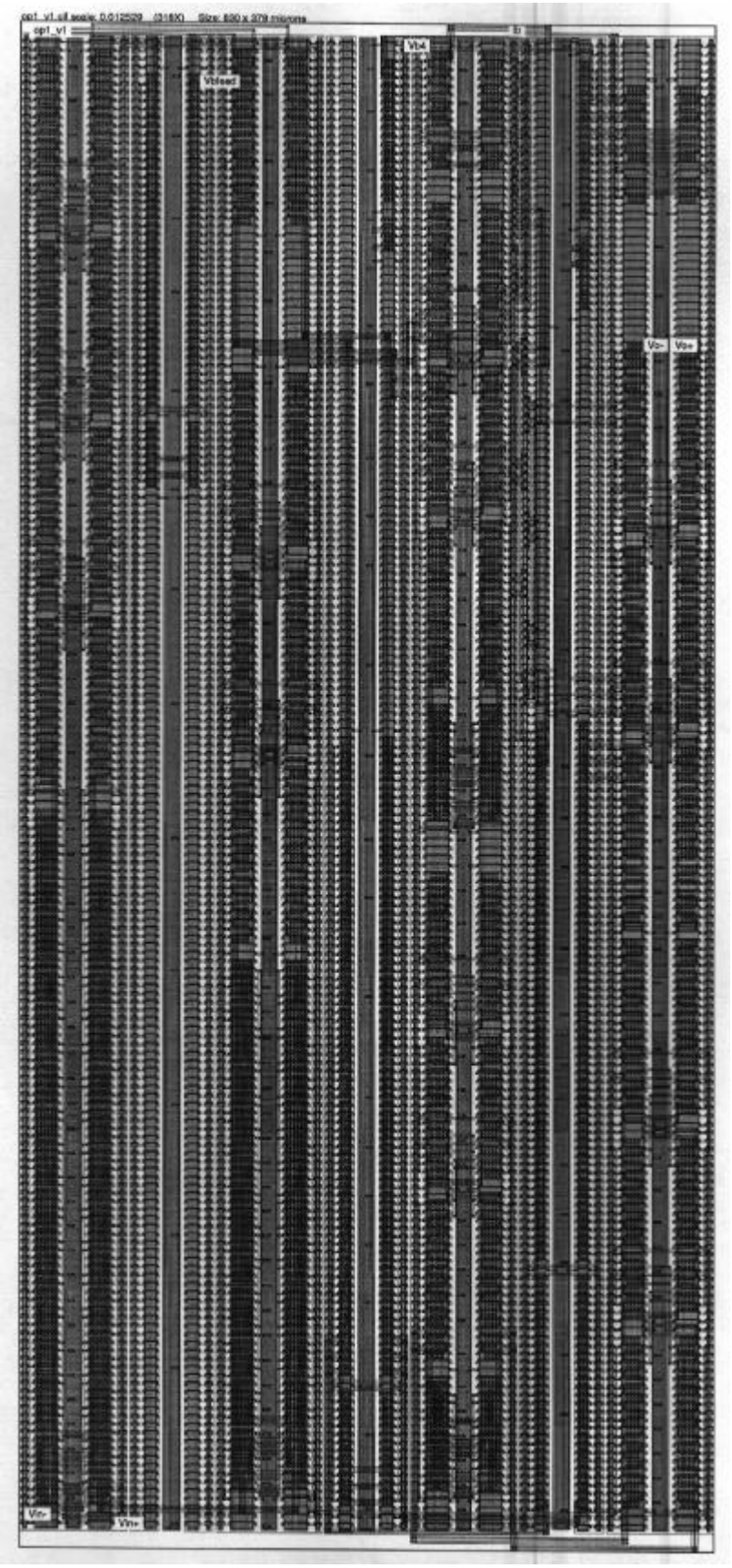


FIGURE D-9 - OTA-1 layout (0.5µm technology): (a)full-custom (b)SOT array.



(b)

Figure D-9: SOT array layout.

Appendix E Summary in Portuguese (Resumo da Tese)

Projeto de Circuitos Mistos Analógico-Digitais Sobre Matriz Pré-Difundida Digital Aplicando a Associação Trapezoidal de Transistores

1 Introdução

1.1 Motivação

As perspectivas de aumento de demanda por produtos eletrônicos sofisticados tem gerado alta competição no mercado. Como consequência, indústrias eletrônicas vêm incorporando continuamente características avançadas em seus produtos. Desde a criação dos circuitos integrados (CIs), centenas de milhares de equipamentos e máquinas miniaturizadas vêm sendo desenvolvidos, os quais progressivamente se tornam sofisticados e modernos devido às tecnologias de integração VLSI (*Very Large-Scale Integration*) e ULSI (*Ultra Large-Scale Integration*). E ainda, apresentam grandes vantagens em custo, confiabilidade e desempenho do sistema.

Atualmente, os equipamentos de comunicação sem-fio estão em todos os lugares [ALI94], [COU94], [YAM94] e fazem parte importante na vida do indivíduos. A utilização de equipamentos de comunicação portáteis (alimentados por bateria) tem crescido rapidamente nos útimos anos, como mostram os telefones celulares, os assistentes digitais pessoais (PDAs), os computadores tipo *lap-tops* e *palm-tops*, etc. Todos esses produtos têm auxiliado no estabelecimento da comunicação tipo "a qualquer hora, em qualquer lugar e com qualquer pessoa", e tem direcionado a difusão de serviços multimídias por todas as camadas da sociedade moderna.

Do processo de fabricação ao projeto de sistems eletrônicos em alto nível de abstração através de ferramentas CAD (*Computer Aided-Design*) e técnicas de projeto, a área digital vem avançando rapidamente e com queda contínua de custos. No mercado existem inúmeras ferramentas de CAD digital disponíveis para incontáveis aplicações. As tecnologias digitais são largamente disponíveis em dezenas de *foundries* a baixíssimos custos. Grandes sistemas com maior complexidade são integrados em pequenas pastilhas de silício, com ganhos em velocidade, consumo de potência e confiabilidade. Entretanto, o tempo de projeto, da especificação ao produto final, é crítico e essencial para a sobrevivência das indústrias, já que os seus competidores e consumidores continuam a exijir produtos cada vez mais avançados com mais qualidade.

Ao contrário do projeto digital, o projeto analógico é quase "artesanal". Não podem ser utilizadas as mesmas ferramentas e metodologias. As ferramentas de CAD analógico e tecnologias especiais ainda são proibitivas em termos de custo e existe uma carência na disponibilidade de bons modelos elétricos para os transistores MOSFET. Em quaisquer sistemas de comunicação, existe um sistema analógico embutido atuando como interface de entrada e saída de todo o sistema, interfaceando o mundo analógico do mundo digital. Em um mercado competitivo, o tempo de

projeto é a chave para o sucesso. Porém, o gargalo no projeto de produtos eletrônicos modernos reside na parte analógica. Atualmente, a grande maioria dos projetos de subsistemas digitais contendo em torno de 100 mil portas lógicas, pode ser realizado e verificado, em alguns dias ou semanas. Entretanto, em sistemas analógicos com aproximadamente 100 transistores pode-se consumir meses de projeto até convergir para o desempenho desejado.

Uma outra preocupação importante em equipamentos portáteis à bateria está no consumo de potência, devido à vida útil da bateria, peso e compactação do sistema. O calor gerado dentro do CI é indesejado e deve ser controlado e minimizado, mesmo para sistemas não-portáteis. Para sistemas digitais existe extensa pesquisa, várias técnicas, e metodologias de projeto para a redução de consumo de potência. Existe diferentes níveis de abstração de projeto que são considerados para o controle de potência: nos níveis de especificação de sistema, funcional, arquitetural, lógico, elétrico e de leiaute. Técnicas de redução de consumo controlam a atividade do circuito, a frequência de operação, o chaveamento de capacitores e tensões de alimentação. Ao contrário dos sistemas digitais, onde menor valor da tensão de alimentação (V_{DD}) contribui para a redução do consumo de potência, em sistemas analógicos esta técnica não é benéfica para o desempenho. Baixo V_{DD} em circuitos analógicos não implica em menor consumo de potência. Pelo contrário, a redução de V_{DD} provoca degradações na relação sinal-ruído (*SNR*) e no desempenho global [VIT94a], [ENZ96b].

Hoje, há uma tendência aceita de que toda a parte analógica estará confinada na interface de entrada e saída dos sistemas VLSI. Ou seja, um pequeno sistema analógico entre o mundo totalmente analógico e o núcleo de processamento de sinal totalmente digital em qualquer sistema de comunicação (com ou sem fio). A principal vantagem do processamento de sinal totalmente digital seria o baixo custo e o potencial ilimitado em precisão e em desempenho dinâmico, graças à regeneração sistemática dos bits de estado em todo os passos de processamento.

Como mencionado anteriormente, as principais vantagens do projeto digital são o baixo custo, relativa facilidade de projeto e testabilidade. O projeto digital envolveria os projetistas de computação através das avançadas ferramentas de síntese com a implementação de algoritmos específicos ou programáveis. Portanto, a tarefa dos projetistas analógicos estaria essencialmente concentrada no desenvolvimento de interfaces de bom desempenho. A função destas interfaces é converter o mais rapidamente possível todas as informações ou grandezas analógicas em números (com aumento de demanda em precisão e exposição aos altos níveis de ruído digital no *chip*) e/ou converter todo o resultado de processamento das informações digitais novamente para os módulos analógicos.

A pesquisa desenvolvida no curso de mestrado do autor [CHO94] foi exatamente nesta fronteira analógica-digital, onde foi estabelecido um estudo comparativo e o projeto de moduladores A/D (analógico-para-digital) Sigma-Delta, devido á sua importância prática e pelos desafios anteriormente mencionados, buscando aqueles de melhor desempenho. Neste processo, foram projetadas e validadas diversas células analógicas que compõem o modulador Sigma-Delta, bem como as suas diversas topologias.

Além disso, indústrias eletrônicas podem utilizar-se de matrizes pré-difundidas em sistemas ASICs (Circuitos Integrados de Aplicação Específica) no intuito de reduzir o tempo de projeto (*design turnaround*) e fabricação, da especificação até o produto final. O estilo de projeto semi-customizado apresenta vantagens como a abstração de nível de projeto, automatizando os passos de projeto de leiaute, oferece alta qualidade e desempenho a baixíssimos custos, rápida prototipação e menos tempo para o produto atingir o mercado. O custo, desempenho e tempo de projeto são também importantes em analógicos. Logo, a aplicação das vantagens do semi-customizado em projetos analógicos merecem ser investigados. No entanto, as matrizes pré-difundidas semi-customizadas não são adequadas para aplicações analógicas. Diversas pesquisas nessa área tem sido desenvolvidas, porém nenhuma delas tem preenchido todas as necessidades dos projetistas, da indústria e do mercado.

Neste contexto, é necessária rápida ação das indústrias e universidades e demandado o desenvolvimento de novas metodologias de projeto de CIs. As universidades não são responsáveis somente pela formação de recursos humanos especializados, mas precisam trabalhar em parceira com a indústria para oferecer produtos avançados e técnicas e ferramentas inovativas.

1.2 Objetivos

O principal objetivo deste trabalho é apresentar uma técnica inovativa, a qual encontra aplicação analógica sobre a matriz pré-difundida digital semi-customizada em tecnologias CMOS submicrônicas. Um bloco elementar em particular para o projeto analógico – Associação Trapezoidal de Transistores (TAT – *Trapezoidal Association of Transistors*) de comprimento de canal mínimo – é proposto para explorar os benefícios do bom desempenho analógico utilizando-se somente os transistores unitários, uniformemente dimensionados, sobre a matriz digital Mar-de-Transistores (SOT – *Sea-Of-Transistores*) [AIT96b], [CHO99a], [CHO99b], [CHO2000b]. Este trabalho compara duas estratégias de projeto de leiaute: posicionamento&roteamento de

transistores totalmente customizados versus o leiaute semi-customizado de transistores regularmente posicionados em uma matriz uniforme. Esta última metodologia é a utilizada para o projeto de módulos analógicos utilizando-se da técnica TAT. O enfoque central é o projeto de circuitos e sistemas, o qual pode ser muito vantajoso em ampla gama de aplicações analógicas e em sistemas mistos.

Os problemas envolvidos no projeto de blocos analógicos – espelhos de corrente, comparadores, amplificadores de fonte-comum e amplificares operacionais (OTA – *Operational Transconductance Amplifier*) – sobre a matriz digital SOT são analisados. Demonstra-se a validade da técnica através de exemplos e comparando implementações de circuitos e sistemas, como OTAs e moduladores Sigma-Delta, os quais podem ser encontrados em muitas interfaces analógicas-digitais. A abordagem demonstrada aqui busca atacar com os problemas de baixo desempenho dos circuitos analógicos com os transistores de canal mínimo e em tecnologia digital. Os passos de projeto de leiaute desta técnica é regular, podem ser mais automatizados e mais insensíveis às grandes variações estastísticas presentes em todos os processos de fabricação de *chips*. Adicionalmente, o consumo de potência é um desafio. As dificuldades relacionadas à operação de circuitos analógicos à baixa tensão de alimentação são também analisadas de forma indireta. A adequabilidade e as formas de trabalhar com a matriz SOT a baixas tensões de alimentação para acompanhar as tecnologias sub-micrônicas, também são enfocadas na técnica TAT.

A idéia da técnica TAT pode ser estendida para qualquer projeto ou aplicação que envolva um desempenho analógico aceitável (em fontes de corrente, referências de tensão, comparadores, amplificadores, etc) em ambientes de sinais mistos, para os quais a tecnologia de fabricação digital CMOS é inevitavelmente a alternativa de implementação.

Inicialmente discute-se os diversos problemas que surgem em projetos semi-customizados e consumo de potência em modernos sistemas ASIC. O princípio do transistor TAT é extensamente investigado e comparado com o seu equivalente transistor simples, através de simulações elétricas e medidas experimentais realizadas em diversas amostras de *chips*-de-teste. Os mesmos procedimentos e análises também são realizados nos amplificadores de fonte-comum, comparadores e OTAs, para demonstrar a aplicabilidade e vantagens da utilização dos transistores TAT. Finalmente, um sistema misto implementado em ambas as metodologias, totalmente customizada e matriz semi-customizada SOT, é proposto e investigado para validar a metodologia SOT. Este sistema A/D é parte do modulador Sigma-Delta multi-padrão de 2ª ordem para sistemas de comunicação sem-fio como descrito no capítulo 6.

As conclusões são suportadas pelas simulações e dados experimentais realizados em silício para todos os blocos básicos e sistema já descritos anteriormente. Diversos veículos de teste, incluindo os *chips*-de-teste em tecnologias CMOS 1.0μm e 0.5μm, foram fabricados. Testes experimentais que permitem várias comparações entre as metodologias de projeto de leiaute SOT e totalmente customizada foram extensivamente realizados. Entre vários modelos de MOSFET ([CUN96], [GAL96], [JES95]), a modelagem e a análise do TAT aqui contidas são baseadas no modelo EKV [ENZ89]. Todos os resultados de simulações elétricas foram obtidos do simulador elétrico HSpice e PSpice.

1.3 Organização do Texto (da versão em Inglês)

No capítulo 2 são apresentadas e estabelecidas as perspectivas dos tópicos descritos anteriormente neste trabalho. O estabelecimento do problema, considerando o projeto analógico e misto em matrizes semi-customizadas, é apresentado. Além disso, por que isto deve ser solucionado e as referências e os comentários sobre as pesquisas relevantes de outros autores no mesmo problema ou similar são também apresentados. As contribuições das idéias propostas, soluções e experimentos deste trabalho são mostrados nos capítulos seguintes.

No capítulo 3 a matriz SOT é revista. A técnica TAT é introduzida e, com propósito de melhor entendimento, primeiro o FET (Field Effect Transistor) trapezoidal é brevemente descrito. No capítulo seguinte (capítulo 4) o transistor TAT é extensamente analisado, investigado e experimentalmente comparado com o seu equivalente transistor simples lado a lado no mesmo *chip*, através de simulações elétricas e medidas experimentais, desenvolvidos em estruturas de transistores implementados em *chips*-de-teste. A modelagem DC, AC e ruído do TAT são também mostrados.

O capítulo 5 é dedicado ao projeto de células básicas e circuitos analógicos, como também apresentam-se as simulações elétricas e medidas experimentais utilizando os transistores TAT sobre a matriz SOT comparados com a implementação totalmente customizada dos seus circuitos e células equivalentes.

No capítulo 6 o projeto de um sistema com a técnica anterior é demonstrado. Um modulador analógico-para-digital Sigma-Delta de 2ª ordem sobre a matriz SOT com o objetivo de validar a técnica TAT é implementado e experimentalmente testado utilizando a metodologia da matriz semi-customizada SOT.

2 Projeto de Circuitos Mistos Analógico-Digital Sobre Matriz Pré-Difundida Digital Aplicando a Associação Trapezoidal de Transistores

2.1 Introdução

A tese de doutorado está dividida basicamente em duas partes: proposta, estudo e análise da técnica TAT para aplicações analógicas; e projeto de sub-circuitos básicos e sistema analógicos com a técnica anterior. Na primeira parte (capítulos 3 e 4) é apresentada as formas de contornar os problemas envolvidos na implementação de circuitos analógicos sobre a matriz pré-difundida digital SOT e uma revisão rápida sobre a matriz SOT e suas características. Inclue-se ainda as modelagens teóricas DC, AC e ruído com uma análise comparativa, teórica e experimental entre o TAT e o seu equivalente transistor simples, onde diversas geometrias de transistores (TAT e simples) foram implementadas em *chips*-de-teste e foram exautivamente testadas.

Na segunda parte (capítulos 5 e 6) é apresentado vários projetos utilizando a técnica TAT proposta. Espelhos de corrente, amplificadores de fonte-comum, comparadores e amplificadores OTA são projetados e também implementados em *chips*-de-teste aplicando a idéia do TAT. As versões com TAT são sempre, teoricamente e experimentalmente, comparadas com as suas versões totalmente customizadas. Para validar de forma completa e decisiva o projeto semi-customizado na matriz SOT com a técnica TAT, um sistema analógico foi projetado e implementado em ambas as metodologias de leiaute, semi- e totalmente customizada. Todas as implementações foram geradas utilizando-se as tecnologias CMOS 1.0μm (puramente digital) e 0.5μm. Nas seções sub-sequentes deste resumo estão descritos sucintamente cada capítulo da tese de doutorado.

As chamadas das referências de figuras, tabelas e equações do texto principal da tese estão aqui indicadas entre parênteses e sublinhadas. As referências aos capítulos e seções também estão sublinhadas. As referências biblográficas estão indicadas como no texto principal da tese em inglês, ou seja, referenciadas diretamente do capítulo 8 (*References*).

2.2 Discussão de Problemas e Soluções em Projeto Analógico Semi-customizado (Resumo do Capítulo 2)

Neste capítulo são discutidos os problemas envolvidos no projeto analógico semi-customizado em matrizes pré-difundidas digitais. São comparativamente apresentadas as vantagens de projeto digital e o uso de tecnologias de fabricação digitais em relação ao projeto analógico. É proposta a utilização das ferramentas CADs e tecnologias digitais para o projeto analógico, possibilitando a implementação de sistemas mistos em ambientes digitais e aumentando a velocidade de prototipação de CIs analógicos e mistos.

As facilidades de projeto digital são bem conhecidas: a concepção se desenvolve em alto nível de abstração, utilização de células IPs (*Intellectual Properties*) pré-caracterizadas disponíveis em bibliotecas, utilização de ferramentas CADs avançadas, geração automática de leiautes (particionamento, posicionamento e roteamento), facilidade de migração para tecnologias submicrônicas, baixo custo, entre outras. As vantagens das matrizes pré-difundidas (*gate arrays*) também são bastante difundidas, ou sejam: rápido ciclo de projeto e prototipagem. Se todas as características anteriores fossem aplicáveis a circuitos analógicos, o tempo de projeto seria substancialmente reduzido, vários passos de projeto de leiuates seriam automatizados, pré-fabricados e salvos, as ferramentas CADs digitais poderiam ser aproveitadas, as células analógicas das bibliotecas seriam facilmente migradas para novas tecnologias, o que possibilitaria a rápida prototipagem de CIs analógicos e mistos.

A alternativa de projeto semi-customizado é barata e permite fabricação “rápida” de CIs, pois todos os transistores são pré-definidos, caracterizados e dispostos regularmente na matriz linear. Apenas o processo de metalização é necessário para finalizar a fabricação do CI. Existe outra vantagem na implementação de analógicos em matrizes pré-difundidas digitais (*Sea-of-Gates*), ou seja, há uma relativa redução no descasamento entre os dispositivos, onde um arranjo regular e linear de transistores unitários (dimensões fixas) possibilita, naturalmente, o emprego da técnica de leiaute para casamento de pares de transistores largamente utilizada em leiautes analógicos. Os pares de transistores de grandes larguras são particionados em diversas partes (*fingers*) e intercalados (*interdigitized*), melhorando o casamento, sendo esta a chamada técnica de interdigitação [ALE97], [ISM94], [TSI96]. Combina a técnica de geometria de centróide comum, minimiza as capacitâncias e resistências parasitas, e reduz os efeitos do diodo reverso lateral

[GRO67] devido à redução da relação perímetro/área das difusões de dreno-fonte e o compartilhamento destes terminais.

Sendo possível a implementação de sistemas analógicos nas matrizes semi-customizadas, todas as vantagens descritas anteriormente serão muito úteis em aplicações analógico-digitais, pois combinam sistemas analógicos e digitais lado-a-lado na mesma pastilha de silício, o que permite integração de sistemas mistos em um único *chip*.

Evidentemente, as condições mencionadas são ideais. Algumas características de implementação não são possíveis. Por exemplo, é necessário o dimensionamento dos transistores pelo projetista, e a re-utilização de células IPs e a migração de tecnologia são tarefas complexas. Portanto, existe necessidade de melhoramentos e desenvolvimento de novas técnicas para serem empregadas nas metodologias e tecnologias existentes. Como a matriz digital SOT é composta por transistores com comprimento de canal mínimo, esta matriz não pode ser utilizada diretamente em aplicações analógicas, a menos que uma técnica específica seja desenvolvida. O princípio TAT (Associação Trapezoidal de Transistores) é empregado neste trabalho como uma alternativa, entre outras, para a implementação analógica em ambientes digitais e encurtar o tempo de fabricação de sistemas analógicos.

A técnica TAT proposta é uma das idéias novas que pode ser extendida para quaisquer transistores digitais (comprimento de canal mínimo), matrizes pré-difundidas digitais, e ainda em metodologias totalmente customizadas. Esta técnica foi proposta e desenvolvida em diversos trabalhos [GAL94], [AIT96b], [CHO99b], [CH2000a]. A técnica originalmente se baseia em dois trabalhos de pesquisa. Primeiro, o Riccò [RIC84] demonstrou que um FET de geometria de canal trapezoidal (área do dreno maior do que área da fonte – formato assimétrico) tem uma substancial redução na condutância de saída, sugerindo que um FET de canal não-retangular pode ser empregado vantajosamente em aplicações analógicas e para amenizar os efeitos de canal curto.

Segundo, a técnica de associação trapezoidal de transistores foi originalmente introduzida por [GAL94], o qual demonstrou que essa associação com transistores FETs é eletricamente equivalente ao transistor FET simples. Desta forma, as variedades de dimensões como comprimento L, largura W e a relação de aspecto W/L do canal necessários em quaisquer sistemas analógicos são emulados (imitados) através da geração do transistor TAT, uma associação série-paralela de transistores mínimos (em nosso estudo e resultados utilizando no máximo 2 transistores em série). Posteriormente, entre outras vantagens, demonstra-se que a associação em estrutura trapezoidal é vantajosa, como em FET trapezoidal.

A técnica TAT foi extensivamente descrita e sistematicamente analizada para demonstrar, teoricamente e experimentalmente, que esta pode ser uma boa alternativa para os projetistas analógicos em ASICs semi-customizados. Diversas estruturas de transistores foram incluídas em ambas as metodologias de leiaute (matrizes semi-customizadas SOT e totalmente customizados) para permitir melhor análise e investigação comparativa.

Os primeiros resultados apresentados neste trabalho são para a tecnologia CMOS digital 1.0µm com diversas simulações elétricas e medidas experimentais entre o TAT e o transistor convencional em dispositivos e amplificador simples *folded-cascode* tipo OTA. Na segunda parte deste trabalho encontram-se o projeto e implementação do Modulador Sigma-Delta de 2ª ordem nas duas metodologias de leiaute semi- e totalmente customizado, neste caso utilizando-se de tecnologia CMOS 0.5µm. Várias células analógicas também são apresentadas, como espelhos de corrente e amplificadores de estágio simples (fonte-comum), e os blocos que compõem o Sigma-Delta anterior, ou sejam: comparador diferencial *track-and-latch*, amplificadores diferenciais *folded-cascode* tipo OTA, integradores diferenciais capacitor-chaveado e chaves CMOS. Adicionalmente, foram incluídos uma pequena estrutura de transistores com TATs e seus equivalentes convencionais em tecnologia CMOS 0.5µm. Todas as células e blocos analógicos anteriores foram implementados nas duas metodologias de leiaute: sobre a matriz pré-difundida SOT em um circuito e totalmente customizado (*full-custom*) em outro circuito.

2.3 Associação Trapezoidal de Transistores (Resumo do Capítulo 3)

Neste capítulo apresenta-se a técnica TAT para projeto analógico em tecnologia CMOS VLSI, com a sua descrição e análise e, de forma genérica, a matriz pré-difundida digital SOT (Mar-de-Transistores).

A arquitetura da matriz SOT utilizada neste trabalho tem geometria retangular (estilo *Manhattan*) e está mostrada na Fig. 1 (Fig. 3.1) [AIT96a], [CHO98a], [CHO98b]. A matriz está associada, primeiro, à organização geral da matriz, ou sejam: construção da matriz propriamente dita, com os transistores unitários; e com a arquitetura das células unitárias, isto é, com o dimensionamento dos transistores unitários.

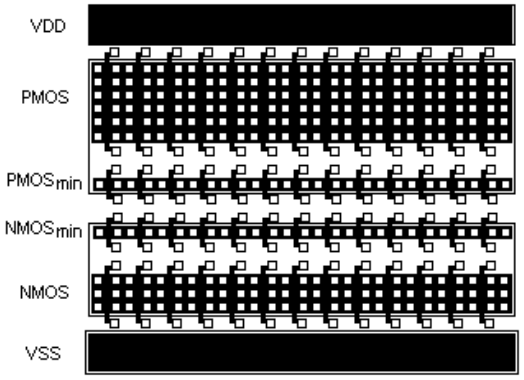


FIGURA 1 - Matriz SOT com as transistores unitários.

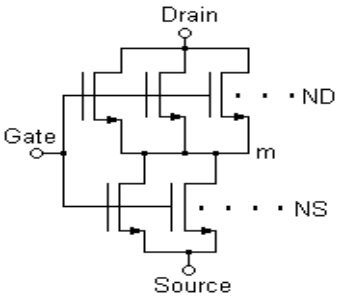


FIGURA 2 - TAT: associação série-paralela de transistores que geram o MS e MD.

A matriz SOT foi projetada em duas tecnologias CMOS diferentes: a digital 1.0µm (poly e duplo metal) e a 0.5µm (duplo poly e triplo metal). A primeira tecnologia pela *foundry* ES2, devido a disponibilidade das regras de projeto e acesso ao programa multi-usuário de prototipação no próprio laboratório da Universidade Federal do RGS. A segunda, pelo serviço americano MOSIS para a implementação do sistema analógico descrito no capítulo 6. No caso da MOSIS, foi utilizada a tecnologia de fabricação da empresa AMI, sendo que o uso do segundo nível de polisilício

permitiu utilizar capacitores poly1-poly2, enquanto a matriz de transistores reproduziu o que é utilizado em uma tecnologia estritamente digital.

A arquitetuta da matriz e as dimensões das células unitárias seguem as restrições mínimas impostas pelas regras de projeto, migração de tecnologia, especificações em projetos digitais e adequação e conveniência da forma e arquitetura da matriz para posicionamento e roteamento das células e transistores unitários. Na matriz da Fig. 1 existe quatro transistores unitários à disposição dos projetistas: dois NMOS; e dois PMOS. Em cada tipo existem duas versões diferentes: um de dimensões mínimas conforme as regras de projeto de uma dada tecnologia; e um com comprimento de canal mínimo ($L_{mín}$), mas com largura do canal (W) adequada às aplicações digitais, ou seja, para atender às especificações de *fan-out* (capacidade de carga) das portas lógicas. A largura do canal do transistor unitário tipo NMOS, foi fixada em dez vezes acima do comprimento mínimo, $W_N = 10L_{mín}$ e para o transistor tipo PMOS em $W_P = 2W_N$. Na Tabela 3.1 do capítulo 3 estão listadas as dimensões dos transistores unitários disponíveis na matriz para as tecnologias 1.0µm e 0.5µm com as quais foram obtidos os resultados experimentais deste trabalho.

Como mencionado anteriormente, o transistor TAT basea-se no trabalho demonstrado por Riccó [RIC84]. Com uma geometria assimétrica do canal (dreno maior que fonte) há uma acentuada redução na condutância de saída em saturação. Posteriormente, no trabalho [GAL94] demonstra-se que a associação trapezoidal série-paralela de transistores FETs, discretos, como mostrado na Fig. 2 (Fig. 3.3a), é equivalente a um FET trapezoidal, desde que atendam às seguintes condições: relação de aspecto W/L similar; largura do canal W no terminal dreno também similar; e os mesmos efeitos de canal-curto (MS e MD em condução). MD e MS (Fig. 2) são associações em paralelo de transistores unitários.

Os TATs são obtidos a partir dos seus equivalentes transistores convencionais. Para cada transistor convencional obtém-se várias possíveis alternativas de associações TAT. Este processo é realizado com um gerador automático de TATs, chamado de TATGen [AIT2000]. Dentre as alternativas possíveis, o projetista interage iterativamente escolhendo aquela que melhor atende às especificações de projeto, observando o seguinte: todas as alternativas são aproximações do equivalente convencional (ou simples).

O TATGen gera os TATs da seguinte forma: a relação de aspecto equivalente da associação é calculada pela seguinte aproximação (Eq. 3.3.1):

$$\left(\frac{W}{L}\right)_{Eq} = \frac{\left(\frac{W}{L}\right)_D \left(\frac{W}{L}\right)_S}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_S} \tag{1}$$

onde $(W/L)_D$ e $(W/L)_S$ são, respectivamente, as relações de aspecto dos transistores superior MD e inferior MS. Pode-se rescrever (1) como (Eq. 3.3.4):

$$\left(\frac{W}{L}\right)_{Eq} = \frac{m}{m+1}\left(\frac{W}{L}\right)_S \tag{2}$$

onde:

$$m = \frac{\left(\frac{W}{L}\right)_D}{\left(\frac{W}{L}\right)_S}, m \geq 1 \tag{3}$$

é a relação entre as relações de aspecto de MD e MS, ou das larguras Ws dos mesmos quando $L_D = L_S$ (Eq. 3.3.2).

Manipulando-se algebricamente a expressão (1), obtém-se a seguinte expressão:

$$\left(\frac{W}{L}\right)_D = \frac{\left(\frac{W}{L}\right)_{Eq} \left(\frac{W}{L}\right)_S}{\left(\frac{W}{L}\right)_S - \left(\frac{W}{L}\right)_{Eq}} \tag{4}$$

que permite calcular as dimensões necessárias de MD em função da relação de aspecto do projeto e do MS. Com este valor, deve-se dividir pela relação de aspecto do transistor unitário, com o valor inteiro mais próximo para se obter o número de transistores unitários em paralelo requeridos em MD. Para manter a geometria trapezoidal e obter menor condutância de saída, a associação de transistores em MD deve ser maior do que em MS, ou seja, $m \geq 1$.

2.4 Análise do Transistor TAT (Resumo do Capítulo 4)

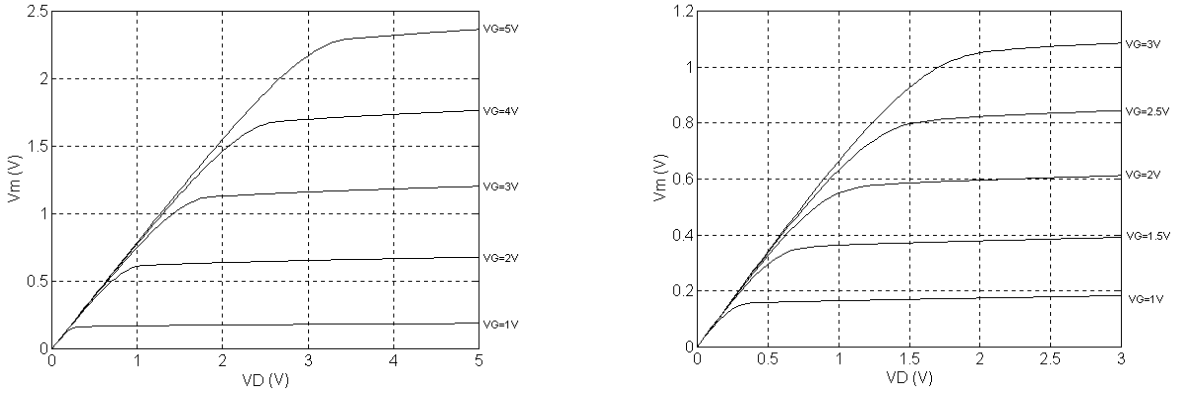
Neste capítulo são descritos os modelos DC, AC e de ruído do transistor TAT. Nestas análises diversas geometrias de TATs e seus equivalentes transistores convencionais foram comparativamente avaliados experimentalmente e por simulações elétricas. Como os TATs são uma uma associação de transistores de comprimento de canal mínimo, os efeitos de canal curto também são analisados. Os *chips*-de-teste que implementam as estruturas de transistores contendo os TATs e seus convencionais equivalentes, são em tecnologia CMOS digital 1.0µm. No capítulo 6 estão incluídos os resultados experimentais da estrutura de teste anterior, agora em tecnologia CMOS 0.5µm.

As correntes de dreno dos transistores em série MD e MS são exatamente iguais à corrente do TAT ($I_{D_{TAT}} = I_{D_{MD}} = I_{D_{MS}}$) dada por [ENZ89], [ENZ96b] (Eq. 4.1.1):

$$I_{D_{TAT}} = I_F(V_P, V_S) - I_R(V_P, V_D) \qquad 1$$

onde V_P, V_D and V_S são a tensão de *pinch-off*, de dreno e fonte, respectivamente, I_F e I_R são as correntes direta (*forward*) e reversa (*reverse*), respectivamente, do TAT.

No TAT, ambos os transistores MD e MS operam em inversão fraca quando a tensão de porta estiver abaixo da tensão de *threshold* V_T equivalente, enquanto que em tensões de porta acima deste valor, ambos os transistores estarão em inversão forte. Logo, aumentando-se o potencial de dreno do TAT V_D ($>V_P$), o transistor MD é saturado (*pinched-off*), porém o transistor MS permanece em condução (região linear). Sob estas condições, MD funciona como fonte de corrente e a sua corrente de dreno mantém-se constante (sem os efeitos de modulação do canal), mesmo aumentando V_D bem acima de V_P. E ainda, a contribuição do transistor MS com o aumento de V_D é invariável, pois o potencial de dreno de MS é fixado pela tensão de saturação do transistor MD. O gráfico $V_m x V_D$ do TAT na Fig. 3 (Fig. 4.2) demonstra este efeito, onde V_m (definido nas Eqs 4.19, 4.1.10 e 4.1.11) é o potencial do nodo intermediário do TAT, entre MD e MS, ou seja, entre os terminais do dreno de MS e fonte de MD.



(a) (b)

FIGURA 3 - Simulação elétrica da curva V_m x V_D do TAT: (a) TAT em tecnologia CMOS 1.0µm. (b) TAT em tecnologia CMOS 0.5µm.

A corrente de dreno do TAT em inversão fraca, válida tanto na região linear como na região saturada, é dada por [ENZ89], [ENZ96b] (Eq. 4.1.5):

$$I_{D_{TAT}} = I_{D_X} = I_{F_X} - I_{R_X} = I_S \cdot e^{\frac{V_P}{U_T}} \left(e^{-\frac{V_{S_X}}{U_T}} - e^{-\frac{V_{D_X}}{U_T}} \right) \qquad 2$$

onde X pode ser MD ou MS, pois $I_{D_{TAT}} = I_{D_{MD}} = I_{D_{MS}}$. Em inversão forte e em saturação são dadas por (Eq. 4.1.6a):

$$I_{D_{TAT}} = I_{D_X} = I_{F_X} - I_{R_X} =$$

$$= \frac{n \cdot b_X}{2} \cdot \left[\left(V_P - V_{S_X}\right)^2 - \left(V_P - V_{D_X}\right)^2 \right] =$$

$$= I_S \cdot \left[\left(\frac{V_P - V_{S_X}}{2 \cdot U_T} \right)^2 - \left(\frac{V_P - V_{D_X}}{2 \cdot U_T} \right)^2 \right] \qquad 3$$

e em condução (inversão forte) (Eq. 4.1.6b):

$$I_{D_X} = n \cdot b_X \left(V_P - \frac{V_{S_X} + V_{D_X}}{2} \right) \left(V_{D_X} - V_{S_X} \right) \qquad 4$$

Desta análise resulta uma conclusão importante. O TAT pode ser utilizado em diversas aplicações de baixa tensão, pois funciona como um circuito auto-cascode (*self-cascode*), isto é, como um estágio cascode intrínseco de característica pobre. Geralmente, necessita-se uma segunda tensão de polarização no terminal porta do transistor MD para operação de um estágio cascode

tradicional. E ainda, não são necessários altos valores de tensão de saturação, já que o transistor MS nunca atinge a saturação e o potencial de dreno no nodo intermediário V_m é baixo (menor do que V_P, pois o TAT é trapezoidal – $ND >> NS$).

Como a relação $(W/L)_{MD}/(W/L)_{MS}$ é feita bem maior do que 1 (associação trapezoidal), a condutância de saída dada pela Eq. 4.3.1 tende para um estágio cascode tradicional [CHO99a], e se reduz para (Eq. 4.3.3):

$$g_o \cong g_{ds_{MD}} \cdot \frac{g_{ds_{MS}}}{g_{mS_{MD}}} \Rightarrow r_o \cong r_{ds_{MS}} \cdot \left(r_{ds_{MD}} \cdot g_{mS_{MD}}\right) \qquad 5$$

E a transcondutância equivalente do TAT pode ser aproximado por (Eq. 4.3.5):

$$g_{m_{TAT}} \cong g_{mG_{MS}} \qquad 6$$

Logo, o transistor MS determina o valor assintótico da transcondutância do TAT. Para melhorar o desempenho global do TAT é necessário aumentar a transcondutância do transistor MS (aumentando NS), diminuir a condutância de saída (diminuindo ND) e/ou aumentar a transcondutância do transistor MD.

Existem propriedades não-ideais bem conhecidas relacionadas com as áreas de difusão em qualquer transistor MOSFET. Primeiro, o efeito da difusão lateral devido às áreas de difusão se tornarem maiores do que as definidas pelas máscaras de leiaute e avançarem sob a área da porta (*gate*). Este efeito causa a diminuição do comprimento efetivo do canal, definido pelo projeto do canal. Segundo, para quaisquer implantes de difusão ficam associadas resistências parasitas série que resultam em uma aparente redução da mobilidade eletricamente efetiva. E finalmente, um outro efeito associado aos implantes de difusão são as junções *pn*, as quais são reversamente polarizadas sob condições normais de operação do TAT (MD em saturação e MS em condução), que resultam em regiões depletadas e capacitâncias de junção.

O ruído equivalente do TAT referido à entrada $V^2_{n_{TAT}}\big|_{in}$ é aproximado para (Eq. 4.5.9):

$$V^2_{n_{TAT}}\big|_{in} = \left\{\frac{ND \cdot \left(g_{mG_{MD}}\big|_u\right)^2}{\left[NS \cdot \left(g_{mG_{MS}}\big|_u\right)\right]^2} + \frac{1}{NS}\right\} \cdot V^2_{n_{fk}}\big|_u + \left\{\frac{ND}{\left[NS \cdot \left(g_{mG_{MS}}\big|_u\right)\right]^2}\right\} \cdot \left(I^2_{n_{th}}\big|_u\right)_{MD} + \\ + \left\{\frac{NS}{\left[NS \cdot \left(g_{mG_{MS}}\big|_u\right)\right]^2}\right\} \cdot \left(I^2_{n_{th}}\big|_u\right)_{MS} \qquad 7$$

onde o fator $NS \cdot \left(g_{mG_{MS}} \big|_u \right)$ é a transcondutância do TAT $g_{m_{TAT}}$ (eq. 6), $V_{n_{fk}}^2 \big|_u$ e $I_{n_{th}}^2 \big|_u$ são os ruídos *flicker* e térmico, respectivamente, de um transistor unitário do TAT. Importante notar que a densidade de corrente em MD é diferente do que em MS, isto é, a corrente em um transistor unitário do transistor MD é menor do que em um transistor unitário do transistor MS (se for associação trapezoidal). Este é o motivo pelo qual os termos do ruído térmico na eq. 7 estão separados.

Enquanto as densidades dos ruídos térmicos (correntes) dos transistores MD e MS forem, respectivamente, ND e NS vezes maiores, as densidades dos ruídos térmicos (tensões equivalentes) referidas à entrada são, respectivamente, $ND \cdot \left(g_{mG_{MD}}^2 \big|_u \right)$ and $NS \cdot \left(g_{mG_{MS}}^2 \big|_u \right)$ vezes menores. A expressão 7 demonstra que as contribuições dos ruídos térmico e *flicker* são menores do que nos transistores unitários. Aumentando a transcondutância do TAT, o ruído total é reduzido, o que é efetivamente realizado aumnetando-se NS. Outro importante ponto a destacar é que o transistor MD é a maior fonte de ruído no TAT. Logo, para melhorar (diminuir o ruído) o desempenho em ruído é necessário transcondutância menor do MD e maior para MS. Porém, implica em menor ND e maior NS, respectivamente, contrariando a regra de construção do TAT. Nos capítulos seguintes é demontrado que a área ativa (*W.L*) no transistor TAT é menor do que no seu equivalente simples, do que resulta maior ruído *flicker* em baixas frequências nos TATs, enquanto que o ruído térmico é comparável ao equivalente convencional.

Com o objetivo de investigar e validar a técnica TAT foram implementados e fabricados vários transistores TATs e seus equivalentes simples em um mesmo *chip*-de-teste. As curvas experimentais ($I_D x V_D$, $g_{ds} x V_D$, $I_D x V_G$, $g_m / I_D x V_S$) estão mostradas comparativamente na Fig. 4 (Fig. A-3) para TAT-3 e Single-3.

As características experimentais do TAT mostram que têm maior corrente de dreno para potenciais de porta abaixo de 3V do que o seu equivalente *full-custom* – Fig. 4a (Fig. A-3a). A condutância de saída no TAT, mostrada na Fig. 4b (Fig. A-1b), é bastante próxima do seu equivalente simples devido ao efeito auto-cascode. Na característica linear $I_D x V_G$, Fig. 4c (Fig. A-1c), pode-se observar o efeito das resistências em série maiores nos TATs, com as medidas realizadas na região de condução (triodo, com $V_D = 100mV$). A redução gradual da corrente de dreno com o aumento do potencial de porta mostra o efeito da associação série nas características na região de condução (triodo).

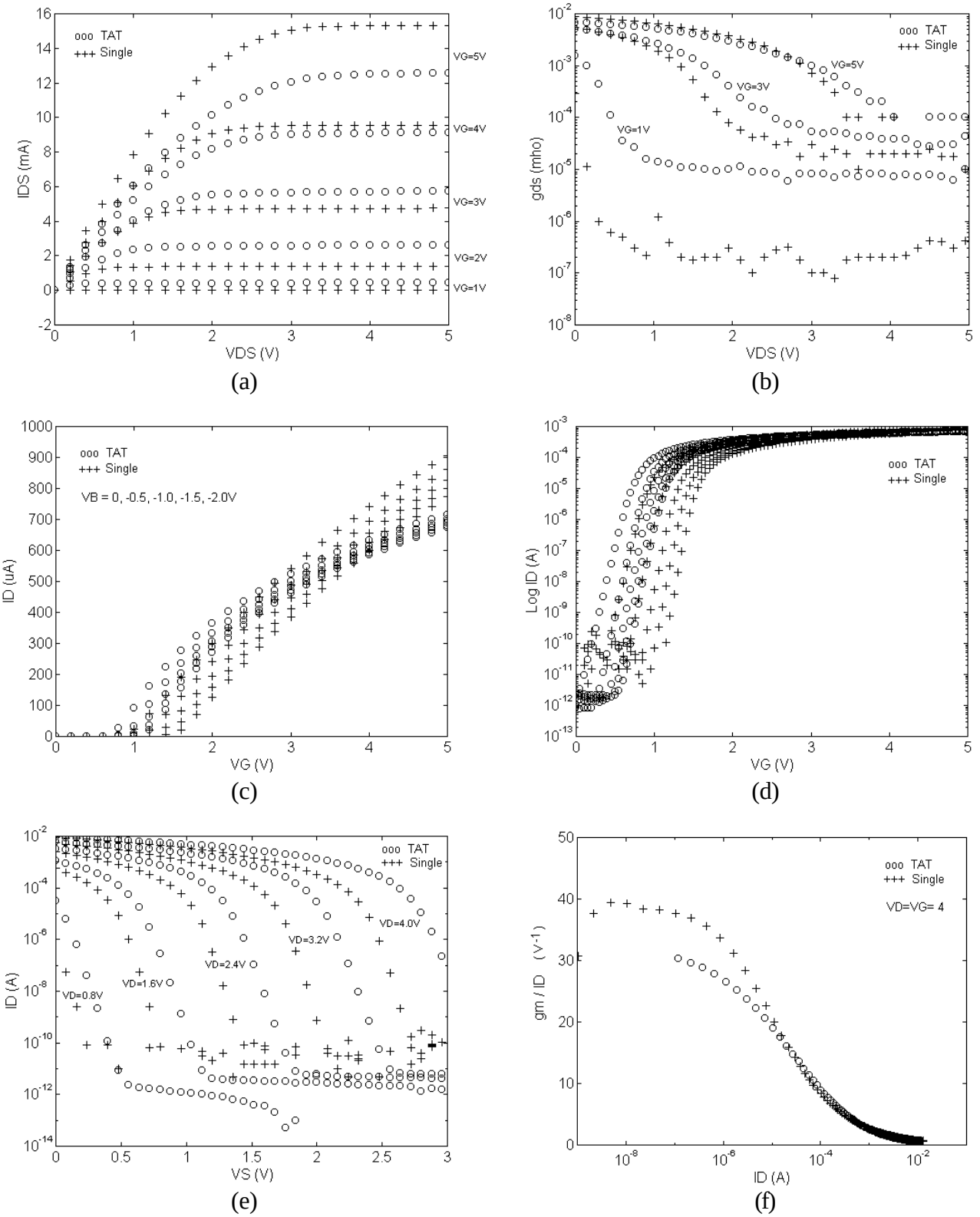


FIGURA 4 - Curvas comparativas experimentais entre TAT-3 (ND=16, NS=4) e Single-3 (W/L=170/5), transistor NMOS em tecnologia 1.0µm. (a) Curva I_DxV_D ($V_B=0V$). (b) Condutância de saída a $V_G=1, 3, 5V$. (c) Curva I_DxV_G com $V_D=100mV$ e o potencial do substrato V_B variando de $0V$ a $-2V$ (passo $0.5V$). (d) $log(I_D)xV_G$. (e) Curva I_DxV_S com $V_D=V_G=0.8, 1.6,\ldots, 4V$ (modo diodo de polarização). (f) $(g_m/I_D)xI_D$ com $V_D=V_G=4V$.

A Fig. 4b (Fig. A-1b) compara a condutância de saída em inversão forte para três níveis de potencial de porta, 1V, 3V e 5V (com comprimento equivalente a L=5µm para os transistores TAT e equivalentes simples). Em inversão forte e em modo de saturação, o TAT com L mínimo apresenta a mesma condutância de saída de um transistor com comprimento de canal longo (L=5µm). Em inversão fraca, os efeitos de canal curto (redução de V_T) e DIBL (*Drain Induced Barrier Lowering* [TSI88]) se combinam para gerar maior condutância de saída no TAT, tanto em condução com em saturação.

O gráfico experimental da Fig. 4d (Fig. A-1d) mostra um grande deslocamento do threshold associado ao TAT em relação ao seu equivalente simples com comprimento do canal L=5µm, devido ao efeito de canal curto nos transistores unitários (L mínimos) do TAT.

A curva característiva em saturação $I_D x V_S$ (modo diodo), mostrada na Fig. 4e (Fig. A-3e), mostra o deslocamento da corrente de dreno na região de *subthreshold* (efeito do canal curto), e mostra que a corrente reversa do diodo (mode desligado) no TAT é menor do que no convencional, causado pelo efeito do diodo reverso lateral e planar (diodo controlado pela porta [GRO67]) nos transistores MOSFET, os quais são o resultado das junções *np* e *pn* entre os implantes das difusões *n+* e *p+* e o substrato. Devido ao arranjo linear dos transistores unitários, compartilhamento do dreno e fonte, e ter menor área e perímetro das difusões, o efeito anterior é minimizado nos transistores TAT.

2.5 Implementação de Subcircuitos Analógicos Básicos Aplicando os Transistores TATs (Resumo do Capítulo 5)

Diversos blocos básicos analógicos são projetados e fabricados em ambas as metodologias de leiaute: semi-customizado SOT e totalmente customizado. Um bom conhecimento destes blocos é crítico para compreender muitos pontos deste trabalho e para projeto de CIs em qualquer matriz semi-customizada. As células analógicas implementadas foram: espelho de corrente, amplificador de fonte comum, comparador e amplificador *fold-cascode* tipo OTA. O chip-de-teste contendo estas células analógicas foi fabricado em tecnologia CMOS 0.5µm, duplo poly e três níveis de metal. Para validação da técnica TAT nas células analógicas foram avaliadas através de simulações elétricas e medidas experimentais.

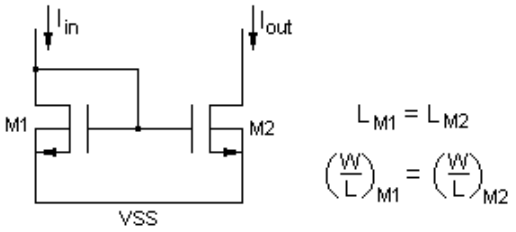


FIGURA 5 - Espelho de corrente com transistors tipo N .

TABELA 1 - Transistores TAT e simples do espelho de corrente (‘ indica versão TAT).

					Tamanho do Transistor	
Tec.	**Transistor**	**W(µm)**	**L(µm)**	**W/L**	**ND**	**NS**
0.5µm	M1-M2	106	1.9	55.86	-	-
	M1’-M2’	106	1.9	55.86	20x(5.4µm/0.6µm)	9x(5.4µm/0.6µm)

Uma boa forma de verificação experimental da condutância de saída do TAT é através da célula espelho de corrente, mostrada na Fig. 5 (Fig. 5.1). O casamento entre os dois transistores pode ser verificado através do desvio entre as correntes de entrada e saída. O desvio na corrente de saída do espelho de corrente pode ser expressa em termos da variação da tensão de saturação do transistor de saída e sua impedância de saída, ou seja por (Eq. 5.1.3):

$$\Delta I_{out} = \frac{\Delta V_{D_{M2}}}{r_{ds_{M2}}} \qquad 8$$

Esta célula foi implementada nas duas metodologias de leiaute (SOT e totalmente customizado) em tecnologias CMOS 1.0µm e 0.5µm. Os transistores dimensionados estão listados na Tabela 1 (Table 5.1) para a tecnologia 0.5µm. A versão com TAT apresentou melhor casamento de corrente, demonstrando a redução prevista da condutância de saída do TAT. Os resultados experimentais estão na seção seguinte (capítulo 6) em tecnologia CMOS 0.5µm.

Outra forma de examinar o desempenho do TAT é através do amplificador simples de fonte comum. Este amplificador básico foi projetado com um transistor tipo PMOS como carga ativa para polarização (fonte de corrente tipo PMOS), como mostrado na Fig. 6 (Fig. 5.2a).

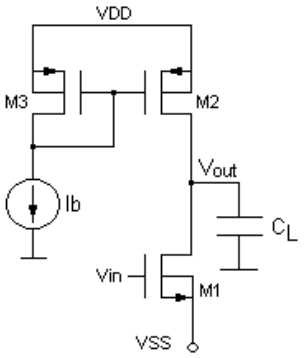


FIGURA 6 - Amplificador de fonte comum com transistor PMOS como carga ativa.

O pólo dominante da versão TAT do amplificador pode ser calculado através do método da análise de constante de tempo zero [JOH97] e é dado por (**Eq. 5.2.7**):

$$w_P \cong \frac{1}{R_{in}\cdot\left[C_{gs_{MS}}+C_{gd_{MD}}+g_{mG_{MS}}\cdot R_2\cdot\left(C_{gd_{MS}}+C_{gs_{MD}}\right)\right]+\left(C_{gd_{MD}}+C_{d2}\right)\cdot R_1+C_{S2}\cdot R_2} \qquad 9$$

onde as capacitâncias C_{d2} e C_{S2} e as resistências R_1 e R_2 são dadas por (Eqs. 5.2.6a, b e Eqs. 5.2.8a, b):

$$C_{d2} = C_{db_{MD}} + C_L + C_{mir} \qquad 10$$

$$C_{S2} = C_{db_{MS}} + C_{sb_{MD}} \qquad 11$$

$$R_1 = r_{ds_{MS}} \cdot r_{ds_{MD}} \cdot g_{mS_{MD}} \qquad 12$$

$$R_2 = \frac{1}{g_{ds_{MS}} + \dfrac{g_{mS_{MD}} \cdot r_{ds_{MD}} + 1}{R_L}} \qquad 13$$

onde C_{mir} é a capacitância parasita na saída do espelho de corrente (terminal dreno da versão TAT de M2 na Fig. 6 - Fig. 5.2a).

TABELA 2 - Dimensionamento dos transistores do Amplif-2 (‘ indica a versão TAT).

Amplif-2: AMP_S2 (simples) e AMP_T2 (TAT) – tecnologia CMOS 0.5mm							
Xtor	**W (mm)**	**L (mm)**	**W/L**	**ND**	**NS**	**Rel. de Area Ativa**	**Rel. de Area**
M1	106	1.9	55.8	-	-	0.46	1.431
M1’	106	1.9	55.8	20x (5.4µm/0.6µm)	9x (5.4µm/0.6µm)		
M2-M3	191	1.7	112.3	-	-	0.54	1.515
M2’-M3’	191	1.7	112.3	16x (11.7µm/0.6µm)	9x (11.7µm/0.6µm)		

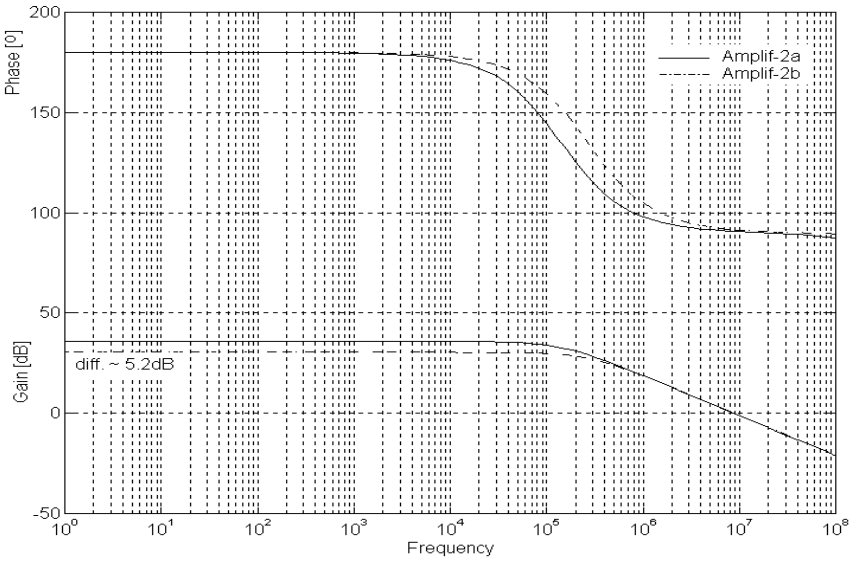


FIGURA 7 - Amplificador fonte-comum Amplif-2: ganho e margem de fase. Simulação elétrica em tecnologia CMOS. AMP_T2 (tracejado) e AMP_S2 (sólido). $(W/L)_{eq}$=106/1.9.

O ganho DC é encontrado com a condutância de saída e a transcondutância do TAT das equações 5 e 6 (Eqs. 4.3.3 e 4.3.5), respectivamente. O resultado é simplesmente dado por ($R_L = \mu$) (Eq. 5.2.9):

$$A_{Vo_{TAT}} \cong -g_{mG_{MS}} \cdot g_{mG_{MD}} \cdot r_{ds_{MS}} \cdot r_{ds_{MD}} \qquad 14$$

Na Tabela 2 (Table 5.3) estão listados os transistores projetados do Amplif-2 em tecnologia CMOS 0.5µm. O AMP_S2 é a versão totalmente customizada do semi-customizado AMP_T2. Observa-se, na tabela, que aos três transistores da versão totalmente customizada (AMP_S2) correspondem um total de 54 transistores unitários da versão TAT (AMP_T2).

Os resultados de simulação elétrica estão mostrados na Fig. 7 (Fig. 5.4) [CHO2000b]. Como esperado, a versão TAT funciona aproximadamente como um amplificador cascode ou um auto-cascode. O ganho e a fase são quase comparáveis ao totalmente customizado. O resultado demonstra que a condutância de saída do TAT é similar ao cascode tradicional (Eq. 5). Os resultados experimentais são apresentados na seção seguinte (capítulo 6).

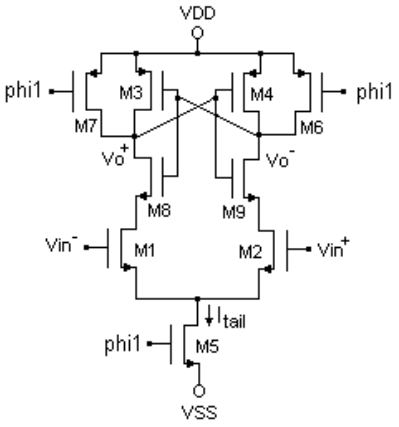


FIGURA 8 - Comparador Track-and-Latch.

No comparador da Fig. 8 (Fig. 5.6), a constante de tempo pode ser estimada aproximadamente pela frequência máxima do relógio. Logo, para que o comparador reconheça a diferença de tensão para que segure o valor lógico da comparação, o tempo de *latch* é dado por (Eq. 5.3.2):

$$T_{latch} = \frac{C_L}{G_m} \cdot \ln\left(\frac{\Delta V_{logic}}{\Delta V_0}\right) = KA \cdot \frac{L^2}{m_n \cdot V_P} \cdot \ln\left(\frac{\Delta V_{logic}}{\Delta V_0}\right) \qquad 15$$

onde, ΔV_{logic} é a diferença de tensão lógica desejada e ΔV_0 é a diferença de tensão de entrada necessária para comparação no começo da fase de *latch*.

Os transistores projetados do TAT e simples do comparador estão listados na Tabela 3 (Table 5.5). O comparador totalmente customizado possui 28 transistores enquanto o seu equivalente com TATs tem 41 transistores unitários. A versão sobre a matriz SOT emprega os TATs somente no par diferencial de entrada (M1 and M2), pois os demais transistores são digitais. O consumo de potência neste comparador é baixo pois a corrente flui no circuito somente no semi-período ativo antes do *latch*.

TABELA 3 - Dimensões dos transistores simples e TAT (‘ indica versão TAT).

Comparador Track-and-Latch (tecnologia CMOS 0.5µm)					
Transistor	**W(µm)**	**L(µm)**	**W/L**	**ND**	**NS**
M1-M2	72	1.2	60	-	-
M1’-M2’	108	-	60	20x(5.4µm/0.6µm)	10x(5.4µm/0.6µm)
M8-M9	30	0.6	50	-	-
M8’-M9’	32.4	-	54	6x(5.4µm/0.6µm)	-
M5	10	15	0.67	-	-
M5’	1.2	-	2	1x(1.2µm/0.6µm)	-
M3-M4	20	0.6	33.33	-	-
M3’-M4’	23.4	-		2x(11.7µm/0.6µm)	-
M6-M7	2.5	0.6	4.2	-	-
M6’-M7’	2.4	-	4	2x(1.2µm/0.6µm)	-

Este comparador foi fabricado em tecnologia CMOS 0.5µm da *foundry* MOSIS, nas duas metodologias de leiaute semi-customizado com os TATs e totalmente customizado. Os resultados experimentais também são apresentados na seção seguinte (capítulo 6).

O amplificador *folded-cascode* tipo OTA, mostrado na Fig. 9 (Fig. 5.10), é de par de entrada diferencial e saída simples. Este sub-circuito foi implementado em tecnologia CMOS digital 1.0µm, na metodologia totalmente customizado [CHO97] e semi-customizado SOT [CHO99c], [CHO2000b].

No primeiro momento, utilizando os transistores TAT, conclui-se que a versão com TAT apresenta maior ganho DC do que a versão totalmente customizado. No entanto, isto não é sempre verdadeiro, pois a transcondutância do TAT é menor do que o seu equivalente simples. Logo, existe um efeito de compensação entre o comportamento dos dois termos – a transcondutância e impedância de saída – os quais determinam o ganho DC, já que a condutância de saída no TAT é quase a mesma ou maior em relação ao seu equivalente simples (capítulo 4 – seção 4.2). Consequentemente, é natural que o *slew-rate* (*SR*) do TAT seja menor, pois o pólo dominante é maior no totalmente customizado (sob as mesmas condições DC para ambos).

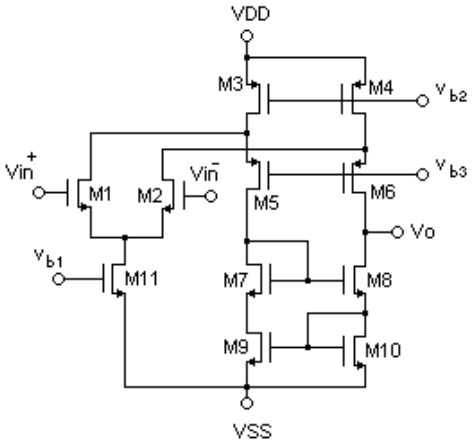


FIGURA 9 - Amplificador *folded-cascode* tipo OTA de saída simples.

TABELA 4 - Projeto dos transistores TAT e simples do OTA totalmente customizado e semi-customizado SOT (‘ indica versão TAT).

OTA *folded-cascode* OTA – tecnologia CMOS 1.0mm							
Xtor	**W (µm)**	**L (µm)**	**W/L**	**ND**	**NS**	**Rel. de Área Ativa**	**Rel. de Área**
M1-M2	170	5	34	-	-	0.247	1.942
M1’-M2’	168	-	33.6	16x (10.5µm/1µm)	4x (10.5µm/1µm)		
M3-M4	63	10	6.3	-	-	0.095	1.883
M3’-M4’	52.5	-	6.6	21x (2.5µm/1µm)	3x (2.5µm/1µm)		
M5-M6	57	10	5.7	-	-	0.25	1.017
M5’-M6’	30	-	6	12x (2.5µm/1µm)	3x (2.5µm/1µm)		
M7-M8	42	10	4.2	-	-	0.113	1.585
M7’-M8’	42.5	-	4.5	17x (2.5µm/1µm)	2x (2.5µm/1µm)		
M9-M10	42	10	4.2	-	-	0.113	1.585
M9’-M10’	42.5	-	4.5	17x (2.5µm/1µm)	2x (2.5µm/1µm)		
M11	15	10	1.5	-	-	0.05	3.049
M11’	5	-	1.7	2x (2.5µm/1µm)	1x (2.5µm/1µm)		

O amplificador OTA foi fabricado nas duas metodologias de leiaute em tecnologia CMOS digital 1.0µm. As geometrias projetadas W’s, L’s and W/L’s dos transistores do amplificador OTA estão listados na Tabela 4 (Table 5.7). Nota-se que a versão com TAT contém 100 transistores unitários contra 11 da versão totalmente customizada.

TABELA 5 - Simulação e medida experimental do desempenho dos OTAs em tecnologia CMOS digital 1.0μm (GBW_{NZ}=Normalizado).

	Simulação		Experimental	
	Tot. cust.	Semi-cust.	Tot. cust.	Semi-cust.
Tensão de Alimentação (V)	±2.5	±2.5	±2.5	±2.5
A_V (db)	106	92.4	64.5	62.9
GBW(MHz) @ C_L(pF)	4.5 / 10	7.7 / 10	0.186 / 82.4	0.514 / 53.5
GBW_{NZ} (MHz) @ C_L=50pF	0.9	1.54	0.307	0.550
SR (V/μs) @ C_L(pF)	3.46 / 10	5.89 / 10	0.42 / 82.4	1.10 / 53.5
Margem de fase (^{o})	80	76.2	79.4	51.7
$\|V_{os}\|$ (mV)	24	0.83	30	15
$V_{o\ max}$(V)	+2.2 / -1.3	+1.6 / -1.4	+1.1 / -0.7	+0.9 / -0.9
P_{diss} (mW)	0.50	2.78	0.87	1.38
SNR(dB) @ 500KHz/1MHz	-	-	99.1 / 97.9	94.1 / 92.8
THD (%)	-	-	5.9	9.8

Dos resultados experimentais fica claro que o amplificador OTA tem o ganho DC similar, enquanto as simulações demonstram ganhos maiores mas valores similares entre as versões. E ainda, a versão SOT tem maior produto ganho-faixa (GBW normalizado para C_L=50pF, quase 1.8 vezes maior) de acordo com as simulações. Os *slew-rates* são bastante próximos com as simulações, porém estão bem abaixo dos valores práticos devido à corrente de polarização do par diferencial (M11) ser muito baixa. O *offset* na versão SOT é menor do que no totalmente customizado, mostrando o melhor casamento devido ao bom padrão intrínseco do leiaute. Isto é, naturalmente transistores TAT são muito similares à técnica de interdigitação largamente utilizada em projetos de leiaute totalmente customizado.

TABELA 5 - Ruído experimetal em várias amostras de chips-de-teste com OTA *folded-cascode* em tecnologia CMOS digital 1.0μm. Versões com TATs.

	Amostra-1	**Amostra-2**	**Amostra-3**	**Amostra-4**	**Amostra-5**
SNR (dB) @ 0.5/1MHz	95.7 / 94.4	102 / 97.6	86.3 / 87.7	95.5 / 94.6	90.8 / 89.5
Ruído térmico (nV/√Hz) @0.5/1MHz	27 / 55	23 / 47	28 / 41	25 / 46	28 / 63
Ruído *1/f* (μV/√Hz)@1KHz	2.83	1.72	1.63	2.83	2.03
Corner 1/f (KHz)	456	426	420	486	416
THD (%)	11.11	15.21	6.72	9.89	5.99

O desempenho em ruído dos OTAs também foram investigados. Os resultados para as amostras com as versões SOT estão na Tabela 5 (Table 5.9b). A amostra-5 da Fig. 10 (Fig. B-1e) mostra que o ruído flicker em ambas as versões é alto pois depende da geometria (área L.W) do par

diferencial de entrada. Neste OTA, o par diferencial (M1-M2 na Tabela 5) tem área ativa pequena. Quanto aos ruídos térmicos das versões, são similares, como esperado (Eq. 7). Em relação à distorção harmônica total (THD), na média as não-linearidades presentes nas versões SOT foram maiores, como mostrados na Tabela 5. Pode-se minimizar estas não linearidades com melhor mapeamento dos transistores para associações TATs e com correntes de polarização dos transistores cascode (V_{DSsat}).

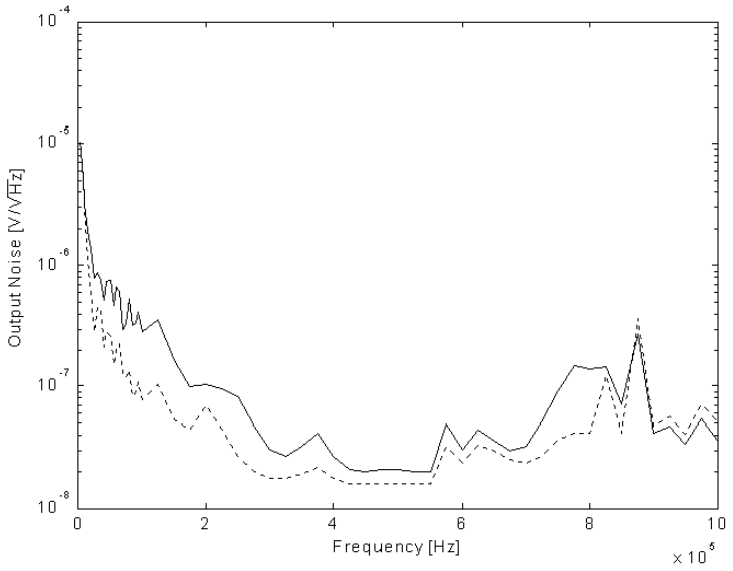


FIGURA 10 - Potência do ruído medido experimentalmente no OTA. Totalmente customizado (tracejado) e SOT (sólido). Amostra-5.

2.6 Implementação do Modulador Sigma-Delta na Matriz SOT Utilizando o Transistor TAT (Resumo do Capítulo 6)

Este capítulo é dedicado ao projeto do modulador Sigma-Delta (SD) para aplicação em sistemas em padrões GSM e DECT. Os objetivos principais neste projeto são: consumo de potência e relação sinal-ruído (SNR) do modulador SD, cuja degradação é causada pela não-linearidade dos integradores. Para a análise do modulador SD foi utilizado o simulador comportamental (Simulink, MatLab) a nível de sistema.

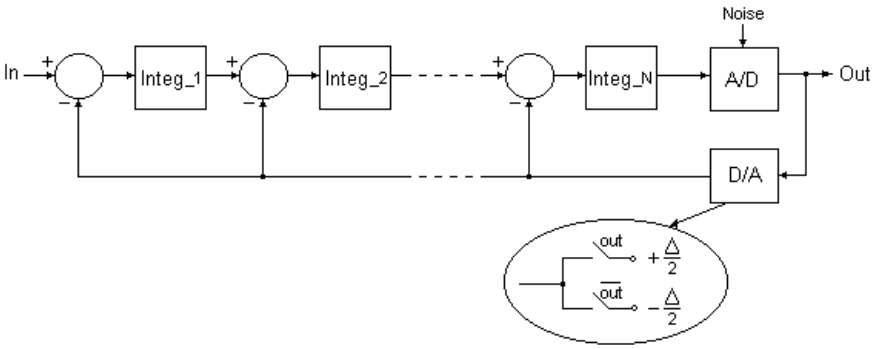


FIGURA 11 - Modulador Sigma-Delta básico de ordem *N*.

O conversor A/D and D/A de sobre-amostragem se tornou popular e muito utilizado devido à sua alta resolução com velocidade média-para-baixa em aplicações de áudio digital de alta qualidade, comunicações nas banda-de-voz, e outros. A popularidade destes conversores é devida ao relaxamento nos componentes analógicos com mais complexidade nos circuitos digitais. Este compromisso é mais desejável para as tecnologias mais modernas, 3V de tensão de alimentação, onde circuitos digitais complexos de alta velocidade são facilmente implementados em menor área de silício. Com o processo de conversão em alta taxa de sobre-amostragem, os componentes analógicos não necessitam de grandes tolerâncias ao casamento e ao ganho dos amplificadores. Outra vantagem é o relaxamento do filtro analógico anti-*alising* de entrada do A/D e filtros de saída do D/A.

O desempenho destes conversores (mostrado na Fig. 11 (Fig. 6.1) em sua arquitetura básica), pode ser caraterizado pela faixa dinâmica do sinal e potência do ruído na banda do sinal. Dada a ordem do modulador Sigma-Delta *N*, a faixa dinâmica do sinal *DR* é dada por [JAN93], [MAL99] (Eq. 6.1.1):

$$DR = \frac{3}{2} \cdot \left(\frac{V_{in_{\max}}}{\Delta} \right)^2 \cdot \frac{2N+1}{p^{2N}} \cdot OSR^{2N+1} \cdot \left(2^B - 1\right)^2 \qquad 16$$

onde B é o número de bits do conversor D/A, $V_{in_{\max}}$ é a amplitude pico-a-pico do sinal de entrada, Δ é o passo da quantização (referência de tensão $\pm\frac{\Delta}{2}$), e OSR é a taxa de sobre-amostragem. O desempenho global de um modulador Sigma-Delta (SDM) pode ser melhorado com o aumento da relação $\frac{V_{in_{\max}}}{\Delta}$ ou da taxa de sobre-amostragem OSR. Ainda, ordens N de SDM maiores, melhoram o desempenho. Porém, cascateando mais estágios de integradores em série, como mostrado na Fig.11, em torno da realimentação global pode causar instabilidades devido ao deslocamento de fase [CAN85], [BOS88], [UCH88]. No entanto, a realimentação é importante no SDM, pois a filtragem do ruído realimentado em torno do quantizador de 1-bit (comparador) tem o efeito de formatar o espectro do ruído quantizado.

O SDM de alta resolução desenvolvido aqui aplica a técnica MASH. Esta técnica permite construir SDM de ordens acima de 3 com SDM de ordens mais baixas (1 ou 2) em uma arquitetura paralelizada. As vantagens são: elimina o problema de instablidades em SDMs convencionais de ordens acima de 3; e reduz a necessidade de alta linearidade do conversor D/A. A desvantagem é o descasamento dos blocos componentes (por exemplo, o ganho) entre os estágios, pois degrada a relação sinal-ruído (*SNR*).

O SDM de 4ª oderm, estrutura Mash, mostrado na Fig. 12 (Fig. 6.4) foi desenvolvido em parceria com o grupo do Prof. M. Ismail, Laboratório Analog VLSI Lab, Ohio State University. Este SDM utiliza dois moduladores de 2ª ordem em paralelo.

Dentre a variedade de estratégias para propiciar a programabilidade de um SDM, foi escolhida a programação por seleção de capacitores unitários dispostos em uma matriz. Desta forma, pode-se ajustar os coeficientes dos filtros (integradores) para trocar as características/comportamento do original. Os maiores problemas estão na degradação do ruído, aumento de consumo de potência e maior área de silício.

As especificações/características do SDM para o padrão de comunicação GSM com largura de banda do sinal 100KHz são: resolução de 14 bits, *DR*=86dB, frequência de amostragem f_s=6.4MHz e taxa de sobre-amostragem entre *OSR*=18-32.

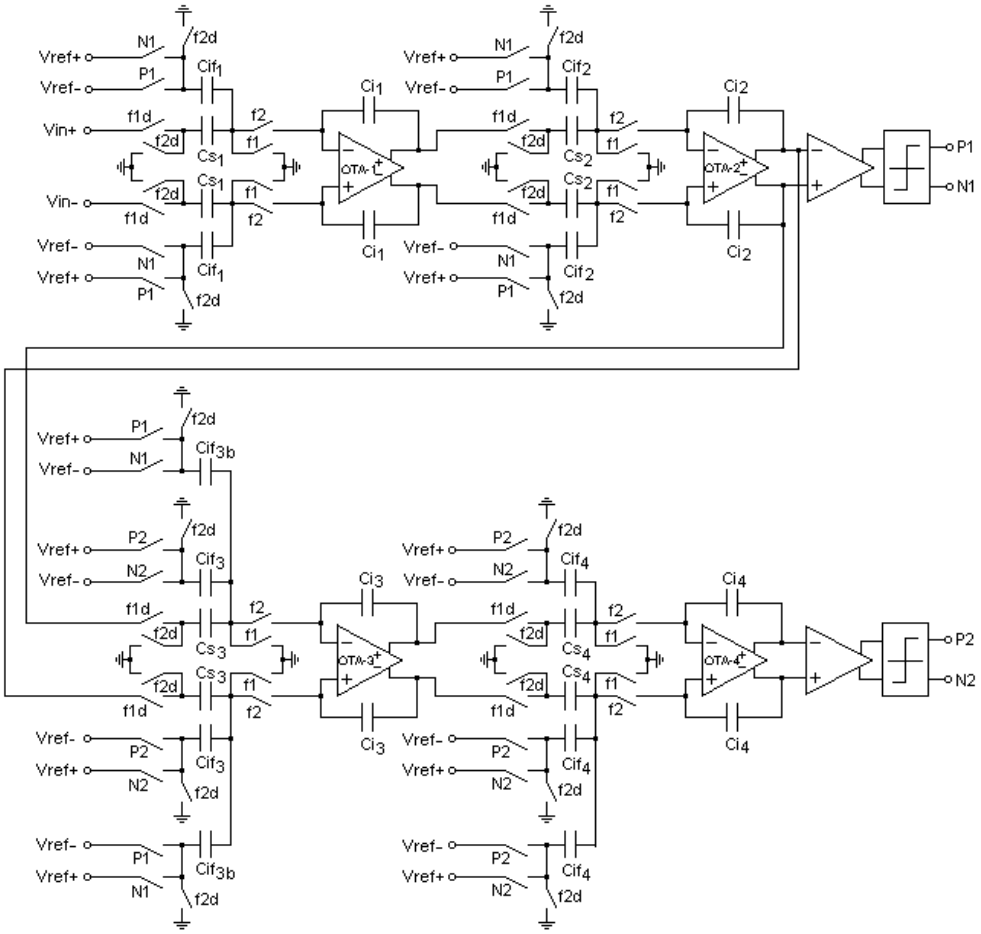
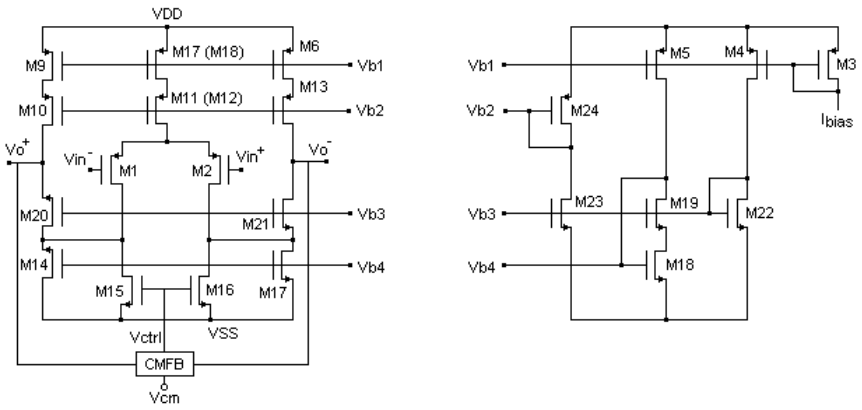


FIGURA 12 - Esquemático do SDM A/D 2-2 de 4^{o}-ordem.

As referências de tensão (D/A de 1-bit), indicados na Fig. 12, estão em V_{ref+}=+2.5V and V_{ref-}=+0.5V (tensão de alimentaçãoV_{DD}=3V), as quais são as excursões máximas do sinal de entrada definidos pelas especificações. O erro de ganho do integrador dever ser menor do que 2% e o *offset* do comparador *track-and-latch* (mesmo da seção anterior) menor do que 20*mV*. Para melhorar o *fan-out* de saída e memorizar e manter o sinal comparado durante o tempo de amostragem e comparação, respectivamente, é acoplada um *latch* tipo D na saída do comparador.

Os coeficientes de ganho de cada estágio também controlam a saturação da amplitude do sinal. Estes coeficientes foram definidos por simulações comportamentais a nível de sistema através do Simulink, Matlab. Os integradores devem controlar as excursões de pequenos sinais para: se obter alta faixa dinâmica do sinal e posterior alto desempenho (*SNR*); para minimizar a quantização do ruído; para a especificação dos OTAs (ganho, *slew-rate*, excursão de saída e tempo de *settling*); e para determinar a sensibilidade dos integradores e coeficientes de realimentação.

Como este SDM é totalmente diferencial – Fig. 12, um novo amplificador OTA, tipo *folded-cascode* totalmente diferencial (entrada e saída diferenciais), foi projetado e implementado, mostrado na Fig. 13a (Fig. 6.6a).



(a) (b)

FIGURA 13 - (a) Amplificador OTA totalmente diferencial *folded-cascode*. (b) Circuito de polarização.

O primeiro integrador, ou seja o amplificador OTA, deve ter alto desempenho, pois este atua como a interface de entrada do sistema conversor, acumulando na entrada os sinais de entrada e ruídos, direto e realimentado. E ainda, este bloco tem a responsabilidade de amplificar o sinal diferença de entrada e realimentado, e não pode introduzir mais ruídos e não-linearidades no sistema. O circuito de realimentação de modo-comum (CMFB– *common-mode feedback*), utilizado no OTA se baseia no circuito capacitor-chaveado, mostrado na Fig. 6.7 (pág. 102), seguindo o integrador que já é capacitor-chaveado e por ser geralmente preferido em relação ao modo contínuo, pois este tem a desvantagem de grande excursão de sinal. Geralmente, o capacitor C_2 é 1/4 a 1/10 do capacitor C_1 [JOH97]. Neste CMFB, os valores são (C_1=10C_2) C_1=1pF and C_2=0.1pF.

Todos os cuidados necessários foram considerados com as fontes de ruído (chaves, comparadores, integradores, capacitores e ruídos aleatórios (seção 6.3). O ruído total no sistema conversor deve ser o mínimo possível. Excluindo as fontes de ruído que estão fora de controle do projetista, o ruído total pode ser minimizado: pelo projeto do primeiro e segundo amplificadores OTA; projeto das chaves; e escolha da melhor arquitetura do SDM. O ruído gerado pelas chaves CMOS é relativamente controlado e as principais fontes são pela injeção de cargas do terminal porta para os terminais fonte e dreno durante as transições do relógio (*clock-feedthrough*). Esta fonte de ruído pode ser minimizada utilizando transistores de dimensões mínimas, com transição

lenta do relógio (formato trapezoidal) e utilizando uma arquitetura totalmente diferencial [CHO94], [ALE97]. Logo, a minimização das fontes ruídos em SDMs se reduzem ao projeto dos amplificadores OTAs.

O ruído em amplificadores OTAs pode ser minimizado aumentando a geometria W e L do par diferencial de entrada e das fontes de correntes (espelhos de corrente). Separando a influência de cada componente, o ruído total equivalente (*flicker* e térmico)é dado por (Eq. 6.3.2):

$$N_{OTA}^2 = N_{par}^2 + \left(\frac{g_{m_{ECor1}}}{g_{m_{M1}}}\right)^2 \cdot N_{ECor_n}^2 + \left(\frac{g_{m_{ECor2}}}{g_{m_{M1}}}\right)^2 \cdot N_{ECor_p}^2 \qquad 17$$

onde N_{par} é o ruído do par diferencial de entrada, N_{ECor_n} e N_{ECor_p} são os ruídos gerados pelas fontes de corrente $\left(\propto \frac{1}{L_{ECor}^2}\right)$, g_m é a transcondutância do OTA, e $g_{m_{ECor1}}$ e $g_{m_{ECor2}}$ são as transcondutâncias das fontes de corrente tipo N e P, respectivamente. A equação 17 demonstra que são necessários cuidados no projeto da geometria (W e L) do par de entrada, com menor valor possível na transcondutância e/ou aumentando o comprimento de canal das fontes de corrente.

Para garantir o correto tempo de *settling* e a estabilidade global, o *slew-rate* SR mínimo foi fixado (definição deste projeto) em parte do semi-ciclo ativo da frequência de amostragem para assegurar correta amostragem do sinal, evitando possíveis problemas com *jitters* de relógio e não-linearidades.

Nos integradores capacitor-chaveados, os valores dos capacitores que definem os coeficientes dos filtros (ganho) iguais ou menores do que $0.1pF$ foram re-dimensionados para evitar imprecisões causadas por capacitores pequenos (*undercutting* do processo, efeito das bordas, etc) durante o processo de fabricação do circuito integrado. A técnica de capacitores unitários foi utilizada neste projeto para minimizar estes efeitos [ALE97], [CHO94], [GRE86].

Os subcircuitos analógicos e SDM projetados foram implementados em *chips*-de-teste em ambas as metodologias de leiaute (semi-customizada SOT e totalmente customizada) em tecnologia CMOS 0.5µm, dois níveis de poly, três níveis de metal. Todos os leiautes, semi- e totalmente customizados, foram projetados à mão, sem nenhuma assistência de uma ferramenta de geração de leiaute automática. Consequentemente, os leiautes na matriz SOT não foram otimizados em área, máxima ocupação das bandas, e simetria dos circuitos. Os leiautes totalmente customizados têm melhor posicionamento geométrico e otimização em área do que na versão em matriz SOT. Porém, os amplificadores OTAs, em particular, não foram otimizados em área.

O tipo de encapsulamento dos CIs da MOSIS (*foundry* americana) é um DIP40 (40 pinos) para tecnologia CMOS 0.5µm da AMI e HP, com área total do *chip* de 1500µm x 1500µm, incluindo os *pads* de entrada e saída. Sem os *pads*, a área total disponível para implementação de circuitos é de 1100µm x 1100µm. Esta restrição de área foi a limitação para projeto maior de subcircuitos e sistemas em metodologia matriz SOT. O desempenho elétrico simulado dos SDMs estão nas figuras do Apêndice D.

Três *chips* foram fabricados. O primeiro *chip*, foto mostrada na Fig. D-2 - Appendix D, contêm uma estrutura de transistores, o primeiro amplificador OTA do SDM, e o comparador *track-and-latch* (semi-customizado matriz SOT e totalmente customizado). Desta forma permite uma comparação mais fiel entre os blocos e as metodologias de leiaute, pois as células são posicionadas lado-a-lado na mesma pastilha de silício, minimizando as variações de processo de *chip* para *chip*.

O segundo (totalmente customizado) e terceiro (semi-customizdo matriz SOT) chips-de-teste, fotos mostradas nas Figs. D-3 and D-4 - Appendix D, respectivamente, contêm os SDMs de 2^o-ordem. Junto com os SDMs, foram incluídos os amplificadores simples de fonte-comum no segundo *chip* (foto da Fig. D-3) e espelhos de corrente (M1-M2 e M1'-M2') no terceiro *chip* (foto da Fig. D-4). Os leiautes detalhados de cada subcircuito analógico estão mostrados em: espelhos de corrente - Fig. D-5, amplificadores simples de fonte-comum - Fig. D-6, comparador - Fig. D-7, primeiro e segundo amplificadores OTAs - Fig. D-9 e Fig. D-8.

Todos os blocos componentes foram testados experimentalmente e validados. O desempenho experimental comparando as versões totalmente customizado e semi-customizado matriz SOT dos espelhos de corrente, amplificadores simples de fonte-comum e comparadores é apresentada nas Tabelas 6, 7 e 8 (Tabelas 6.8, 6.9 e 6.10), respectivamente.

Observa-se erros de corrente no espelho de corrente entre o simulado e medido na Tabela 6: os erros previstos na simulação são maiores para os espelhos de corrente com TATs. O erro na versão com TAT é pouco pior devido ao efeito de canal curto e efeito de corpo (MD) presentes nos transistores de L mínimos.

TABELA 6 - Erro simulado e medido nos espelhos de corrente (nFET) em tecnologia CMOS 0.5µm. E.Corr_1: L=1.2µm, W=102µm, ND=9, NS=9 (5.4µm/0.6µm). E.Corr_2: L=6µm, W=102µm, ND=45, NS=5 (1.2µm/0.6µm). Média de 7 amostras.

Metodologia	**Erro Simulado (%)**		**Erro Experimental (%)**	
	E.Corr_1 (L=1.2µm)	E.Corr_2 (L=6µm)	E.Corr_1 (L=1.2µm)	E.Corr_2 (L=6µm)
Totalm-cust.	3.22	0.02	4.88	4.26
Semi-cust.	14.42	1.38	5.31	-0.43

TABELA 7 - Desempenho experimental do amplificador fonte-comum totalmente-customizado e semi-customizado em tecnologia CMOS 0.5µm. Média de 9 amostras.

Amplificador simples de fonte-comum		
	Totalm.-cust.	**Semi-cust.**
V_{DD} (V) / C_L (pF)	3 / 1200	3 / 1200
A_v (dB)	33.0	29.9
f_T (KHz)	318.5	268.2
MF (o)	86.4	83.9
SR (V/µs)	0.114	0.086
V_o max (V)	2.2 / 0.7	2.0 / 0.8

TABELA 8 - Desempenho experimental do comparator totalmente-customizado e semi-customizado em tecnologia CMOS 0.5µm. Média de 5 amostras.

Comparador		
	Totalm.-cust.	**Semi-cust.**
V_{DD} (V)	3	3
f_{max} (MHz)	41.1	30.5
Sensibilidade (mV)	7.33	14.2

Como esperado, o desempenho da versão com TAT do amplificador fonte-comum é menor do que o seu equivalente totalmente customizado – Tabela 7. O ganho DC é similar para ambas as metodologias de leiaute e a frequência de corte mais baixa para o semi-customizado. Novamente, o desempenho experimental e simulado é similar demostrando a boa aproximação dos modelos elétricos. A mesma comparação é válida para o comparador *track-and-latch* – Tabela 8. A máxima frequência de chaveamento da versão com TAT é aproximadamente 25% menor e a sensibilidade mínima é duas vezes maior. No entanto, a sensibilidade simulada foi menos otimista (maior) e a velocidade super-estimada, esta última devido à estimação não-realista dos efeitos parasitas (capacitâncias e resistências).

TABELA 9 - Primeiro amplif. OTA *folded-cascode* totalmente dif.: desempenho experimental da versão com TAT em tecnologia CMOS 0.5µm. Média de 5 amostras.

OTA *folded-cascode* totalmente dif.	
	Semi-cust.
V_{DD} (V)	3
C_L (pF)	82
A_v (dB)	59.0
f_T (MHz)	1.167
MF (o)	148
SR (V/µs)	1.177
V_{os} (mV)	9.2
V_o máx (V) / V_o mín (V)	2.1 / 1.1

TABELA 10 - SDM de 2º ordem: desempenho experimental da versão com TAT em tecnologia CMOS 0.5µm. Média de 4 amostras.

SDM 2º-ordem / OSR=64 (versão com TAT)	
Sinal de entrada & Freq. de amostragem	**SNR (dB)**
Senoidal 5KHz / f_s = 6.9MHz	75.1
Senoidal 7KHz / f_s = 6.9MHz	69.1
Senoidal 1KHz / f_s = 1.7MHz	63.4

As Tabelas 9 e 10 (Tabela 6.11 e Tabela 6.12) mostram os desempenhos do amplificador OTA totalmente diferencial e do SDM de 2ª ordem. O desempenho comparativo destes circuitos implementados com ambas as metodologias de leiaute semi- e totalmente customizadas foi prejudicado, pois a versão totalmente customizada apresentou erros de projeto de leiaute. Erros nos leiautes dos circuitos fabricados foram encontrados no amplificador OTA e integradores capacitor-chaveados que impediram de funcionar. No entanto, os resultados experimentais mostram um bom desempenho de circuitos em metodologia matriz SOT com transistores TAT.

O desempenho da versão com TAT do amplificador OTA está mostrado na Tabela 9 (Table 6.11). As simulações e medidas utilizaram uma corrente de polarização externa ao *chip* fixada em 50µA. A medida da excursão de saída de aproximadamente 1V é uma restrição relativamente severa, causada pela arquitetura intrínseca do TAT e correntes de polarização do par diferencial de entrada e ramos *folded* de saída. As comparações de f_T e *slew-rate* não foram realizadas devido às altas cargas capacitivas presente nos *chips* e equipamentos de medida que influenciaram o desempenho global do OTA.

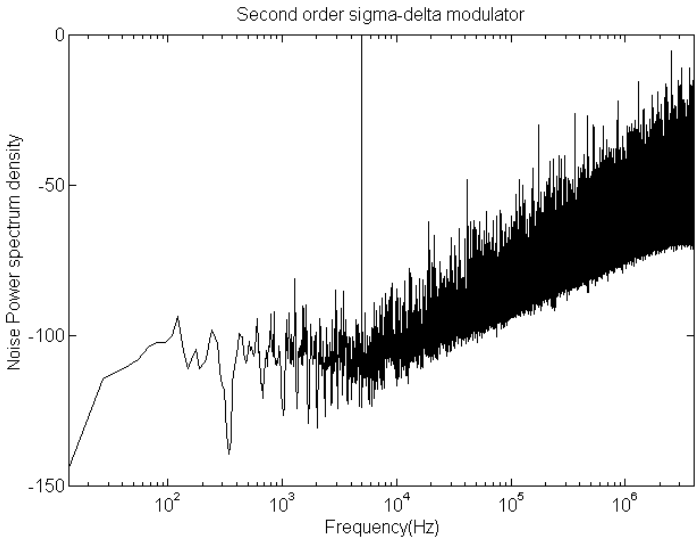


FIGURA 14 - Espectro da densidade de potência do ruído experimental: SDM de 2^o ordem, versão com TAT, tecnologia CMOS 0.5µm. Sinal de entrada: senoidal a 5KHz; f_s=6.9MHz e *OSR*=64. Média de 4 amostras.

Finalmente, a validação da técnica TAT para aplicações analógicas e mistas na matriz SOT está na Tabela 10 (Tabela 6.12) e mostra o bom desempenho alcançado pelo SDM em metodologia matriz SOT. Apesar de alguns efeitos parasitas nas medidas, a relação sinal-ruído medido permite uma resolução entre 11 e 12 bits. O espectro da potência do ruído é mostrado na Fig. 14 (Fig. 6.11). A potência rms do ruído na banda do sinal é aproximadamente -110dB.

3 Conclusão

Este trabalho demonstrou uma técnica inovativa para o projeto analógico-digital de sinais mistos sobre a matriz digital pré-difundida semi-customizada, demonstrando que a abordagem TAT é uma boa alternativa para aplicações ASICs analógicas semi-customizadas. A utilização de matrizes TAT e o mapeamento de transistores convencionais totalmente customizado para TAT são relativamente simples. As análises DC, AC e ruído foram comparadas com os resultados obtidos das simulações elétricas e experimentais. Os resultados comparativos demonstraram poucas diferenças entre os valores esperados e desempenhos teóricos e experimentais do TAT. Estes resultados foram publicados em artigos em diversas conferências e revistas, tais como [CHO99c], [CHO99b], [CHO99a], [CHO2000c], [CHO2000b], [CHO2000a], [CHO2001].

Diversos dispositivos MOSFETs foram fabricados e testados para facilitar a análise dos transistores TATs em emular os seus equivalentes transistores simples. Os chips-de-teste foram fabricados com um estrutura de transistores tendo diferentes geometrias de TAT (L, W, W/L) e seus equivalentes transistores MOSFET simples, ambos em tecnologia CMOS 0.5µm e 1.0µm. Os ótimos resultados obtidos para os TATs demonstraram que estes são adequados para emular transistores simples. Outra vantagem importante do TAT é a melhora em uma das suas características, ou seja, na condutância de saída, a qual garante a utilização de transistores de comprimento de canal mínimo em circuitos analógicos semi-customizados. Os resultados obtidos na seção 5.1 para espelhos de correntes na cópia de corrente (alta impedância de saída), confirmam que a condutância de saída é melhor em TATs.

A redução da transcondutância do TAT nas regiões de condução e de saturação (seção 4.3 – equação 4.3.5) pode ser considerada com o projeto adequado do W/L equivalente (relação do transistor MS). Os efeitos de canal curto (seções 4.2 e 4.5) presentes nos TATs podem ser vantajosos para aplicações de baixa tensão de alimentação em sub-circuitos analógicos em VLSI/ULSI digital semi-customizada. A maior preocupação em relação ao TAT é o desempenho em ruído (seções 4.4 e 5.4), devendo-se tomar cuidado com as fontes de ruído. O transistor TAT é mais ruidoso do que o seu equivalente transistor simples, já que transistores de canal mínimo são empregados na associação dos TATs. Entretanto, quanto maior ND ou NS nas associações de MD e MS, respectivamente, as desvantagens em ruído do TAT podem ser compensadas, mantendo inalterada a relação W/L equivalente. Para aplicações de baixo ruído, associações em maior área, de dezenas ou talvez algumas centenas de transistores unitários, são necessárias. Embora a potência

total do ruído seja maior e haja algumas limitações naturais (efeito de corpo, canal mínimo e grande área de silício), os transistores TAT na matriz SOT apresentaram um bom desempenho.

Diversos circuitos analógicos (espelhos de corrente, amplificadores de um estágio, comparadores *track-and-latch*, OTAs) também foram projetados e fabricados. Nos capítulos 5 e 6, os OTAs implementados na matriz SOT (1.0µm and 0.5µm) indicam um bom desempenho do TAT e implementação de circuitos analógicos totalmente semi-customizados empregando somente dispositivos TAT.

Os ganhos e as margens de fases (seções 5.2 e 6.8) são estáveis mesmo com a presença adicional do nodo interno intermediário no TAT. As capacitâncias parasitas no TAT são similares ao seu equivalente simples. As combinações das principais capacitâncias que influenciam o desempenho AC do TAT são as capacitâncias entre os terminais porta-fonte e porta-dreno do transistor MS e entre os terminais porta-fonte e porta-dreno do transistor MD. O ganho do amplificador TAT, resultado do efeito *cascode*, pode ser maior do que a sua versão simples (totalmente customizada) apenas melhorando a condutância de saída do transistor MD e elevando a transcondutância do MS. Devendo ser respeitada a restrição para TAT, ou seja, as associações em paralelo com transistores unitários de MD e MS devem ser trapezoidais: MD maior do que MS.

A maioria das deficiências do TAT não impedem sistemas mistos e analógicos sobre a matriz digital, dos quais as principais desvantagens já foram estudadas. A técnica TAT demonstrou que possui um bom compromisso, para uma dada aplicação, entre desempenho, custo e tempo de projeto e prototipação. E mais, como já descrito, esta técnica não está restrita somente para matrizes pré-difundidas, isto é, pode ser utilizada vantajosamente até mesmo em metodologia totalmente customizada para analógicos. Isto permite o projeto de leiautes analógicos mais rápido (rápida prototipação) e a maior vantagem é o baixíssimo custo de implementação de circuitos mistos analógico-digitais com a tecnologia digital.

Os próximos passos deste trabalho serão: (1) a extração dos parâmetros dos modelos para comparação entre simulação e experimental do TAT e transistor simples; (2) a análise experimental do ruído no TAT (único); (3) a modelagem RF do TAT; (4) o projeto da versão totalmente customizada do modulador Sigma-Delta e OTA; e (5) o desenvolvimento do gerador automático do TAT e ferramentas de automação de leiaute (posicionamento&roteamento sobre a matriz SOT).

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