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**Low Power SAR Analog-to-Digital
Converter for Internet-of-Things RF
Receivers**

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Coadvisor: Prof. Dr. Eric Fabris

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"...

*and when we speak we are afraid
our words will not be heard
nor welcomed
but when we are silent
we are still afraid*

*So it is better to speak
remembering
we were never meant to survive."*

— AUDRE LORDE, *THE BLACK UNICORN: POEMS*

*"Le jour où il sera possible à la femme
d'aimer dans sa force, non dans sa faiblesse,
non pour se fuir, mais pour se trouver,
non pour se démettre, mais pour s'affirmer,
alors l'amour deviendra pour elle, comme pour l'homme,
source de vie et non mortel danger."*

— SIMONE DE BEAUVOIR, *LE DEUXIÈME SEXE*

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— HELGA DORNELAS

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ABSTRACT

The "Internet of Things" (IoT) has been a topic of intensive research in industry, technological centers and academic community, being data communication one aspect of high relevance in this area. The exponential increase of devices with wireless capabilities as well as the number of users, alongside with the decreasing costs for implementation of broadband communications, created a suitable environment for IoT applications. An IoT device is typically composed by a wireless transceiver, a battery and/or energy harvesting unit, a power management unit, sensors and conditioning unit, a microprocessor and data storage unit. Energy supply is a limiting factor in many applications and the transceiver usually demands a significant amount of power. In this scenario the emerging wireless communication standard IEEE 802.11ah, in which this work focuses, was proposed as an option for low power sub-GHz radio communication.

A typical architecture of modern radio receivers contains the analog radio-frequency (RF) front-end, which amplifies, demodulates and filters the input signal, and also analog-to-digital converters (ADC), that translate the analog signals to the digital domain. Additionally, the Successive-Approximation (SAR) ADC architecture has become popular recently due to its power efficiency, simplicity, and compatibility with scaled-down integrated CMOS technology. In this work, the RF receiver architecture and its specifications aiming low power consumption and IEEE 802.11ah standard complying are outlined, being the basis to the proposition of an 8-bit resolution and 10 MHz sampling rate ADC. A power efficient switching scheme for the charge redistribution SAR ADC architecture is explored in detail, along with the circuit-level design of the digital-to-analog converter (DAC). The transistor-level design of the two remaining ADC main blocks, sampling switch and comparator, are also explored. Electrical simulation of the physical layout, including parasitics, at a 130nm CMOS process resulted in a SINAD of 47.3 dB and 45.5 dB and at the receiver IF 3 MHz and at the Nyquist rate, respectively, consuming 21 μW with a power supply of 1 V. The SAR ADC resulting Figure-of-Merit (FoM) corresponded to 11.1 fJ/conv-step at IF, and 13.7 fJ/conv-step at the Nyquist rate.

Keywords: CMOS Analog Design. Analog to Digital Converter. Low Power Design. Successive Approximation ADC. Internet of Things.

Conversor Analógico-Digital SAR de Baixo Consumo para Receptores RF de Internet-das-Coisas

RESUMO

O conceito de Internet-das-Coisas (do inglês, IoT) tem sido um tópico de interesse e pesquisa intensa na indústria, centros tecnológicos e comunidade acadêmica, sendo a comunicação de dados um de seus aspectos mais relevantes. Um dispositivo IoT tipicamente consiste de: transceptor sem-fio, bateria e/ou unidade de coleta de energia, unidade de gerenciamento de potência, sensores e memória. Em um sistema de comunicação sem-fio de baixa potência, todos blocos devem ser projetados de maneira a minimizar o consumo de potência e, frequentemente, o transceptor tem maior impacto no consumo. Nesse sentido, o emergente padrão de comunicação sem-fio IEEE 802.11ah foi desenvolvido a fim de incluir cenários IoT, na faixa do espectro de frequência sub-GHz, tornando-se, portanto, apropriado para implementação em sistemas de rádio de baixo consumo. Uma arquitetura típica de rádios receptores inclui não somente o *front-end* de rádio-frequência analógico, que amplifica, demodula e filtra o sinal de entrada, mas também o conversor analógico-digital (do inglês, ADC), responsável pela conversão de dados entre os domínios analógico e digital. Neste âmbito, ADCs são blocos essenciais ao possibilitar o processamento digital de sinais (do inglês, DSP), comumente presente em sistemas de chip modernos. Ademais, ADCs do tipo Aproximação Sucessiva (do inglês, SAR) tornaram-se recentemente mais populares devido a sua eficiência energética, simplicidade e compatibilidade com o escalonamento de tecnologias CMOS. No presente trabalho, arquitetura e especificações de um receptor de baixa potência de acordo com o padrão de comunicação sem-fio IEEE 802.11ah são apresentados, assim como a definição de resolução de 8 bits e taxa de amostragem de 10 MHz para o ADC. Seleção e projeto de um esquema de chaveamento para uma topologia de redistribuição de cargas do ADC SAR são exploradas em detalhe, assim como o projeto a nível de circuito do conversor digital-analógico. O projeto a nível de transistor do comparador e do amostrador também são apresentados. Simulação do leiaute implementado em processo CMOS de 130 nm resultou em um SINAD de 47.3 dB e 45.5 dB na frequência intermediária do receptor, 3 MHz , e na taxa de Nyquist, respectivamente, consumindo $21\text{ }\mu\text{W}$ com uma fonte de alimentação de 1 V . O projeto do ADC SAR resultou numa figura de mérito de 11.1 fJ/conv-step a 3 MHz , and 13.7 fJ/conv-step na taxa de Nyquist.

Palavras-chave: Projeto de Circuito Analógico CMOS, Conversor A/D, Projeto de Baixa Potência, ADC por Aproximação Sucessiva, Internet das Coisas.

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LIST OF ABBREVIATIONS AND ACRONYMS

ADC	Analog-to-Digital Converter
AMS	Analog and Mixed Signal
A/D	Analog-to-Digital
BER	Bit Error Rate
CMOS	Complementary Metal-Oxide-Semiconductor
C_S	Sampling Capacitor
C_{min}	Minimum Capacitor
C_{unit}	Unit Capacitor
DAC	Digital-to-Analog Converter
DAC _{p/n}	Positive/ Negative DAC array
DFT	Discrete Fourier Transform
DNL	Differential Nonlinearity
DSP	Digital Signal Processing
D/A	Digital-to-Analog
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
f_B	Signal Frequency, Signal Bandwidth
f_{clk}	Clock Frequency
f_{comp}	Comparator Frequency
FoM	Figure of Merit
f_{Ny}	Nyquist Frequency, Nyquist Rate
f_S	Sampling Frequency, Sample Rate
FS	Full Scale
GND	Ground

HBSI	Higher-Bit Switching Instead
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
INL	Integral Nonlinearity
IoT	Internet of Things
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low Power
LSB	Least Significant Bit
MCS	Modulation Coding Schemes
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOS	Metal-Oxide-Semiconductor
MOSCAP	Metal-Oxide-Semiconductor Capacitor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MSB	Most Significant Bit
n	Number of Bits, or Resolution
NF	Noise Figure
NMOS	N-channel MOSFET
OpAmp	Operational Amplifier
OSSI	One-Side Switching Instead
PGA	Programmable Gain Amplifier
PHY	Physical Layer
PMOS	P-channel MOSFET
PNoise	Periodic Noise Analysis
PSS	Periodic Steady-State Analysis

RF	Radio-Frequency
R_{on}	On-Switch Resistance
RX	Receiver
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SINAD	Signal-to-Noise-and-Distortion Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
t_{comp}	Comparator Response Time
t_{cycle}	Conversion Cycle Period
t_{DAC}	DAC Response Time
T_S	Sampling Period
t_{SAR}	SAR Response Time
ULP	Ultra-Low Power
V_{cm}	Common Mode Voltage
V_{DD}	Power Supply
V_{DS}	Drain-to-Source Voltage
$V_{G/GS}$	Gate Voltage; Gate-to-Source Voltage
V_{in}	Input Voltage
$V_{refp/n}$	Positive/Negative Reference Voltage
V_{th}	Threshold Voltage
WSN	Wireless Sensor Networks

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1 INTRODUCTION

1.1 The Internet of Things

The concept of the Internet of Things (IoT) has been a topic of increasing discussion both in academic community and industry (LIN et al., 2017; MANYIKA et al., 2015). The primary purpose of the IoT concept is the ability to monitor and manage a wide variety of objects in the physical world electronically, as well as exchange and storage input data through wireless communication systems. The Internet of Things has a broad range of applications such as wearables, health care, transportation, industrial automation, smart buildings and smart cities (SAHA; MANDAL; SINHA, 2017).

Smart objects along with their supposed tasks constitute domain-specific applications (vertical markets) while ubiquitous computing and analytical services form application domain independent services (horizontal markets) (AL-FUQAHA et al., 2015). Figure 1.1 illustrates the overall concept of the IoT in which every domain-specific application is interacting with domain-independent services, whereas in each domain sensors and actuators communicate directly with each other.



Figure 1.1: Examples of applications on the IoT market (AL-FUQAHA et al., 2015).

Broadband communication is available virtually everywhere at decreasing connection costs. The number of devices or with wireless capability grows every day, associated with ever reducing manufacturing costs. Mobile communication systems, in contrast, increases exponentially, along with the overall number of users. This set of factors has created a suitable environment for the expansion of Wireless Sensor Networks (WSN) and IoT applications.

A significant number of communication standards have been developed to attend the demands of WSN and IoT applications, such as Bluetooth Low Energy (BLE), ZigBee, LoRaWan and Wi-Fi HaLow (IEEE 802.11ah) (GAZIS, 2017). The IEEE 802.11ah is a wireless networking protocol published in 2017 as an amendment to the 802.11 standard (Wi-Fi) addressing the gap between traditional mobile networks and the growing demand for WSN. Seeing that the Wi-Fi HaLow is an emerging standard which has only been recently published, it represents a promising alternative for WSN and IoT.

The IEEE 802.11ah deals with the specification in the sub-1GHz license-exempt frequency spectrum to support a broad set of scenarios based on a large number of low data rate devices, a long range and energy constraints (ADAME et al., 2014). Therefore, suitable low power radio systems are desired to comply with the standard requirements.

A low power wireless system comprises a number of functional blocks in addition to the wireless transceiver, as shown in Figure 1.2. An IoT “node” will typically consist of a battery or energy harvesting unit as the energy source, a power management unit, data storage unit, sensors and wireless transceiver that generate and condition the environmental data which is processed typically by a microcontroller. In a low-power wireless system, all these blocks must be carefully specified and designed to minimize the total power consumption. However, it is often the wireless transceiver which consumes the highest power when active of all the blocks (BURDETT, 2015). Thus, to minimize the overall power consumption, a radio architecture must be appropriately selected to attend standard requirements, as well as power optimization strategies must be implemented.

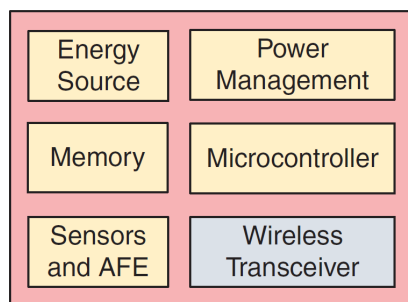


Figure 1.2: Block diagram of an IoT Node (BURDETT, 2015).

The usual architecture of modern radio receivers is composed by an analog radio-frequency (RF) front-end, which amplifies the antenna receiving signal, converts its frequency and selects its spectrum by filtering. The output signal is then digitized by an analog-to-digital converter, and finally demodulated and reconstructed by digital processing.

1.2 Data Converters

Although signal processing can be performed by analog electronic circuits, in many complex situations analog processing lacks required functionality. Digital signal processing (DSP) fills this gap in functionality. Important advantages of digital processing over analog processing are perfect storage of digitized signals, unlimited signal-to-noise ratio, the option to carry out complex calculations, and the possibility to adapt the algorithm of the calculation to changing circumstances (PELGROM, 2010).

To benefit from the DSP advantages, an analog signal must first be converted to a digital format, a task which is performed by an Analog-to-Digital Converter (*A/D converter* or ADC). The reverse procedure, that is, conversion from digital to analog domains, is performed by a Digital-to-Analog Converter (*D/A Converter* or DAC). Provided that our world is made of physical quantities, which are inherently analog, the data conversion represents an essential step in connecting our world to modern electronic systems and computing machines, which process and store information primarily in a digital format.

The DSP chain is illustrated in Figure 1.3, in which the ADC converts the analog signal collected by the microphone into a digital signal. In a digital format, the data collected can be adjusted or modified with computer software. Finally, the modified data is converted to an analog signal and reproduced in a sound system. The waveforms of each step are also shown.

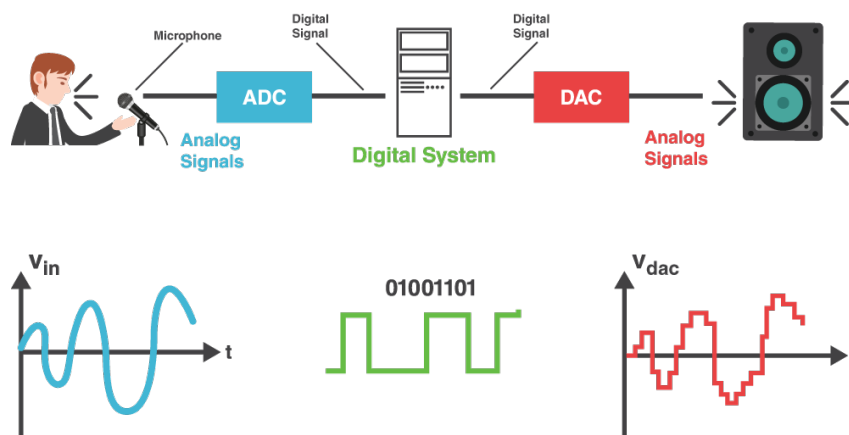


Figure 1.3: Block diagram of a Digital Processing System.

The conversion process involves **sampling** and **quantization** of the input analog signal, which inevitably introduces a rounding error. Additionally, the quantized and sampled signal is only meaningful when a relationship exists between the digital number range considered and a physical reference value. These three functions, represented in Figure 1.4, characterize the analog-to-digital converter.

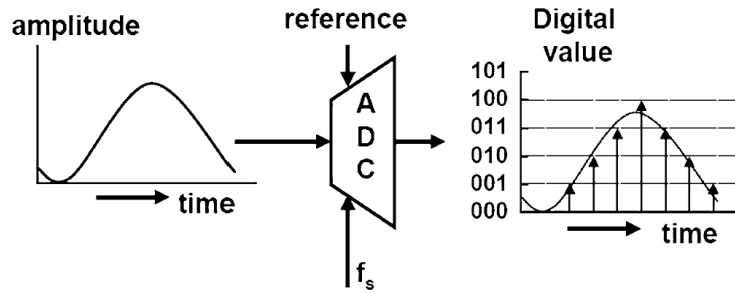


Figure 1.4: Functions of the A/D Converter: sampling in time, quantizing in amplitude and linking to a reference (PELGROM, 2010).

Data converters have often been a critical bottleneck in determining how much signal information can move between analog and digital domains. Traditionally, *bandwidth* and *dynamic range* are considered the two fundamental dimensions of any signal processing problem (ROBERTSON, 2015). Signal bandwidth is directly related to the **sample rate**, f_s (based on the Nyquist theorem) and dynamic range to the **converter resolution**, or number of bits n (based on the signal-to-quantization noise ratio). However, other parameters can be as meaningful as the sample rate and the number of bits for characterizing the performance of data converters, depending on the context and application. **Power consumption** can often be taken as a third dimension, especially in the context of IoT applications.

Together with the quantization noise, distortion and noise introduced by the data converter will also affect the accuracy of its output. In that sense, a n -bit converter will not necessarily have the full accuracy or precision implied by n . The effective number of bits (ENOB) is a broader metric for representing converter resolution, and it has long been used as an alias for the signal-to-noise-and-distortion ratio (SNDR or, equivalently, SINAD), represented in Figure 1.5. In the case of a pure, full-scale digitized sinusoidal signal at a given frequency f_{sig} this is:

$$ENOB(f_{sig}) = \frac{SNDR_{dB}(f_{sig}) - 1.76dB}{6.02dB} \quad (1.1)$$

where ENOB is a real number, expressed in bits, while $SNDR_{dB}$ is a dimensionless real number expressed in decibel (dB).

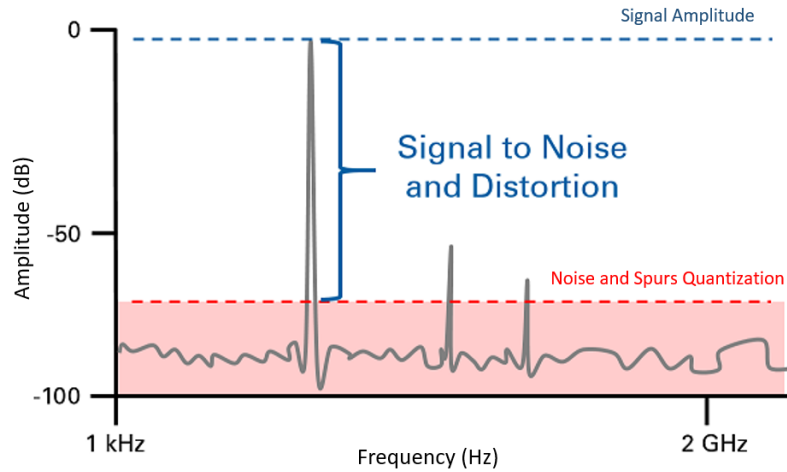


Figure 1.5: Illustration of the signal-to-noise-and-distortion ratio of a signal (NATIONALINSTRUMENTS, 2017).

Figure 1.6 shows a collection of data converters classified by their architectures in terms of energy per conversion (power consumption P divided by the sampling rate f_s) and accuracy, expressed as SNDR (HARPE, 2016). As one can see, Successive-Approximation Register (SAR) A/D Converters are very power efficient architectures for medium accuracies between 40 and 70 dB. SAR ADCs stand out because they consist mainly of simple analog and digital circuits which are compatible with the increasingly scaled-down technology. Their simple structure also allows operation at reduced supply levels, which can save additional power.

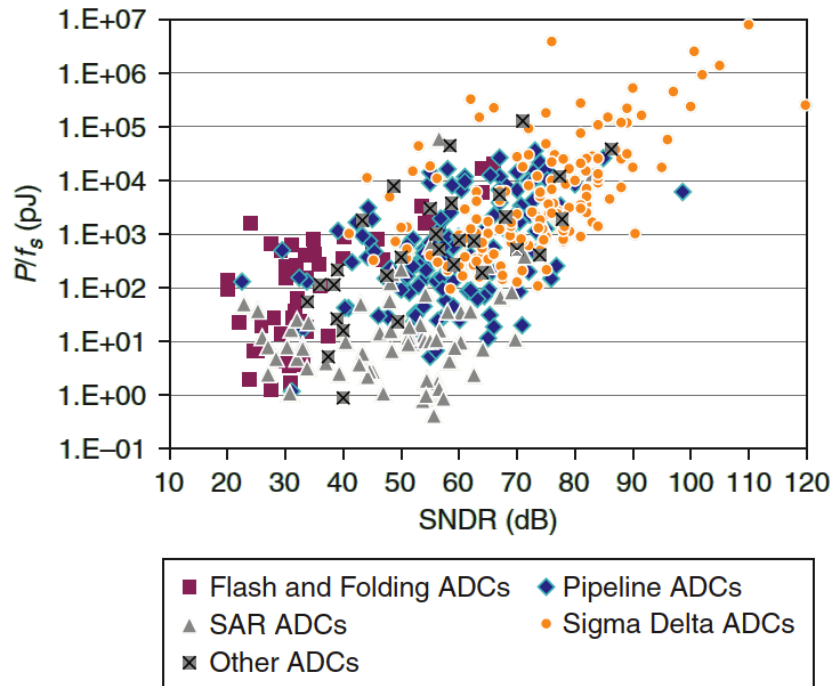


Figure 1.6: An ADC performance benchmark with data converters specified in terms of energy per conversion versus SNDR (HARPE, 2016).

1.3 Objectives

Energy efficiency is one of the critical attributes of emerging ultra-low power sensing and monitoring systems. Applications aimed for WSN and the IoT market require ultra-low power (ULP) radio designs, which includes the design of ADCs that convert the received signals to digital domain, enabling the use of digital signal processing for data demodulation. Such ULP radio typically complies with a wireless communication standard. In that sense, the wireless communication standard selected is the emerging IEEE 802.11ah and specifications and architecture of the A/D Converter are defined accordingly. Finally, the design of the SAR ADC topology chosen is presented, focusing on the power efficiency of the switching scheme and DAC design. Additionally, the fundamental dimensions, sample rate, resolution and power consumption, along with supply levels limits are also subject of investigation.

1.4 Organization

This work is organized as follows: a brief overview of the Wi-Fi HaLow standard as well as the ULP radio architecture and specifications, specifically for the receiver, will be presented in Chapter 2. Chapter 3 explores the basics of ADCs and its different architectures, the SAR topology and presents bibliographic review. Chapter 4 presents the architecture of SAR ADC, the switching scheme as well as the design of internal blocks. Simulation results are presented and discussed in Chapter 5. Finally, conclusions are drawn in Chapter 6. The appendix contains the SAR code employed in this work.

2 LOW POWER WIRELESS TRANSCEIVER FOR IOT

The wireless communication system for IoT applications usually has to operate with severe power source restrictions. It comprises a number of functional blocks which must be thoroughly specified and designed to minimize the total power consumption. It is often the wireless transceiver, however, which consumes the highest power when active. Thus the radio architecture must be carefully selected to attend the communication needs and wireless standard requirements as well as to minimize power consumption.

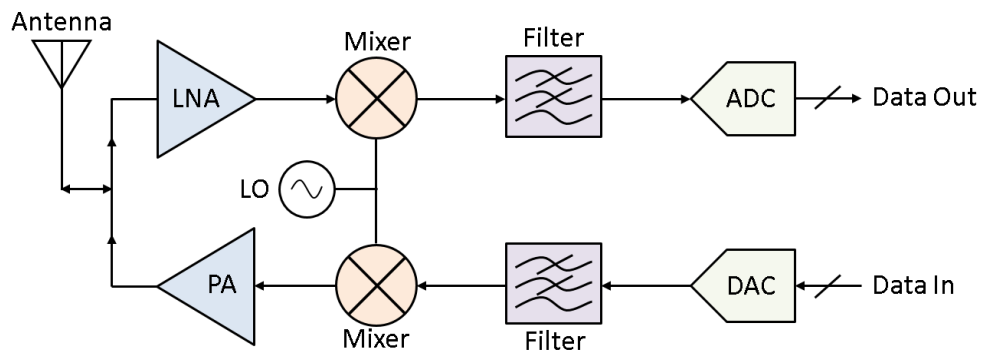


Figure 2.1: Transceiver main blocks. The antenna is shared by both receiver and transmitter. Low Noise Amplifier (LNA), Mixer, Filter and ADC form the receiver (RX), while DAC, Filter, Mixer and Power Amplifier (PA) the transmitter (TX).

The power consumed by a wireless radio can be straightforwardly minimized by either reducing the consumption while on active mode; or also by decreasing the average power consumed through the implementation of a duty-cycle technique. With duty-cycling, the radio remains *on* only when necessary, and the remaining time it stays in sleep mode, exemplified in Figure 2.2.

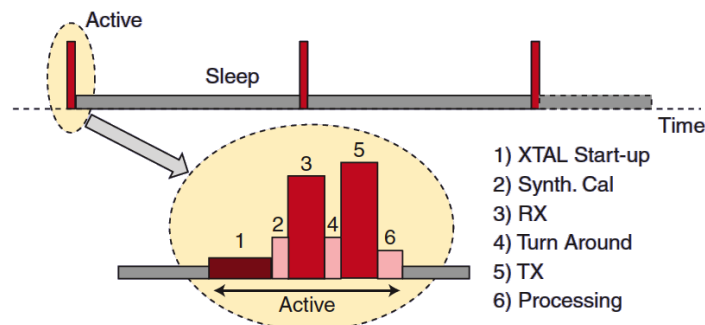


Figure 2.2: Duty Cycle-Technique (BURDETT, 2015).

The next sections will cover an overview of both the wireless communication standard and its requirements, as well as the receiver architecture and specifications for the low power wireless system in which this project is inserted. Since the ADC is the last block in the receiver

chain, its specification is determined by the RF front-end characteristics and the communication standard requirements.

2.1 The IEEE 802.11ah Standard

The IEEE 802.11 standard, which is the baseline for internet Wi-Fi communication technology, defines the medium access control (MAC) and the physical (PHY) layer for implementation of a wireless local area network (WLAN). The release of a base version of the standard was in 1997, and since then it has evolved to support more cases that require higher throughput (PARK, 2015). In most amendments, the enhancements were focused on allowing higher data rates and improvement in performances for a small number of devices, but not for a large number of low data rate devices such as WSN and IoT applications.

Nowadays different standards fulfill these objectives, but the IoT market is expanding, and none of these standards has been established as a global answer (GAZIS, 2017). In this scenario, the IEEE 802.11ah Task Group was formed in 2010 to create an amendment addressing the demand for WSN and IoT purposes.

The IEEE 802.11ah solution, or Wi-Fi HaLow, defines its specification over a set of unlicensed sub-1GHz bands that are available in most territories, such as United States, Europe, and Japan. Although sub-1GHz bands are more limited regarding bandwidth availability, they are suitable for IoT applications which consists of a high number of low-rate, low-power, and long distance devices (ADAME et al., 2014), thus presenting all characteristics to support WSN. The carrier frequency of about 900 MHz allows long distance (up to 1 km) in a low-traffic band. A hierarchical identification structure enables a network up to 6,000 devices connected to an Access Point (AP). Low-power strategies and fast and short transmissions (approximately 100 bytes per data package) complete these features.

Since regulation of the sub-1GHz frequency spectrum varies between different regions, so does the operation range of IEEE 802.11ah. Operation in Europe, United States, Japan, and Brazil is possible in the frequency range between 863 MHz and 930 MHz. Five different channel bandwidths are supported, with 1 MHz and 2 MHz bandwidths mandatory and widely adopted. The standard employs eleven modulation coding schemes (MCS) (INSTITUTE, 2014), ten of which are equivalent to the modulation coding schemes in IEEE 802.11ac standard. A new version of the MCS0, with half the corresponding code rate, is introduced as MCS10 for improvement in robustness.

Table 2.1 gathers characteristics and requirements of the PHY layer for the 802.11ah

receiver (RX) design for the mandatory modulation coding schemes. All MCS require a maximum packet error rate (PER) of 10%, considering a package formed by 256 octets. The maximum RF input power level supported by the standard is -30 dBm for any modulation scheme.

2.2 Receiver Architecture and Specifications

Two primary RF receiver architectures are typically employed in radio systems design: homodyne and heterodyne. In the first case, the demodulated signal is down-converted to the base-band of the original modulated signal (near DC) and in the latter to a particular intermediary frequency (IF). In a *low-IF receiver*, the IF is typically up to three times the signal bandwidth.

Table 2.1: RX PHY layer characteristics for mandatory MCS

	MCS10	MCS0	MCS1	MCS2	Unit
Modulation	BPSK	BPSK	QPSK	QPSK	-
Code Rate	1/4	1/2	1/2	3/4	-
Data Rate (1 MHz-band)	0.150	0.300	0.600	0.900	Mpbs
Data Rate (2 MHz-band)	-	0.650	1.300	1.950	Mpbs
Sensitivity (1 MHz-band)	-98	-95	-92	-90	dBm
Sensitivity (2 MHz-band)	-	-92	-89	-87	dBm
Adjacent Channel Rejection	19	16	13	11	dB
Non-adjacent Channel Rejection	35	32	29	27	dB

The down-conversion can be done using only one mixer, which is called **direct-conversion architecture**, but it is not appropriate for a narrow band system because of the dominant impact of the flicker noise (also called $1/f$ noise) at low frequencies and because of the electromagnetic coupling (crosstalk) between the local oscillator (LO) and the RF input stage (CROLS; STEYAERT, 1998). The **heterodyne IF architecture** has many of the desired properties of the zero-IF architectures (or direct-conversion), but avoids the aforementioned issues (RAZAVI, 2011). Selection of a IF closer to the signal bandwidth, thus a low-IF, only one downconversion is necessary which allows low power, and is, thus, a more suitable for an on-chip 802.11ah system. Figure 2.3 represents the block diagram of the final receiver architecture.

The system IF is then defined based on the *corner frequency* of the technology process, to avoid significant flicker noise contribution. The corner frequency establishes the limit after which the MOSFET flicker noise is not predominant anymore, becoming lower than the thermal noise. The Complementary Metal-Oxide-Semiconductor (CMOS) technology process available for the receiver design, a 130nm CMOS process, presents a MOSFET corner noise frequency

around 2 MHz for moderate-strong inversion condition and, for that reason, the IF was chosen equal to 3 MHz, suitable for both 1 and 2 MHz mandatory bandwidths.

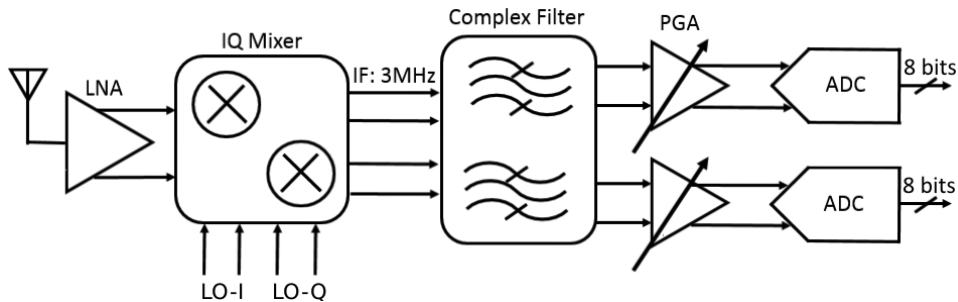


Figure 2.3: Receiver Architecture (ANDRADE et al., 2017).

The system level specifications of the IEEE 802.11ah Receiver are covered in detail in (ANDRADE et al., 2017). Specifications that are closely related to the A/D Converter design will be highlighted in the following paragraphs.

The receiver sensitivity is defined as the minimum signal power level that the receiver can detect with acceptable quality, which is the minimum signal-to-noise ratio (SNR) that the system can tolerate with an established error rate (RAZAVI, 2011). The relation between minimum SNR and error rate depends on the type of modulation, on the error correction mechanisms, and on the quality of the digital decoder system (TRAN et al., 2015). Thus system signal bandwidth, SNR and noise figure (NF) present limitations to the receiver sensitivity, which can be expressed as (RAZAVI, 2011):

$$P_{sen} = -174dBm/Hz + NF + 10\log f_B + SNR_{min} \quad (2.1)$$

Where P_{sen} is the sensitivity, NF is the receiver total noise figure, f_B is the signal bandwidth, SNR_{min} is the minimum required SNR and the term $-174dBm/Hz$ is the equivalent 300 K thermal noise of a 50Ω input impedance.

The worst case for NF is the minimum sensitivity required by MCS10 for a 1-MHz bandwidth, according to equation (2.1). The minimum SNR needed is defined taking into consideration the maximum PER mentioned previously and was estimated from simulation results as around 5 dB (ANDRADE et al., 2017) and corroborated with results found in (TRAN et al., 2015). For such a signal quality, NF should then be less than 11 dB. With an implementation margin of 2 dB, the receiver total noise figure resulted in 9 dB.

Considering the minimum and maximum input level for the 802.11ah standard -98 dBm (MCS10) and -30 dBm, respectively, the dynamic range of the receiver is 68 dB. The gain control is necessary to narrow the input signal variations at the A/D Converter input and relax its

resolution specification. This control is mainly performed by the programmable gain amplifier (PGA), but also by the low noise amplifier (LNA). The ADC full scale (FS) was set to 1 V_{pp} for differential signals, which corresponds to 1 dBm for a 50Ω reference impedance.

A 3-bit control was chosen for the PGA and 1-bit control for the LNA, leading to a 8.5 dB step size with eight steps, represented in Figure 2.4. By changing the receiver gain according to the input level, noise and linearity requirements can be better adjusted for each level, defining eight gain modes.

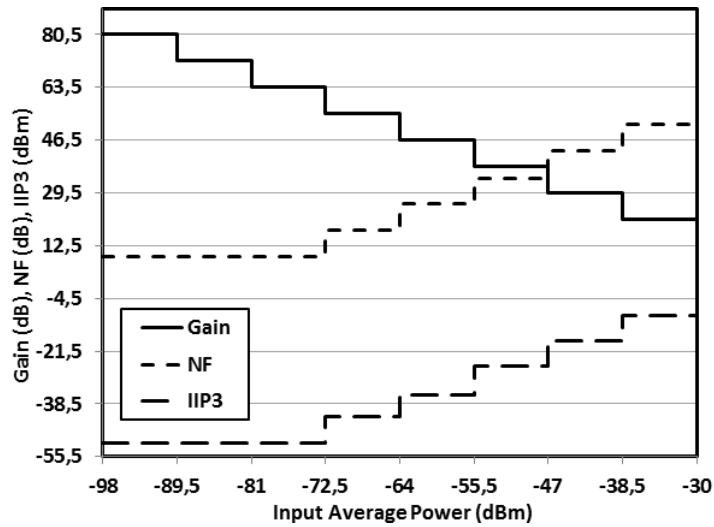


Figure 2.4: Receiver specifications for 8 different gain modes (ANDRADE et al., 2017).

The ADC resolution was chosen based on the worst case SNR degradation. The acceptable degradation caused by the analog-to-digital conversion should be lower than 0.5 dB for an input SNR of 8.5 dB. Considering that an effective number of bits of 7 leads to a signal degradation of 0.42 dB, a resolution of 8 bits was established for the ADC with 1 bit for implementation error margin.

Table 2.2 summarizes the IEEE 802.11ah receiver specifications.

Table 2.2: Receiver Specifications Summary (ANDRADE et al., 2017).

RX Spec	Min	Typ	Max	Unit
Intermediary Frequency	-	3	-	MHz
Gain	21	-	80.5	dB
Noise Figure	9	-	-	dB
Ip1dB	-41	-	-	dBm
IIP2	0	-	-	dBm
IIP3	-51	-	-	dBm
I/Q Amplitude Mismatch	-	-	0.07	dB
I/Q Phase Mismatch	-	-	0.45	°
Filter Order	6	-	-	-
PGA Step Size	-	8.5	-	dB
ADC Resolution	7	8	-	bits

2.2.1 A/D Converter Specifications

One of the fundamental specifications of an ADC is its resolution. As mentioned previously, the A/D converter resolution was set to 8 bits considering an SNR degradation of less than 0.5 dB, and the dynamic range of 8.5 dB established by the PGA that precedes the ADC.

The sampling rate can also be derived from the receiver specifications. During a sampling procedure, the original signal with bandwidth f_B is replicated at each multiple of the sampling frequency f_S . As illustrated in Figure 2.5, if a signal is sampled at $f_S < 2 * f_B$, it cannot be appropriately reconstructed by filtering. This limitation during the sampling of signals is known as the Nyquist-Shannon Sampling Theorem (or simply Nyquist Theorem). Since the IF is 3 MHz, and the maximum mandatory bandwidth is of 2 MHz, the higher limit of f_B is 4 MHz. The signal bandwidth defines a lower limit to the sampling frequency, which must be higher than 8 MHz. Thus, as an initial value, it was set to 10 MHz.

The role of the PGA includes not only the dynamic range definition but also the filtering process. The sampling frequency of the ADC should also account for the frequency planning of this filtering stage, as well as the stabilization time necessary of the gain control. At this stage of the project, the precise specifications of the filter are not yet defined, thus this sampling frequency may change as the project evolves.

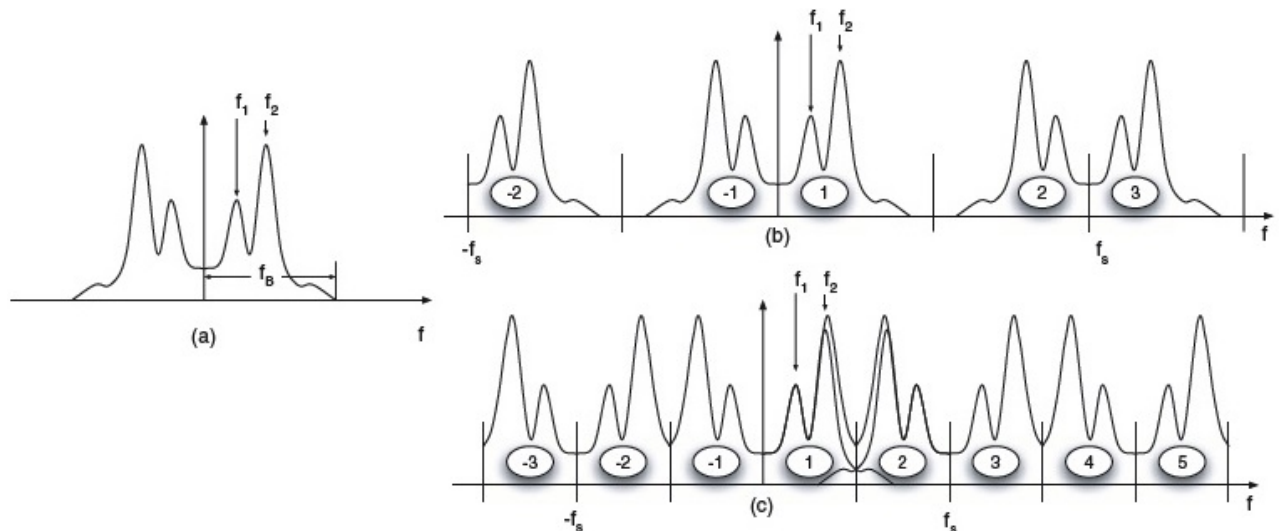


Figure 2.5: Illustration of the Nyquist Theorem: (a) a signal with bandwidth f_B ; (b) the signal sampled at $f_S > 2 * f_B$ and (c) at $f_S < 2 * f_B$, with the presence of aliasing (MALOBERTI, 2010).

The Global Foundries 130 nm CMOS technology selected typically employs supply voltages of either 1.2 V or 1.0 V. In this project, the latter was chosen. The ADC full scale was set initially to 1 Vpp for differential signals (0.5 V for both single inputs). Although a

larger signal swing could improve power efficiency of the ADC, from a system point of view, a smaller swing is more practical (HARPE et al., 2011). The ADC in question is preceded by an IF amplifier, which will benefit greatly from a shorter signal swing regarding gain and linearity. For that reason likewise, the FS was set to half the available range for the ADC considering the 1-V supply voltage, centered at middle range.

The preliminary ADC specifications are summarized in Table 2.3.

Table 2.3: Analog to Digital Converter Specifications

Resolution	n	8	bits
Supply Voltage	V_{DD}	1	V
Sampling Frequency	f_S	10	MHz
Signal Bandwidth	f_B	4	MHz
Full Scale (diff.)	FS	1	V

3 ANALOG TO DIGITAL CONVERSION

The transfer of information between analog and digital domains is the fundamental function of a data converter, allowing interaction of the digital abstract world with the real analog world. Many have said the converter acts as a *bridge* or *doorway* between these two domains. Over the decades, this doorway has often been a critical bottleneck in determining how much signal information can move between analog and digital worlds (ROBERTSON, 2015).

Signal bandwidth and dynamic range are considered primary dimensions when talking about data converters. As mentioned previously, they are directly related to sample rate, f_S , and to resolution, n , of a converter. Advances in technology may be traced as an advance in these two dimensions: greater f_S allow converters with greater bandwidths and higher resolutions provide more dynamic range and thus the ability to handle more signal information.

The analog-to-digital conversion process involves both the **sampling** function, translating the signal from continuous time to discrete time, and the **quantization** function, which corresponds to discretization regarding amplitude. Discretization procedures, both in time and in amplitude, inevitably introduce a rounding error, even in a theoretically perfect converter. The Nyquist theorem establishes a limitation to the maximum signal bandwidth that can be unambiguously represented in a sampling procedure, thus avoiding *aliasing*. The quantization process produces errors which include clipping signals that exceed the full scale and the *quantization noise* that forms a sensitivity floor.

3.1 ADC Basics

3.1.1 Sampling

Mathematically, sampling is performed by multiplying the time-continuous function $A(t)$ of Figure 3.1.(a) with a sequence of Dirac-pulses, resulting in a time discrete signal of Figure 3.1.(b) (PELGROM, 2010). The frequency domain representation of $A(t)$ is exemplified by $A(w)$ in Figure 3.1.(c), and after sampling, in Figure 3.1.(d). In the time domain, the sampling results in the original signal $A(t)$ defined at each sampling period T_S ($f_S = 1/T_S$) as for the frequency domain, results in replicas of the original signal $A(w)$ spectrum at multiples of the sampling rate f_S . A direct consequence of sampling is that, to correctly reconstruct the original signal afterwards, the sample rate f_S should be at least $2 * f_B$ (Nyquist theorem) to avoid aliasing.

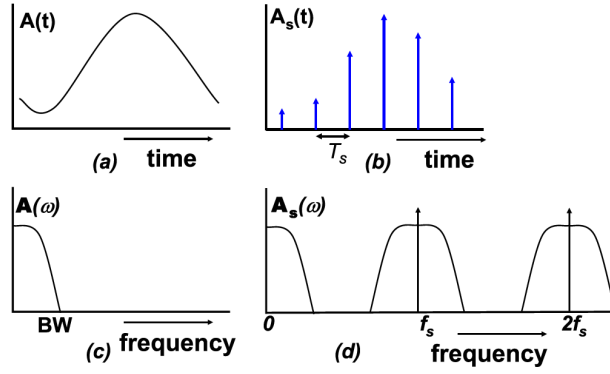


Figure 3.1: (a) Time domain signal $A(t)$ (b) and its sampled version. (c) Frequency domain signal $A(w)$ (d) and its sampled version.(PELGROM, 2010).

An equivalent schematic of a basic sampling circuit is shown in Figure 3.2. It consists of a storage capacitor and a switch, which is modeled as a resistance impaired with thermal noise (in real circuits every switch presents finite resistance and every element with resistivity generates thermal noise). A low pass filter is formed when the switch is on, thus the average noise energy is a filtered version of the noise energy supplied by the resistor, and represented by:

$$v_{C,noise} = \sqrt{\frac{kT}{C}} \quad (3.1)$$

with Boltzmann's constant $k = 1.38 \times 10^{-23} (m^2.kg)/(s^2.K)$ and the absolute temperature T in Kelvin. The simple and well-known expression of the sampled noise on a capacitor is the kT/C -noise, which represents a lower boundary for the sampling capacitor value when a certain resolution is targeted.

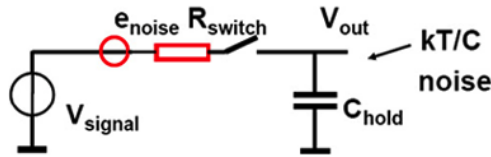


Figure 3.2: Equivalent schematic of basic sampling circuit. (PELGROM, 2010).

3.1.2 Quantization

In A/D Converters, the quantization process is performed after sampling. The quantization process corresponds to discretization of the sampled-signal from a continuous-level to discrete-level. The converter dynamic range is divided into equally-spaced quantized levels, each represented by an analog amplitude.

Since digital representation is done in binary numbers, the number of quantization levels is usually a power of 2, 2^N , and N (or n) is the converter resolution or number of bits. The N^{th} bit is called *Most Significant Bit* (MSB), and the 1^{st} bit, *Least Significant Bit* (LSB), both illustrated in Figure 3.3. The *Full Scale* (FS) of the converter corresponds to the available analog dynamic range, $V_{refp} - V_{refn}$ (typically $V_{refn} = 0$), thus the amplitude of each quantization step is given by:

$$A_{LSB} = \frac{FS}{2^N} \quad (3.2)$$

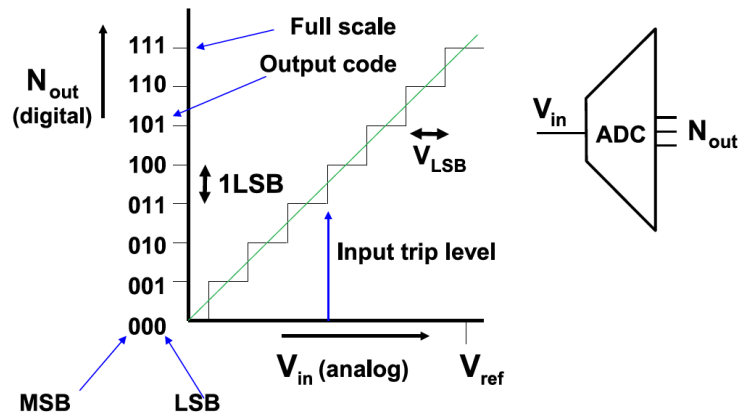


Figure 3.3: Definition of A/D Conversion Parameters. (PELGROM, 2010).

The unavoidable rounding error generated during quantization is known as *quantization error* in time domain or *quantization noise* in frequency domain. The power associated with this error is a fundamental limit to the analog-to-digital converter performance, which can be approximated to (MALOBERTI, 2010):

$$P_{Quant} = \frac{A_{LSB}^2}{12} = \left(\frac{FS}{2^N \sqrt{12}} \right)^2 \quad (3.3)$$

The quantization error is often considered as a noise contributor when it is, in fact, a non-linear phenomena, which generates distortion. With a resolution of $N = 1$ bit, the conversion of a sinusoidal wave will result in a square wave, which can otherwise be represented as a Fourier Series. Each term of the Fourier series represents the harmonics and its respective power contributions. Intuitively, the higher the resolution, the more accurate the representation of the original sine wave, and the smaller the contribution of each harmonic.

More precisely, for a sufficiently large signal with a frequency uncorrelated with f_s , the distortion products that fold with sample rate multiples allow a statistical approximation of the error signal generated in the quantization process. This deterministic error signal after sampling is approximated as white noise in the band from 0 to $f_s/2$ and mirrored to the higher bands. (PELGROM, 2010).

3.1.3 Dynamic Metrics

In the frequency domain, converters dynamic performance is characterized by the power ratios *signal-to-noise ratio* (SNR), *signal-to-noise-and-distortion ratio* (SNDR or SINAD), *total harmonic distortion* (THD), *spurious free dynamic range* (SFDR), among other metrics. Figure 3.4 shows some of these dynamic metrics.

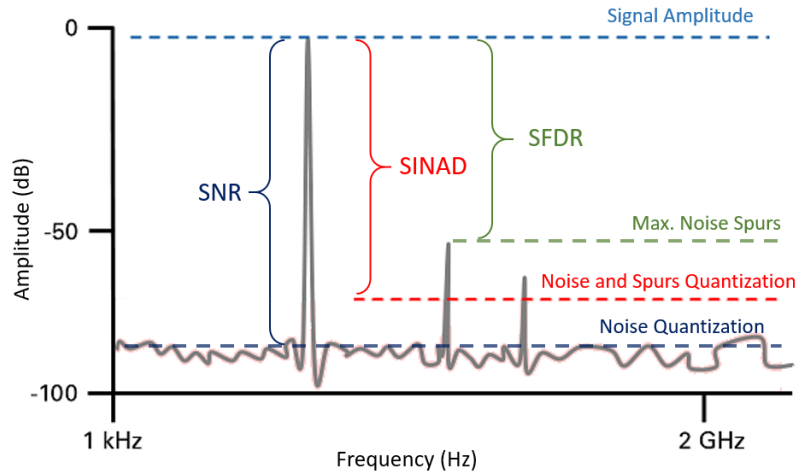


Figure 3.4: Common dynamic metrics: SNR, SINAD and SFDR.

In A/D Converters, sinusoidal signals are used to characterize the performance. Considering the signal power in terms of A_{LSB} as $(2^{2N} A_{LSB}^2)/8$ and the quantization power of equation (3.3), the SNR is given by equation (3.4). The SNDR estimate considers all unwanted components, not only the quantization noise but also thermal noise, distortion, etc.

$$SNR = \left(\frac{P_{Sig}}{P_{Quant}} \right) = \frac{3}{2} 2^{2N} \Rightarrow SNR_{dB} = 1.76 + 6.02 \times N \quad (3.4)$$

$$SNDR_{dB} = 10 \log_{10} \left(\frac{P_{Sig}}{P_{Quant} + P_h} \right) \quad (3.5)$$

where P_{Sig} is the power of a pure sine-wave signal, P_{Quant} is the quantization power and P_h is the power of the harmonics except the fundamental.

The expression for ENOB of equation (1.1) merely is a SINAD version of equation (3.4) with the number of bits N isolated.

Linearity deviations in the frequency domain are represented by the THD:

$$THD_{dB} = 10 \log_{10} \left(\frac{P_h}{P_{Sig}} \right) \quad (3.6)$$

3.1.4 Static Metrics

The ideal staircase of Figure 3.5 and its steps can deviate from the ideal in different ways, that can be quantified in terms of *offset error*, *gain error*, *integral nonlinearity* (INL) and *differential nonlinearity* (DNL). Offset and gain errors can be understood straightforwardly, as they portray a shift and a slope deviation of the staircase from its ideal position, respectively. Neither introduces harmonics and typically are easy to compensate. On the other hand, INL and DNL introduce distortion which degrades further the output signal, as the frequency increases.

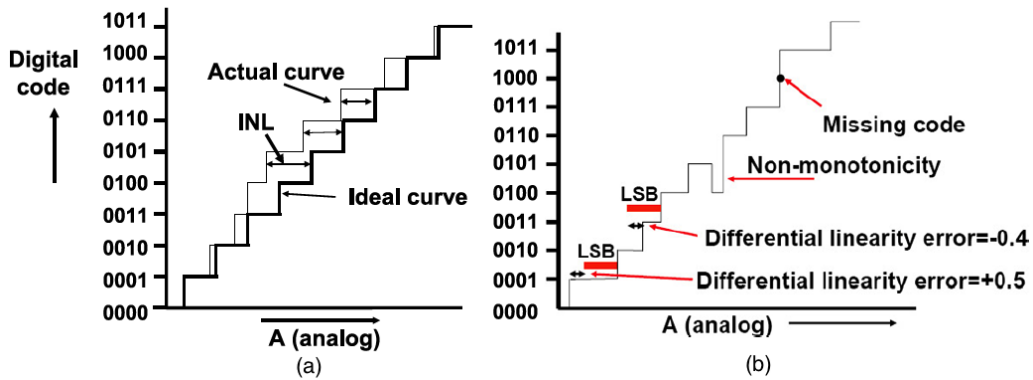


Figure 3.5: (a) Definition of INL and (b) DNL (PELGROM, 2010).

The integral nonlinearity represents the maximum deviation of the converter response from the ideal conversion function. As for the differential nonlinearity, it represents the deviation of each step with respect to the ideal LSB size. INL and DNL are represented in equations 3.7 and 3.8. An absolute DNL greater than 1 LSB represents a *missing code* ($DNL < -1$ LSB or $DNL > +1$ LSB) (PELGROM, 2010).

$$INL = \frac{A(i) - i \times A_{LSB}}{A_{LSB}} \quad \forall i = 0 \dots (2^N - 1) \quad (3.7)$$

$$DNL = \frac{A(i+1) - A(i)}{A_{LSB}} - 1 \quad \forall i = 0 \dots (2^N - 2) \quad (3.8)$$

3.2 Categories of A/D Converters

The converters can be divided in two great categories: *nyquist* and *oversampled* converters. They differ on the relationship between f_S and f_B . For the Nyquist converters, most of the available bandwidth, from DC to $f_S/2$, is employed and they often operate at speed limit. On the oversampled converters, f_S is larger than the sample rate that fulfills the Nyquist criteria which

consequently reduces the noise contribution on the signal bandwidth, due to uniform spreading of noise throughout the greater 0 to $f_s/2$ band.

Converters that operate on a *parallel*, *sequential* or *linear* search are Nyquist Converters, such as Flash, as successive approximation converters (SAR) and Pipeline, and as "dual-slope" converters, respectively. The Sigma-Delta converter is the most common Oversampled Converter employed. Figure 3.6 illustrates the categories of conversions stated above.

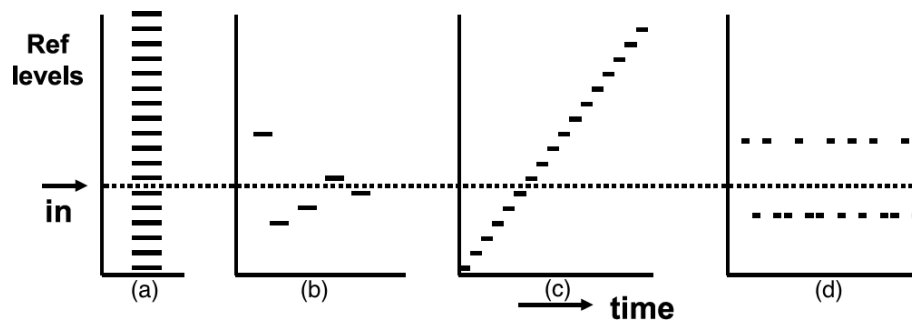


Figure 3.6: Types of AD conversion principles. (a) On the parallel search, all the reference levels are available at the same time; (b) on the sequential search, the next reference level is defined based on the previous result; (c) on the linear search, each reference level is available at consecutive clocks; (d) on the oversampled type, on which on a few levels are available throughout the conversion (PELGROM, 2010).

On the **parallel search**, the input signal and all the reference levels are available at the same time. Only one clock cycle is necessary for the conversion, and it is typically the converter with the highest speed. The required hardware, on the other hand, is very extensive and matching issues have a significant impact on the final result.

On the **sequential search**, the conversion process sets a new reference level at each clock cycle narrowing down the difference between input signal and the analog estimate. The SAR converter is a type of sequential search converter which employs a single stage and circulates it over multiple clock cycles while the analog input is frozen (RAZAVI, 2015b). The Pipeline converter is also a type of sequential search converter that uses a concurrent operation with multiple hardware stages needing only one clock cycle for the conversion process between consecutive samples (after the acquisition of the first sample).

On the **linear search**, the reference levels are generated in increasing or decreasing order and compared to the input signal. The conversion process is very slow, but requires a minimum amount of hardware.

On the converters that use the **oversampling process**, a time average approximation of the input is created using only one or a few reference levels, around which the analog estimate switches. The most usual case is the use of only one reference level (one bit quantization), as

can be seen in sigma-delta-converters, being their accuracy (or resolution) a result of the large amount of samples acquired in the time domain.

3.2.1 Why SAR?

Selection of the appropriate A/D converter architecture depends heavily on the demands of the application it will take part (ROBERTSON, 2015). The following assortment will consider resolution and sample rates as metrics.

Audio applications must account that human ears are sensitive to nonlinearity issues, thus making a high resolution a necessity. Together with the fact that audio bandwidth is relatively mild, up to 20 kHz, makes this field of application practical for oversampling converters, specially sigma-delta converters.

Imaging applications, which include not only consumer usage, but also industrial and healthcare imaging, must consider a high resolution for the *pixel stream* and high frame rates. This combination makes the pipeline converters an ideal architecture.

For applications in the **Communications** environment, three main categories will be outlined: mobile and handset devices, instrumentation and optical applications, and wireless sensor networks (WSN).

On the first group, the evolution of cellular standards pushed data rates to higher levels, combined with tight power budgets. On that scenario, continuous-time sigma-delta became the desired solution, for combining both data conversion in filtering in the same structure.

As for optical applications, ultrahigh speed is of essence. In the past, flash converters were the primary solution, yet nowadays, interleaved and hybrid structures have become the answer. Advances in technology process, which enabled an increase in integration density possible in silicon, reinforced this trend.

In the WSN field, the SAR A/D converter became the best candidate, due to its power efficiency in medium resolutions and bandwidths space, and its tendency to scale well with process technologies.

The SAR architecture continues to be actively researched, and its applications go beyond the WSN applications, including also implantable biomedical devices field, and as part of the recent trend on hybrid-interleaved converters. The chart of Figure 3.7 indicates the growth of investigation of SAR converters.

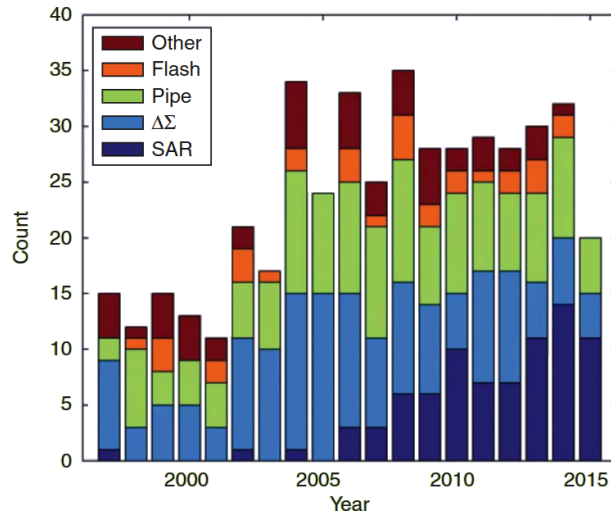


Figure 3.7: Architectures of ADCs described in the literature (MURMANN, 2015).

3.3 SAR Basic Operation

The SAR ADC is one of the oldest and best-known ADC architectures. Initially called *feedback subtraction ADC*, the basic algorithm of a SAR ADC conversion process can be traced back to 1500s (KESTER, 2015), relating to a mathematical puzzle illustrated in Figure 3.8.(a). The conversion algorithm of a SAR A/D Converter employs a binary search to converge to the closest analog estimate of the input voltage, shown in Figure 3.8.(b), much like the mathematical puzzle.

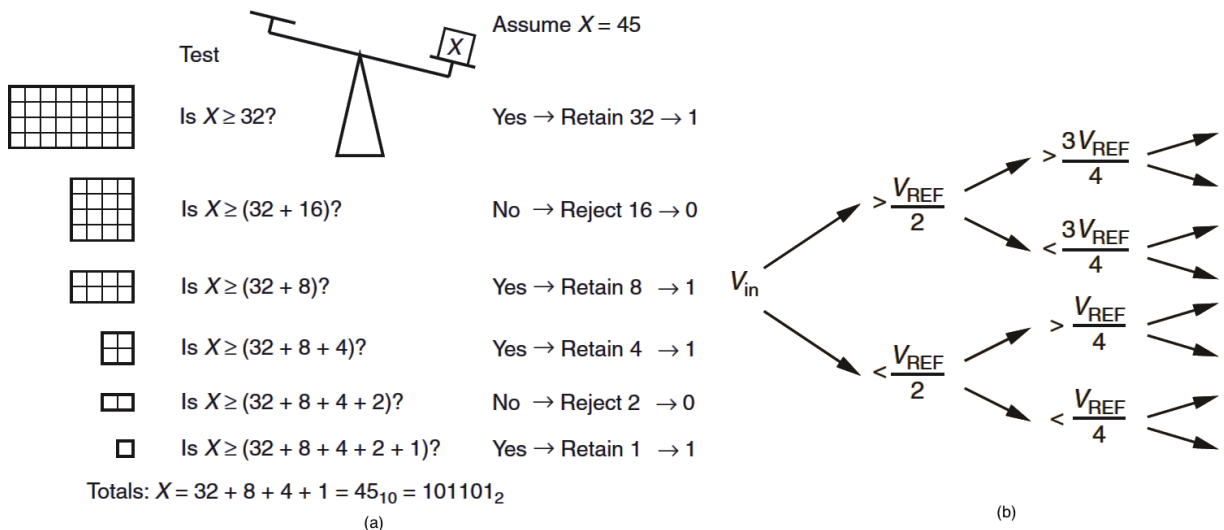


Figure 3.8: (a) Illustration of mathematical puzzle in which an unknown weight is estimated following a sequence of weighting operations. (KESTER, 2015), and (b) the binary search computation.

Depicted in Figure 3.9.(a), the basic SAR architecture consists of a sampling switch, a comparator, the SAR logic, and a DAC in a negative feedback loop. The basic function

consists of comparing the sampled input V_{in} , at each clock cycle, to successive reference values generated based on the previous comparator response and set by the SAR logic combined with the DAC. The reference values converge progressively to a point where the comparator input difference, that is, $V_{DAC} - V_{samp}$, falls under 1 LSB. Typically, after sampling the input, the converter needs N cycles of the SAR algorithm to resolve a N -bit conversion. Thus, an internal clock f_{clk} is usually $N + 1$ higher than the sampling frequency f_s .

Many physical quantities could be used in the feedback DAC to represent the analog value: voltage, current, charge or time. The most usual nowadays is the **Charge Redistribution** strategy, as shown on Figure 3.9.(b). It consists of binary-weighted capacitors in parallel, which are switched between positive and negative reference values, V_{refp} and V_{refn} (typically ground), respectively, based on the comparator response. With this type of topology, the capacitor array also serves as sampling capacitor C_S , making an additional sample-and-hold capacitor for that purpose unnecessary.

The SAR ADC has mainly a digital-like and opamp-free architecture, thus making it very power efficient, consuming mostly dynamic power. Furthermore, due also to their switched-capacitor implementation, SAR A/D converters benefit from technology downscaling making low-voltage operation feasible and reducing conversion time (FATEH et al., 2015; LIN; HSIEH, 2015; ZHU; LIANG, 2015; RABUSKE; FERNANDES, 2016).

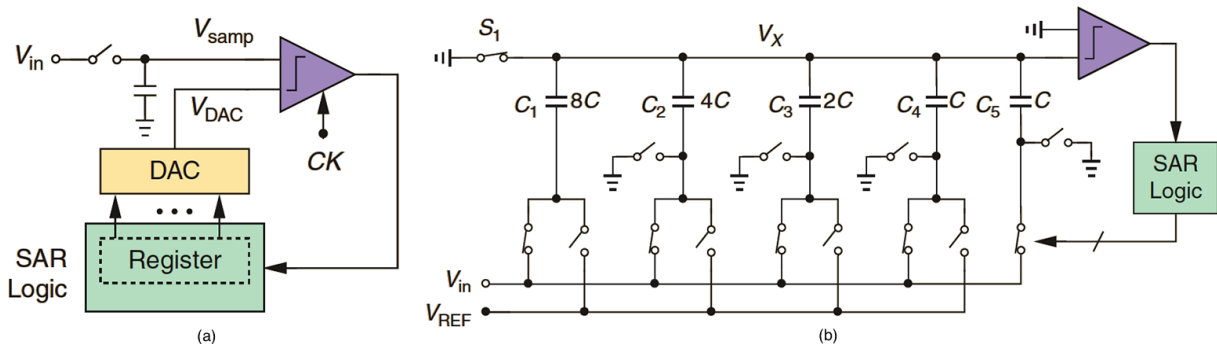


Figure 3.9: (a) The basic SAR ADC architecture and (b) the commonly employed charge redistribution topology (RAZAVI, 2015b).

3.3.1 Limiting factors

The trade-offs of a converter design include requirements of speed, noise, linearity, area, and power consumption.

While simple and efficient, the SAR ADC is not a fast architecture and is often not suitable for high sample rates, since it requires multiple clock cycles for the conversion to end.

One clock cycle must be as long as to include the comparator response time (t_{comp}), the SAR logic delay (t_{SAR}) and the settling of the switch-capacitors DAC (t_{DAC}).

The comparator, sampling switch and DAC's noise, along with quantization noise, are the primary noise contributors on A/D converter design. The impact of quantization noise when compared to other contributors varies directly with the desired ADC resolution, as explored further previously.

When looking into linearity issues, gain and offset errors of the internal blocks often translate to ADC gain and offset errors, which do not cause distortion. For high precision applications, however, both errors can have a significant impact, and in those cases, they must not be ignored. Linear errors of the SAR ADC mainly come from the sampling switch distortion and mismatch on the DAC capacitors. In this sense, the output of both blocks must be as accurate as the ADC's desired digital conversion, one LSB. Hence a N-bit ADC design requires 2^N unit capacitors on the DAC array to provide the same accuracy.

Furthermore, the high amount of unit capacitors impacts directly on the occupied area. Ultimately, for higher resolutions, the DAC occupies a significant portion of the ADC area.

Power consumption primarily lies in the analog capacitive DAC network and dynamic comparator, and in the digital SAR logic. The power of analog and digital circuits scales differently with the resolution of the converter. In digital circuits, it tends to scale linearly with an increase in resolution. As for analog circuits, fundamentally, for each 1-bit increment, power consumption tends to scale by a factor of four (HARPE, 2016).

3.4 Bibliographic Review

Like any other analog design, improvements in either of those requirements explored in the last paragraphs have a direct effect in one or more of the remaining specifications. For instance, scaling up the dimensions of capacitors on the DAC array can improve matching and noise requirements as well as area, but most likely it will have a negative impact on power consumption and speed. Hence, what researchers and their investigations aim is the improvement of a some of the requirements, while maintaining the others within an acceptable range.

Several strategies continue to be topic of research for reduction of power consumption in the last decade, especially in the last few years after the popularity of IoT and WSN. These strategies can focus either on a block level or a system-level improvement. Typically, the capacitive DAC and SAR control logic are the power-hungry blocks in a SAR ADC, and a great variety of switching schemes have been published recently as improvements of the conventional

switching sequence.

On the **Conventional** scheme (GINSBURG; CHANDRAKASAN, 2005), at the sampling phase, the input signal is sampled at the bottom plate of the capacitors, with its top plate connected to $V_{cm} = (V_{refp} + V_{refn})/2$. At each cycle N , C_N from both arrays of a differential topology are connected to V_{refp} , connecting the remaining to V_{refn} . Depending on the result of the comparison, the logic switches C_N to V_{refn} or maintains connected to V_{refp} . It is a trial-and-error method that consumes unnecessary power.

On the **Monotonic** switching scheme (LIU et al., 2010), sampling is done at the top plate of the capacitors while bottom plates are connected to V_{refp} (or V_{refn}). Unlike the conventional scheme, only one of the DAC arrays switches at each cycle, connecting the capacitors to V_{refn} (or V_{refp}), which comparatively accounts for energy saving of 81%.

In contrast, the **Vcm-based** switching method (ZHU et al., 2010) samples the input at the top plates of the capacitor while connecting the bottom plates to V_{cm} . At each cycle, both arrays are switched, one to V_{refp} and the V_{refn} , leading to half the voltage shift for each capacitor, which reduces switching energy by 87% when compared to the conventional scheme. The V_{cm} -based method is less power hungry when compared to the respective bit in the monotonic scheme. In contrast, it requires a third reference level, which are potential sources of distortion and noise, and represents additional circuitry.

The work of (LIN; TANG, 2013) presents a novel **Tri-Level** switching scheme which also employs the dummy capacitor on the logic. On the **Charge Average** procedure explored in (LIOU; HSIEH, 2013) connection between bottom plates of capacitors of both arrays generates the necessary voltage shift at each cycle. On the **Merge-and-Split** switching scheme of (LIN; HSIEH, 2015), this connection between bottom plates is performed at sampling, and splitting may occur or not based on the comparator results. The work of (ZHU; LIANG, 2015) presents a novel switching scheme based on the one-side switching instead (OSSI) and higher-bit switching instead (HBSI) methods. On the **Charge Average, Merge-and-Split** and **OSSI-HBSI**, reset energy is very significant, as depicted on Table 3.1. On (LIU; SHEN; ZHU, 2016), researches developed an improved version of the OSSI-HBSI (**New OSSI-HBSI**), in which the reset energy is zero.

Another strategy to decrease power consumption is to reduce the number of steps necessary for the conversion, by resolving more than 1 bit per cycle (JIN; GAO; SÁNCHEZ-SINENCIO, 2014; SHEN et al., 2018b) or skipping some bits altogether. On (CHENG; TANG, 2015), if the difference between positive and negative inputs is within a specified range, some bits are skipped. The work of (YAUL; CHANDRAKASAN, 2014) presents an LSB-first esti-

mation method, with conversion progressively moving toward the MSB and requiring between 2 and $2N+1$ cycles to resolve an N -bit resolution. On (SONG et al., 2016) implementation of a judge window allows skipping of some cycles, by comparison of two consecutive samples. For the LSB-first method, input signals close to the dc level demonstrates high efficiency; as for the judge-window method, efficiency occurs when the difference between samples is within a predefined range.

Table 3.1: Comparison of DAC Switching Techniques

Switching Procedure	Ref.	Switching Energy (CV_{Ref}^2)	Reset Energy (CV_{Ref}^2)	Reduction of Switching Energy (%)	Reduction of Conversion Energy (%)
Conventional	ISCAS'15	1363.3	0	reference	reference
Monotonic	JSSC'10	255.5	0	81	81
Vcm-based	JSSC'10	170.2	0	87.5	87.5
Tri-Level	ISCAS'13	70.9	- ¹	94.8	94.8 ¹
Charge Average	ISSCC'13	88.6	255.5	93.5	74.8
Merge-Split	TCAS'15	-21.6	255.5	-	82.8
OSSI-HBSI	TCAS'15	15.8	31.2	98.9	96.6
New-OSSI-HBSI	TCAS'16	26.54	0	98.1	98.1

¹ The reset energy was not explicitly informed.

Although more popular, charge redistribution is not the only topology researched. Charge-sharing SARs are a topic of recent investigation (TSAI et al., 2014; RABUSKE; FERNANDES, 2016). An advantageous fact is that the reference is only sampled at the start of conversion, which makes this topology immune to inaccuracies from the references. In contrast, they are more sensitive to noise and comparator offset (RABUSKE; FERNANDES, 2016). Hybrid structures that employ time-domain comparators were also a topic of interest recently assuming that, with time domain information, both reduction in conversion cycles and power consumption is achievable (CHEN; CHANG; HSIEH, 2016). Additionally, the work of (JIN; GAO; SÁNCHEZ-SINENCIO, 2014) demonstrates a resistive-based DAC, and that of (CHEN; CHANG; HSIEH, 2016) presents a hybrid ADC, in which part of the conversion is performed at the time domain.

Another form of power reduction is by implementing reconfigurable SARs, allowing variations on resolution and sample rate (HUANG et al., 2013), or power scalable SARs (ZHU et al., 2015). Such structures enable saving of energy when employed under conditions in which the input signal levels and frequency may vary with time, and they can be adjusted accordingly.

Power efficiency and speed are often two performances interrelated that by improving one improves the other. In particular, asynchronous architectures are an attractive method found in several works (LIN; TANG, 2013; LIN; HSIEH, 2015; SONG et al., 2016; JIN; GAO; SÁNCHEZ-SINENCIO, 2014; RABUSKE; FERNANDES, 2016; LIU; SHEN; ZHU, 2016;

SHEN et al., 2018b). The asynchronous strategy corresponds to a duty-cycling technique that uses to its advantage the different comparator delays (t_{comp}) that result from the different input signals (HARPE, 2016). Power can be saved by turning off the comparator after a valid result. Still, when only speed is essential and higher sampling rates are the goal, hybrid structures employing ADCs that have better speed performance, such as a flash (SHEN et al., 2018a) or pipeline (ZHANG et al., 2017), become interesting solutions. Another possibility is the implementation of time-interleaved structures like in (SHEN et al., 2018b).

As for linearity issues, implementation of a bootstrapped sampling switch (FATEH et al., 2015; SONG et al., 2016; ZHANG; BONIZZONI; MALOBERTI, 2016; ZHU; LIANG, 2015) not only reduces the dependency with the input signal but also shortens the charge injection effect by fixating the signal that activates the switch (RAZAVI, 2015a). Variations of the boosting switches were also investigated, with complementary design (CHENG; TANG, 2015), bulk biasing (SHEN et al., 2018b), double boosting for low voltage applications (LIOU; HSIEH, 2013; CHEN; CHANG; HSIEH, 2016).

To minimize the effect of capacitor mismatch, some approaches optimized the unit capacitor (ZHANG; BONIZZONI; MALOBERTI, 2016; LIN; HSIEH, 2015; HARPE; CANTATORE; ROERMUND, 2013), also improving the noise performance. Others added redundancy with augmentation of the number of steps by implementing a sub-radix-2 design (FATEH et al., 2015), in which a 14-bit conversion requires 17 cycles.

Nevertheless, the most common strategy is through calibration techniques (DING et al., 2017; SHEN et al., 2018a; HA et al., 2014; FATEH et al., 2015), which also increases the number of steps. The addition of trimming capacitors for gain and offset error corrections are part of the work of (TAO; LIAN, 2015). On (CHUNG, 2013), a calibration technique is implemented on the DAC split array, by performing sampling twice with a swap of roles for the MSB and LSB arrays. Swapping also occurs on (HA et al., 2014), but differently, sampling is performed only once, along with an error compensation technique that checks whether the difference in DAC outputs is smaller than 1 LSB.

Offset cancellation techniques on the comparator were explored in (LIU; SHEN; ZHU, 2016; CHEN; CHANG; HSIEH, 2016), as well as auto-zeroing techniques on the comparator preamplifier (TAO; LIAN, 2015). A two-mode comparator design is demonstrated in (DING et al., 2017), with the LSB estimation in both modes. If the result is different, a dynamic offset will be detected enabling the comparator correction circuit.

Typically, the calibration schemes are responsible for improvements not only in linearity but also in noise performances. Besides the strategies mentioned, oversampling (HSU et al.,

2018) and data-driven noise reduction with majority-voting (HARPE; CANTATORE; ROERMUND, 2013) have also been topics of investigation on reducing noise. The work of (SHEN et al., 2018a) presents an LSB technique, in which the LSB can be estimated up to 10 times then averaged.

Finally, the DAC occupies most of the area, so the cutback on the number of unit elements is desired either by employing split-array (FATEH et al., 2015; HUANG et al., 2013; HA et al., 2014), or by resolving more than one bit per cycle (JIN; GAO; SÁNCHEZ-SINENCIO, 2014; SHEN et al., 2018b), or even by performing part of the conversion in the time-domain (CHEN; CHANG; HSIEH, 2016). Besides that, decreasing the dimensions of the unit element can also accomplish area reduction (HARPE et al., 2011; HARPE; CANTATORE; ROERMUND, 2013; ZHANG; BONIZZONI; MALOBERTI, 2016; LIN; HSIEH, 2015). Metal-oxide-semiconductor capacitors (MOSCAPs), which correspond to the gate-substrate capacitor of the MOS transistor, have largest capacitance density when compared to metal-oxide-metal (MOM) or metal-insulator-metal (MIM) capacitors. Therefore, implementing a DAC capacitor array with MOSCAPs can potentially reduce DAC area (RABUSKE; FERNANDES, 2016), at the cost of an increase in nonlinearity since MOSCAPs are intrinsically nonlinear. Last, but not least, a single topology uses only one DAC (TAO; LIAN, 2015), thus reduces occupied area and power, at the price of additional circuitry for common mode rejection.

It is of main interest for the radio specified in Chapter 2 a low power operation, that includes optimizing power consumption for every block, A/D Converter included. With that in mind, among the switching schemes presented in Table 3.1, the OSSI-HSBI method implemented (ZHU; LIANG, 2015) was studied more thoroughly due to the reduction of 96% conversion energy when compared to the conventional scheme. It is worth noting, at this stage, that at the start this project, the improvement of the OSSI-HSBI method had not yet been published.

The architecture developed on (ZHU; LIANG, 2015) contemplated a low voltage and low rate application, for medical implanted devices. With a supply voltage of 0.6 V and a sampling rate of 20 kS/s, the design achieved an ENOB of 9.4 and consumed 38 nW in CMOS 0.18 μm .

The switching scheme implemented is based on two methods: one-side switching instead (OSSI) and higher-bit switching instead (HBSI), illustrated in Figure 3.10. Although steps in Figures 3.10.(a) and (b) represent identical voltage shifts at the comparator input, the OSSI method causes no potential difference at the equivalent capacitance, thus consumes no energy. Likewise, steps in Figures 3.10.(c) and (d) represent identical voltage shifts at the comparator

input, yet on the HBSI method, a larger capacitance sees a smaller voltage shift, similarly to the vcm-based switching.

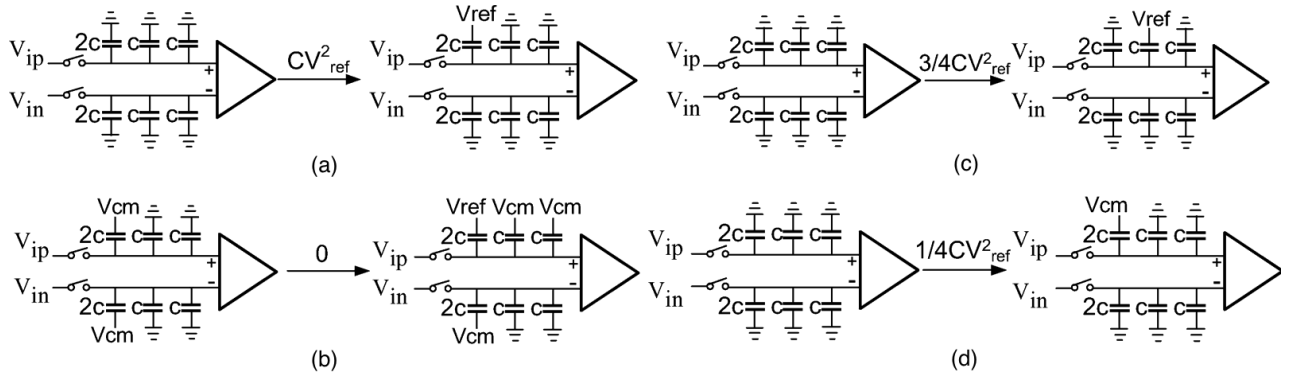


Figure 3.10: Switching methods: (a) traditional scheme for 1^{st} -switching and (b) the OSSI; (c) traditional scheme for 2^{nd} -switching and (d) the HBSI (ZHU; LIANG, 2015).

Several studies have focused on an asynchronous functioning, such as the one explored in (RABUSKE; FERNANDES, 2016). The SAR ADC architecture relies on the charge-sharing principle and differently from most works it uses only **MOSCAPS**, instead of the typical MOM or MIM capacitors. With a supply voltage of 0.6 V and a sampling rate of 20 MS/s, the design achieved an ENOB of 8.48 and consumed 2.78 μ W in CMOS 0.13 μ m.

The asynchronous logic is implemented according to Figure 3.11. The comparator self-timing feedback loop uses combinational logic to generate a *valid* signal that additionally controls the SAR logic. A controllable delay with *valid* signal as input then turns off the comparator.

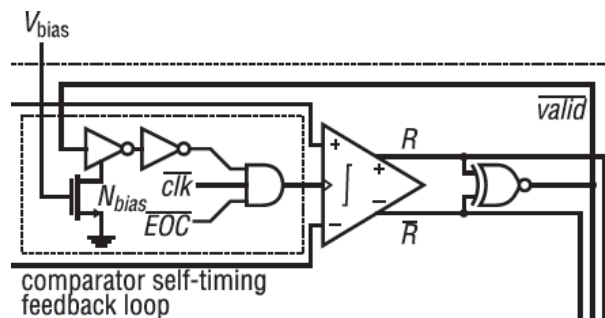


Figure 3.11: Asynchronous logic (RABUSKE; FERNANDES, 2016).

The differential topology, albeit its disadvantages concerning area and power consumption, provides more dynamic range than the single topology. Considering that, on the receiver chain the ADC will be preceded by a baseband amplifier, which will benefit from a smaller swing because of linearity and gain requirements (HARPE et al., 2011) (**Low Energy Radio** on Table 3.2), a larger dynamic range is of great importance.

Table 3.2 summarizes the performances of the works highlighted on Table 3.1, as well as those mentioned on the last paragraphs.

Table 3.2: Comparison of Performances

	Ref.	Tech. (nm)	VDD (V)	Power (μ W)	f_S (MS/s)	Resolution (bits)	ENOB ¹ (bits)	FoM (fJ/conv-step)
Tri-Level	ISCAS'13	90	0.5	3.87	1.28	10	9.69	3.66
Charge Average	ISSCC'13	90	0.7	11	4	10	9.05	5.2
Merge-Split	TCAS'15	90	0.5	1.8	2	10	8.97	1.78
OSSI-HBSI	TCAS'15	180	0.6	0.038	0.02	10	9.4	2.8
New-OSSI-HBSI	TCAS'16	180	1.8	820	10	12	10.82	44.2
MOSCAP	JSSC'16	130	0.6	2.78	1	9	8.48	7.8
Low Energy Radio	JSSC'11	90	1	26.3	10.24	8	7.77	12

¹ At Nyquist rate.

4 LOW POWER SAR ADC DESIGN

After discussing both the primary application of the A/D Converter and basics of converters as well as reviewing recent SAR ADC works on the previous chapters, from henceforth on the focus will be on presenting the A/D converter architecture and its implementation on circuit level.

4.1 SAR ADC Architecture

The architecture of the 8-bit successive approximation A/D converter is presented in Figure 4.1. It consists of two binary-weighted capacitive DAC, a low power comparator, the SAR digital logic, the asynchronous logic and two input bootstrapped switches. The differential topology allows suppression of voltage noise, reduction of parasitics impact and has good common-mode supply rejection, as well as provides a preferable increase in the dynamic range.

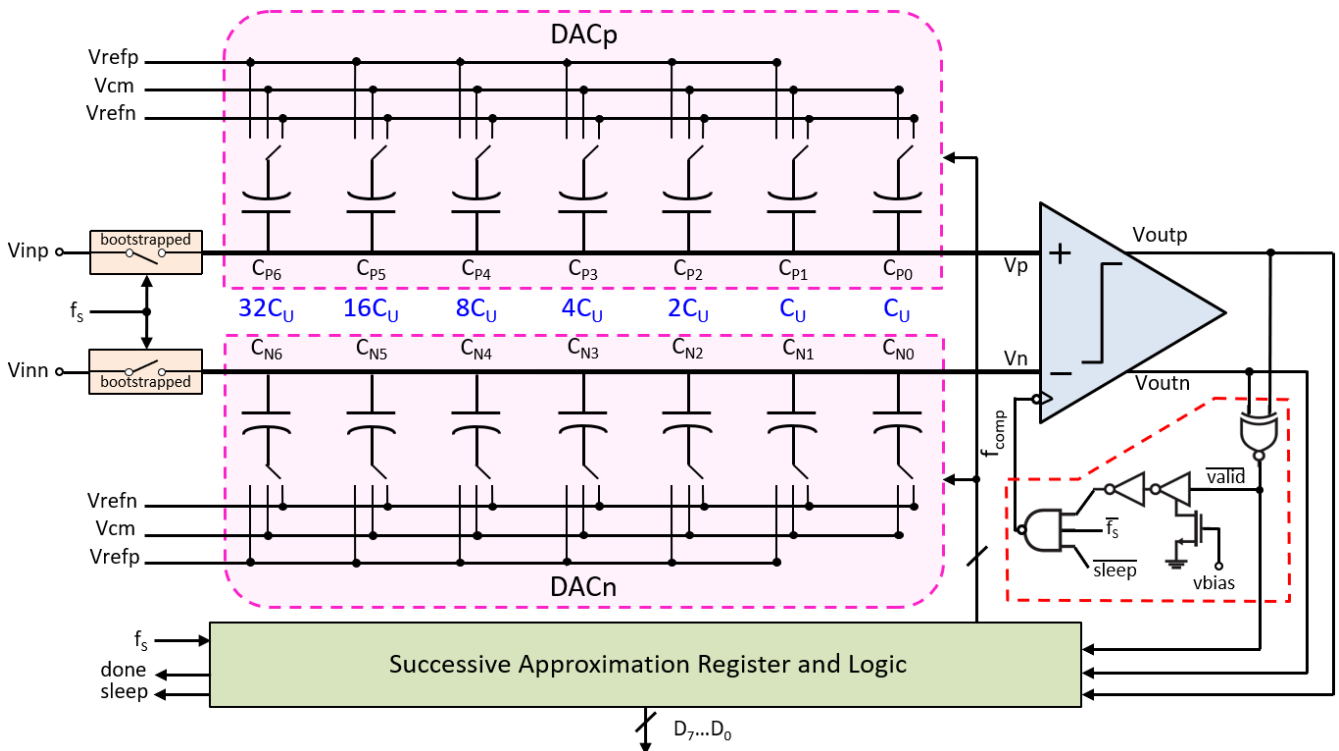


Figure 4.1: The architecture of the proposed SAR ADC.

The DAC arrays, DACp and DACn, not only perform the A/D conversion but also function as *Sample-and-Hold*, through top-plate sampling. One cycle starts with the comparator sensing the difference between positive and negative arrays and generating the outputs, which

are fed both to the SAR logic and to the asynchronous logic. The asynchronous logic activates the SAR logic as well as turns off the comparator. Finally, the DAC converts SAR logic output into an analog value, which is again sensed by the comparator. An N-bit conversion requires N-1 comparisons.

Reviewing briefly the primary specifications presented in Chapter 2, the ADC design aims an 8 – bit resolution with sampling frequency of 10 MHz and a power supply of 1V. The signal bandwidth is centered at 3 MHz, with a maximum value of 4 MHz. Additionally, reference levels are $V_{refp} = 750mV$, $V_{cm} = 500mV$ and $V_{refn} = 250mV$, set in the middle of the available range for each signal input, resulting in a full scale of 1 V.

4.1.1 Switching Scheme

While aiming a low power operation, one of the first aspects that one considers is an implementation of an energy-efficient switching scheme for the capacitive DAC, since typically it is the bottleneck for power consumption. On the review presented on Chapter 3, we glimpsed that the switching method implemented on (ZHU; LIANG, 2015), the *OSSI-HBSI* method, showed important efficiency for a low-voltage and low-rate application.

The switching scheme implemented is based on two methods: one-side switching instead (OSSI) and higher-bit switching instead (HBSI). The first method, illustrated in Figure 4.2.(a), takes advantage of the fact that when both plates of a capacitor see the same voltage shift, no energy is consumed. The equivalent capacitance Figure 4.2.(b), in both situations, is connected to the same potential difference ($\Delta V = V_{refp} - V_{cm} = V_{cm}$), and the internal node V_+ sees the necessary voltage shift of $V_{refp}/2$. In this method, the entire array is switched, instead of only one capacitor, or the MSB-array.

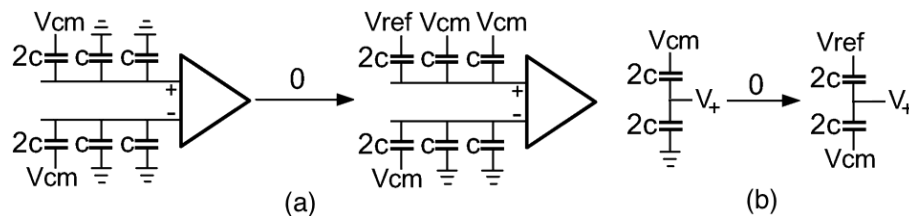


Figure 4.2: (a) The one-side switching instead method (ZHU; LIANG, 2015) and (b) simplified scheme.

The second method, shown in Figure 4.3.(a), reduces the energy consumed by generating half the voltage shift on a capacitance of twice the size. That is, instead of shifting the

capacitance C of V_{refp} , and consuming $3/4 CV_{refp}^2$, the capacitance $2C$ (corresponds in this case to the higher bit) sees a voltage shift of $V_{refp}/2$, thus consuming $1/4 CV_{refp}^2$. The internal node $V+$ of Figure 4.3.(b) sees the necessary voltage shift of $V_{refp}/4$.

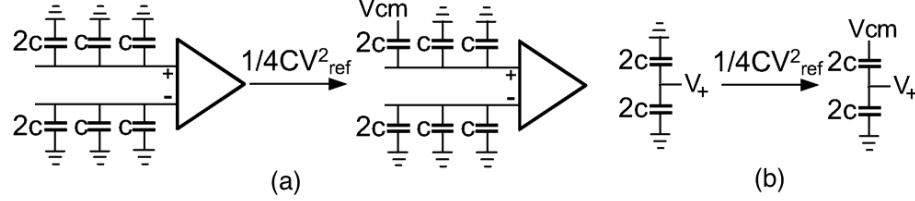


Figure 4.3: (a) The higher-bit switching instead (ZHU; LIANG, 2015) and (b) simplified scheme.

Top-plates sampling allows the estimate of MSB without any switching, followed by OSS1 in the determination of MSB-1. Finally, the remaining comparison cycles employ the HBS1. In the next paragraphs, the switching scheme for the 8-bit converter is described. For simplicity on the following description at equation level, consider with $V_{ref} = V_{refp} - V_{refn}$, and $\Delta V_{in} = V_{inp} - V_{inn}$. Figure 4.4 exemplifies the switching scheme for a 4-bit converter, where $V+$ and $V-$ represent positive and negative reference levels.

1. **Sampling:** During the sampling phase, the bottom plates of the capacitors C_{P6} and C_{N6} are connected to V_{cm} , while the remaining capacitors of both arrays are connected to V_{refn} . At the same time, activation of the bootstrapped switches by f_S connects positive and negative inputs, V_{inp} and V_{inn} , to the comparator's inputs (also capacitors top plates).

$$V_p = V_{inp} \quad V_n = V_{inn} \quad (4.1)$$

2. **MSB-Comparison (D_7):** At the end of the sampling phase, the transition of f_S from "1" to "0" turns off the bootstrapped switches and triggers the asynchronous logic. The asynchronous logic, which will be explored further on, is in charge of activating the comparator. At the falling edge of f_{comp} , the comparator senses nodes V_p and V_n directly and generates the MSB, D_7 , at its output.

$$\begin{aligned} \Delta V_{in} > 0 &\rightarrow D_7 = 1 \\ \Delta V_{in} < 0 &\rightarrow D_7 = 0 \end{aligned} \quad (4.2)$$

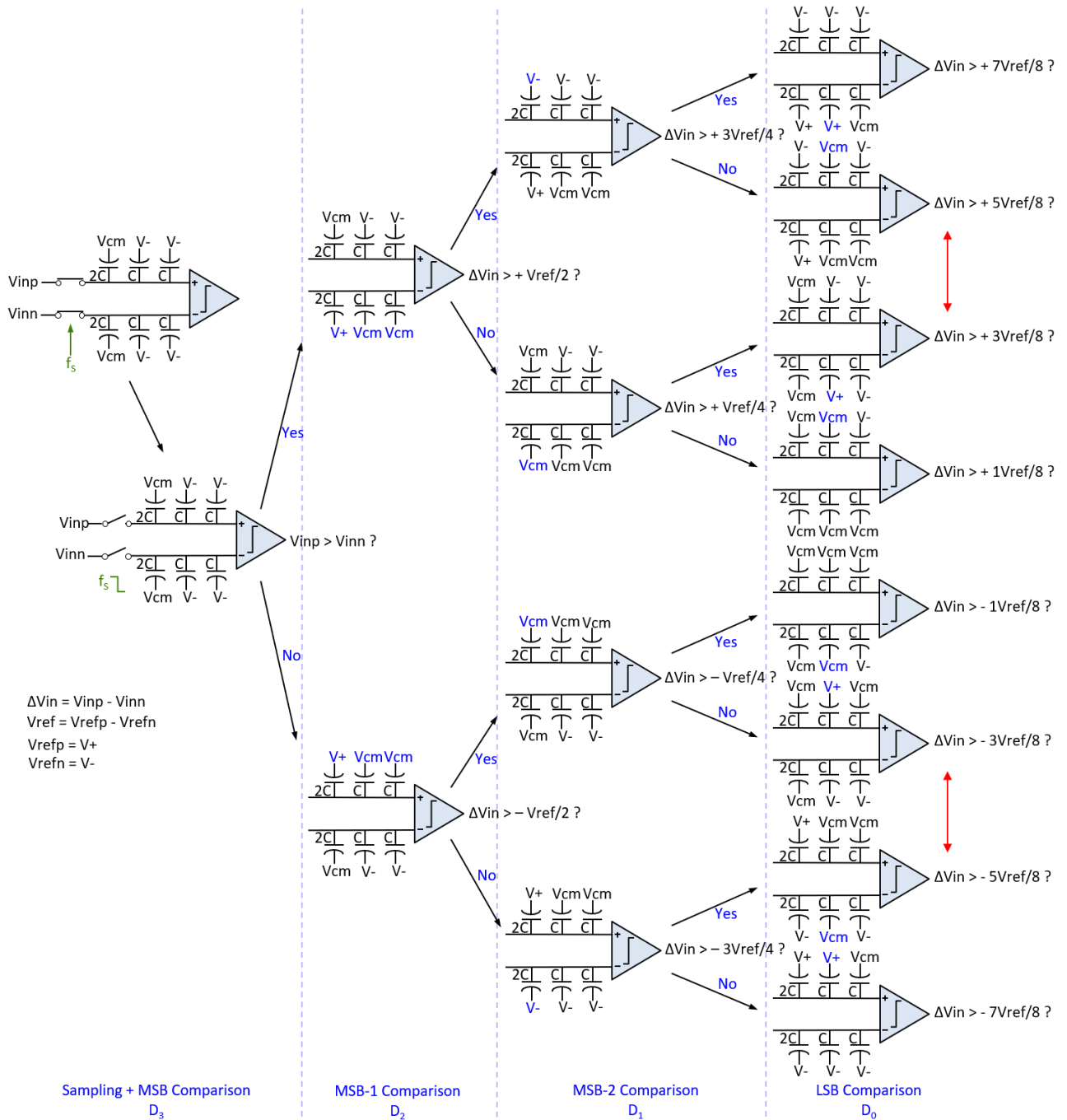


Figure 4.4: Switching scheme for a 4-bit ADC.

- MSB-1 Comparison (D_6):** The OSSI method is applied at this moment. If $D_7 = 1$, an up-transition of $V_{ref}/2$ occurs for all the capacitors of DACn array. Capacitor C_{N6} switches from V_{cm} to V_{refp} and $C_{N5} - C_{N0}$ from V_{refn} to V_{cm} ; meanwhile, the DACp array remains unchanged. As a consequence, V_n shifts of $V_{ref}/2$, like illustrated in Figure 4.2. If $D_7 = 0$, a similar operation occurs with the roles of DACp and DACn interchanged.

$$\begin{aligned}
\mathbf{D}_7 = \mathbf{1} &\rightarrow \begin{cases} V_p = V_{inp} \\ V_n = V_{inn} + \mathbf{V}_{ref}/2 \\ \Delta V = \Delta V_{in} - V_{ref}/2 \end{cases} \\
\mathbf{D}_7 = \mathbf{0} &\rightarrow \begin{cases} V_p = V_{inp} + \mathbf{V}_{ref}/2 \\ V_n = V_{inn} \\ \Delta V = \Delta V_{in} + V_{ref}/2 \end{cases}
\end{aligned} \tag{4.3}$$

At the second fall of f_{comp} , the comparator generates D_6 .

$$\begin{aligned}
V_p > V_n &\rightarrow D_6 = 1 \\
V_p < V_n &\rightarrow D_6 = 0
\end{aligned} \tag{4.4}$$

4. **MSB-2 Comparison (D_5):** From this moment on, the switching is based on the HBSI method. If $D_6 = 1$, a down-transition of $V_{ref}/2$ happens on C_{P6} . Depending on the D_7 decision, the switching of C_{P6} will occur from V_{cm} to V_{refn} (if $D_7 = 1$) or from V_{refp} to V_{cm} (if $D_7 = 0$). As a consequence, node V_p drops down by $V_{ref}/4$, and V_n remains unchanged, as illustrated on equation 4.5. Similarly, with $D_6 = 0$, C_{N6} is switched, and V_n changes accordingly to equation 4.6.

$$D_7 \mathbf{D}_6 = \mathbf{11} \rightarrow \begin{cases} V_p = V_{inp} - \mathbf{V}_{ref}/4 \\ V_n = V_{inn} + V_{ref}/2 \\ \Delta V = \Delta V_{in} - 3V_{ref}/4 \end{cases} \tag{4.5}$$

$$D_7 \mathbf{D}_6 = \mathbf{01} \rightarrow \begin{cases} V_p = V_{inp} + V_{ref}/2 - \mathbf{V}_{ref}/4 \\ V_n = V_{inn} \\ \Delta V = \Delta V_{in} + V_{ref}/4 \end{cases}$$

$$D_7 \mathbf{D}_6 = \mathbf{10} \rightarrow \begin{cases} V_p = V_{inp} \\ V_n = V_{inn} + V_{ref}/2 - \mathbf{V}_{ref}/4 \\ \Delta V = \Delta V_{in} - V_{ref}/4 \end{cases} \tag{4.6}$$

$$D_7 \mathbf{D}_6 = \mathbf{00} \rightarrow \begin{cases} V_p = V_{inp} + V_{ref}/2 \\ V_n = V_{inn} - \mathbf{V}_{ref}/4 \\ \Delta V = \Delta V_{in} + 3V_{ref}/4 \end{cases}$$

Then, D_5 is resolved at the third falling edge of f_{comp} , similarly to D_6 in equation 4.4.

5. **Remaining Comparisons (D_i with $i = 4..0$):** All the remaining bits are decided accord-

ing to the HBSI method. Also, from now on, a comparison that results in "1", affects the DACn array; likewise, a comparison that results "0" influences the DACp array. In both cases and for each step, only one capacitor is switched and sees an up-transition of $V_{ref}/2$. The nodes V_n or V_p increase by a parcel of V_{ref} , seeing that an up-transition occurs.

Using D_4 as example, preceding its decision, C_{N5} or C_{P5} will see an up-transition of $V_{ref}/2$, that ultimately depends on the MSB decision (because the D_7 resulted in switching of the entire DACn or DACp array). If $D_5 = 1$, C_{N5} switches from V_{cm} to V_{refp} , independently of D_6 , but only if $D_7 = 1$; if, in turn, $D_7 = 0$, still with $D_5 = 1$, C_{N5} switches from V_{refn} to V_{cm} . In both situations, the switching result in an increase of V_n by $V_{ref}/8$. This example is illustrated in equation 4.7, and equation 4.8 shows the scenario for when $D_5 = 0$. After this, with the next falling edge of f_{comp} , the comparator then estimates D_4 , similarly to D_6 in equation 4.4.

This procedure goes until the bit D_0 is defined.

$$\begin{aligned}
 D_7 D_6 D_5 = 111 &\rightarrow \begin{cases} V_p = V_{inp} - V_{ref}/4 \\ V_n = V_{inn} + V_{ref}/2 + \mathbf{V}_{ref}/8 \\ \Delta V = \Delta V_{in} - 7V_{ref}/8 \end{cases} \\
 D_7 D_6 D_5 = 101 &\rightarrow \begin{cases} V_p = V_{inp} \\ V_n = V_{inn} + V_{ref}/2 - V_{ref}/4 + \mathbf{V}_{ref}/8 \\ \Delta V = \Delta V_{in} - 3V_{ref}/8 \end{cases} \\
 D_7 D_6 D_5 = 011 &\rightarrow \begin{cases} V_p = V_{inp} + V_{ref}/2 - V_{ref}/4 \\ V_n = V_{inn} + \mathbf{V}_{ref}/8 \\ \Delta V = \Delta V_{in} + V_{ref}/8 \end{cases} \\
 D_7 D_6 D_5 = 001 &\rightarrow \begin{cases} V_p = V_{inp} + V_{ref}/2 \\ V_n = V_{inn} - V_{ref}/4 + \mathbf{V}_{ref}/8 \\ \Delta V = \Delta V_{in} + 5V_{ref}/8 \end{cases}
 \end{aligned} \tag{4.7}$$

$$\begin{aligned}
D_7 D_6 D_5 = 110 &\rightarrow \begin{cases} V_p = V_{inp} - V_{ref}/4 + \mathbf{V}_{ref}/8 \\ V_n = V_{inn} + V_{ref}/2 \\ \Delta V = \Delta V_{in} - 5V_{ref}/8 \end{cases} \\
D_7 D_6 D_5 = 100 &\rightarrow \begin{cases} V_p = V_{inp} + \mathbf{V}_{ref}/8 \\ V_n = V_{inn} + V_{ref}/2 - V_{ref}/4 \\ \Delta V = \Delta V_{in} - V_{ref}/8 \end{cases} \\
D_7 D_6 D_5 = 010 &\rightarrow \begin{cases} V_p = V_{inp} + V_{ref}/2 - V_{ref}/4 + \mathbf{V}_{ref}/8 \\ V_n = V_{inn} \\ \Delta V = \Delta V_{in} + 5V_{ref}/8 \end{cases} \\
D_7 D_6 D_5 = 000 &\rightarrow \begin{cases} V_p = V_{inp} + V_{ref}/2 + \mathbf{V}_{ref}/8 \\ V_n = V_{inn} - V_{ref}/4 \\ \Delta V = \Delta V_{in} + 7V_{ref}/8 \end{cases}
\end{aligned} \tag{4.8}$$

It can be seen, through equations 4.2-4.8, the typical the binary-search algorithm converging, just like presented in Figure 3.8.

It is worth mentioning that, unlike, traditional switching algorithms in which the status of either an MSB-capacitor or an MSB-array change at initial steps, this switching algorithm switches an entire array. This array ultimately plays the role of an MSB-array. As a consequence, this method is only applicable to a differential structure, since the convergence happens only with either DACp array or DACn array switching and decreasing the difference between nodes V_p and V_n .

Another outcome is that there is no need for an MSB capacitor, cutting by half the amount of capacitors when compared to other differential structures of the same number of bits; and employing a similar number of unit capacitors when compared to the typical single topology of the same resolution.

4.2 Circuit Implementation

4.2.1 Charge Redistribution DAC

The total capacitance of the DAC array is directly dependant on the number of unit capacitors, C_{unit} , necessary for the switching scheme implementation, as well as the size of those

unit capacitors. To reduce the power consumption, C_{unit} values should be kept as small as possible. However, sizing of the unit capacitors must additionally account for noise requirements and matching properties, as well as the design rule of the manufacturing process.

Regarding noise, thermal noise poses a limitation to the size of the sampling capacitor, the kT/C -noise, briefly introduced in Chapter 3. This noise contribution should be smaller than the quantization noise, to avoid further signal degradation.

For a peak-to-peak Full Scale of 1 V and a resolution of 8 bits, 1 LSB corresponds to 3.906 mV , according to equation 3.2. From equation 3.3, the quantization noise equals 1.128 mV , and approximately 0.4 mV_{rms} . Therefore, a kT/C -noise smaller than the quantization noise results in a minimum sampling capacitor $C_S = 26 fF$.

In the Charge Redistribution SAR architecture, because the DAC array plays the role of sampling capacitor and all the capacitors are connected in parallel, the total capacitance is large enough to suppress the thermal noise at the bootstrapped switch output. Therefore, mismatch requirements dictate the sizing of the unit capacitor.

As mentioned in Chapter 3, the DAC array must be as accurate as the desired resolution. To guarantee that, the capacitor mismatch should satisfy both $3\sigma_{INL,MAX} < 1/2LSB$ and $3\sigma_{DNL,MAX} < 1/2LSB$. The INL deviation relates to the number of capacitors switched to obtain a digital code, and the DNL to the number of capacitors switched in a transition between two adjacent digital codes.

In the 4-bit example of Figure 4.4, the switching at each comparison step is indicated in blue. It can be seen that, in order to generate the 4 bits, 7 capacitors were switched (after 1st-comparison, the entire array is switched = $4C_u$; after the 2nd, only C_{P3} or $C_{N3} = 2C_u$; after the 3rd, only C_{P2} or $C_{N2} = C_u$). For the N-bit converter, an entire conversion requires switching of $2 \times (2^{N-2} - 1) + 1$ unit elements. Additionally, the worst cases of differential nonlinearity occur when switching of 6 capacitors are needed (C_{P3} and $C_{N3} = 2C_u$ each, C_{P2} and $C_{N2} = C_u$ each), indicated by the red arrows in Figure 4.4. In the case of an N-bit converter, switching of $2 \times (2^{N-2} - 1)$ unit elements are necessary for the transition between two adjacent digital codes.

The effective capacitance of each unit capacitor C_u , due to process variation, deviates by an error of δ_u from the nominal value, as shown in equation 4.9.

$$\begin{aligned} C_0 &= C_u + \delta_0 \\ C_i &= 2^{i-1}C_u + \delta_i \quad (i = 1 \dots n - 2) \end{aligned} \tag{4.9}$$

Assuming that the error distributions of C_u satisfy the Gaussian distribution, the mean

and variance error terms are $E(\delta_u) = 0$ and $E(\delta_u^2) = \sigma_u^2$. If n unit capacitors are connected in parallel, the standard deviation can be obtained by adding n independent random variables:

$$\begin{aligned}\sigma^2(\delta_0) &= \sigma_u^2 \\ \sigma^2(\delta_i) &= 2^{i-1}\sigma_u^2 \quad (i = 1 \dots n-2)\end{aligned}\quad (4.10)$$

For a given digital input, the DAC array generates a corresponding $V_{DAC}(X)$. Considering the array initially discharged ($V_{in} = 0$), the analog output of the N-bit capacitive DAC of the studied scheme and its total error are given by:

$$\begin{aligned}V_{DAC}(X) &= \frac{\sum_{i=1}^{N-2} (2^{i-1}C_u + \delta_i)S_i + (C_u + \delta_0)S_0}{\sum_{i=0}^{N-2} C_u} V_{ref} \\ V_{error,DAC}(X) &= \frac{\sum_{i=0}^{N-2} \delta_i S_i}{\sum_{i=0}^{N-2} C_u} V_{ref}\end{aligned}\quad (4.11)$$

where the DAC digital input $X=[S_i \dots S_0]$, S_i equal to 1, 1/2 or 0 representing the DAC connecting to V_{refp} , V_{cm} or V_{refn} . The SAR logic generates S_i according to the comparator's output.

If we recall the expressions for estimating INL and DNL from Chapter 3, their deviations, in terms of the voltage error that results from the C_u deviations, can be expressed as:

$$INL = \frac{V_{DAC,real}(X) - V_{DAC,ideal}(X)}{LSB} = \frac{V_{error}(X)}{LSB}\quad (4.12)$$

$$DNL = INL(X) - INL(X-1) = \frac{V_{error}(X) - V_{error}(X-1)}{LSB}\quad (4.13)$$

By combining equation 4.11 with equations 4.12 and 4.13, and considering the worst cases for INL and DNL, the variance of the maximum INL and DNL can be estimated as:

$$\begin{aligned}\sigma_{INL,max} &= \sqrt{(2^{N-1} - 1)} \frac{\sigma_u}{C_u}, \quad \sigma_{DNL,max} = \sqrt{(2^{N-1} - 2)} \frac{\sigma_u}{C_u} \\ \sigma_{INL,max} &\approx \sigma_{DNL,max} \approx \sqrt{2^{N-1}} \frac{\sigma_u}{C_u}\end{aligned}\quad (4.14)$$

In this design, C_u elements are of MIM type. The mismatch of a MIM capacitor in the CMOS 130 nm manufacturing process available is modeled as:

$$\sigma\left(\frac{\Delta C}{C}\right) = \sqrt{\frac{M_A^2}{WL} + \frac{M_W^2}{W^2} + \frac{M_L^2}{L^2}}, \quad C = K_C \cdot A\quad (4.15)$$

where W , L and A represent the capacitor width, length, and area, respectively; M_A ,

M_W and M_L are matching coefficients, and K_C is the capacitor density parameter.

Considering a squared capacitor and the PDK Pelgrom coefficients for the MIM type capacitor ($M_A = 4.0\% \mu m$, $M_W = 1.0\% \mu m$, $M_L = 0.0\% \mu m$), $\sigma_u(\Delta C/C)$ equals to K_σ/\sqrt{A} , with $K_\sigma = 4.12\% \mu m$. A reasonable bound for C_u accounting for equation 4.14 and $K_C = 2.05 \text{ fF}/\mu m^2$ is then defined as:

$$C_u \approx 36 \cdot 2^{N-1} K_C K_\sigma^2 \approx 16 \text{ fF} \quad (4.16)$$

However, for the CMOS 130 nm manufacturing process in question, the minimum MIM capacitor available is 60 fF (C_{min}). An equivalent capacitor of larger size is possible by connecting capacitors in parallel, a feature that the charge redistribution architecture employs on its DAC. On the other hand, the capacitor series configuration enables a reduction of the equivalent capacitance. Thus the connection of two minimum capacitors in series results in a unit capacitor of 30 fF ($C_u = C_{min}/2$). Further reduction of C_u is possible by adding more capacitors in series, as illustrated in Figure 4.5.

A direct advantage of connecting two capacitors in series to generate C_u is the reduction of capacitor number used by almost half, from 64 to 35 capacitors. With the connection of four C_{min} in series, this number is further reduced to 25. Additionally, the different C_u and the distinct topologies result in different total equivalent capacitances, each reduction decreasing C_{eq} by half (and also fulfilling the KT/C -noise requirement). Finally, a smaller equivalent capacitance allows reduction power consumption.

The compromise between power consumption and linearity made the topology in which $C_u = C_{min}/2$ more suitable for the low power radio application. Still, all three different DAC topologies of Figure 4.5 are explored throughout Chapter 5.

The switches also play an important role in the DAC performance, especially regarding time consumption and speed. Unlike the sampling switch that operates at $f_S = 10 \text{ MHz}$, DAC switches operate typically at $N \times f_S$, where N is the ADC resolution. Hence, the time constant $\tau = R_{on} C_{P/N(i)}$ (with $i = 0 \dots N - 2$) must be such that it allows capacitor charging through the switch resistor R_{on} . A voltage from gate to source V_{GS} exceeding the threshold voltage V_{th} of the transistor sets a conductive channel between source and drain terminals. With a low or near-zero drain to source voltage V_{DS} , the switch on-resistance is given by (MALOBERTI, 2010):

$$R_{on} = \frac{1}{\mu C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{th})} \quad (4.17)$$

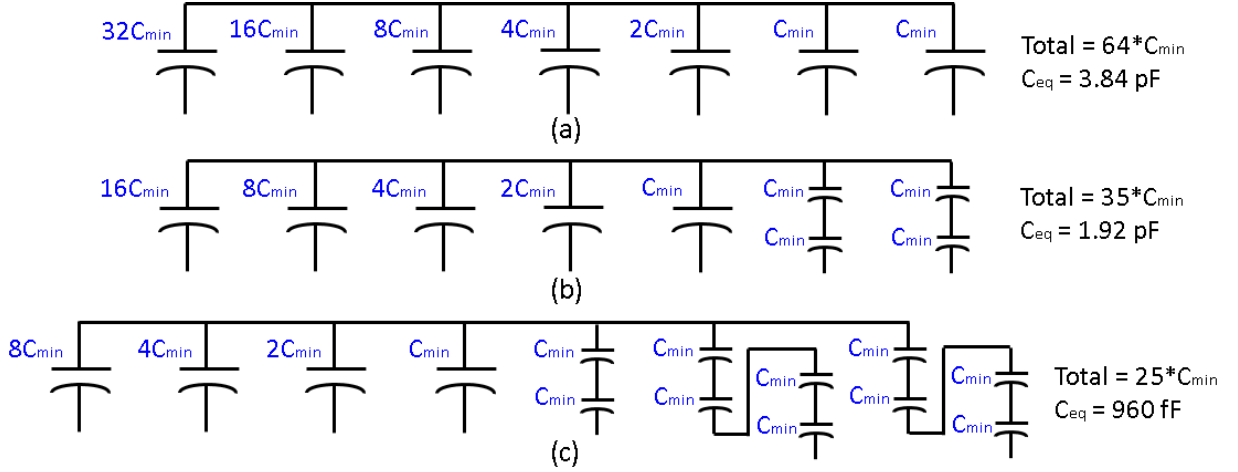


Figure 4.5: DAC topologies based on the different C_u element: (a) $C_u = C_{min}$, (b) $C_u = C_{min}/2$ and (c) $C_u = C_{min}/4$.

where μ represents the carrier mobility, C_{ox} the oxide capacitance; V_{GS} and V_{th} are the gate to source and threshold voltage, respectively; and where W and L represent the transistor width and length.

Equation 4.17 shows that R_{on} increases and goes to infinite as $V_{GS} - V_{th}$ nears zero. When the switch input voltage varies over a large range, often a complementary switch is necessary, with both NMOS and PMOS, to ensure the on-state of the switch. Additionally, another issue that often generates linearity errors is the channel charge-injection on the hold-mode. When the switch turns off, the switch charge moves to both the sampling capacitor, creating a pedestal step, and to the source signal.

In this project, the signals coming from the SAR logic activate the switch by feeding its gate with either "0" or "1", so $V_G = 0$ or V_{DD} . The switches input are the voltage references fed to the capacitors, which are $V_{refp} = 750 \text{ mV}$, $V_{cm} = 500 \text{ mV}$ and $V_{refn} = 250 \text{ mV}$. Thus, the minimum V_{GS} is equal to 250 mV . The *low-VT* transistors available on the manufacturing process have a $V_{th} = 101 \text{ mV}$, resulting in $V_{GS} > V_{th}$ by a margin that allows usage of NMOS-only switches. The narrower dynamic range also ensures a smaller variation of R_{on} . Additionally, dummy transistors with half the size of the switch serve as compensation for the charge injection effect (MALOBERTI, 2010), with a complementary activation when compared to the switches. Finally, since the array of capacitors follows a binary growth, the switches were sized accordingly to optimize power consumption.

The switches sizes must be such that its time constant allows settling of the capacitor in time for the next comparison. For $f_s = 10 \text{ MHz}$, the conversion process can last up to 100 ns . For this algorithm, the sampling time plus eight cycles are necessary ($t_{cycle} = t_{comp} + t_{SAR} + t_{DAC}$). To give some margin and simplify the calculation, we considered a total of 10 cycles,

which results in DAC operation frequency of 100 MHz and a time constant $\tau < 1.6\text{ ns}$.

Considering the smaller switch, the on-resistance is given by $R_{on} = \tau/C_u$, where $C_u = 30\text{ fF}$. With a maximum $\tau = 1.6\text{ ns}$, it gives a maximum $R_{on} = 53\text{ k}\Omega$. The time constant τ and the available time per cycle must be enough so that the voltage across the charging capacitor, shown on equation 4.18 is within the $\pm 0.5\text{ LSB}$ limit. As mentioned earlier, the maximum voltage shift that the capacitors see is $V_{ref}/2$, which corresponds to 250 mV . The graph of Figure 4.6 illustrates the voltage across the capacitor, with $V = 250\text{ mV}$, in terms of τ . Indicated on the graph are the voltage levels regarding LSB, for different τ . The time window should be at least $5 \times \tau$ to respect the $\pm 0.5\text{ LSB}$ limit.

$$V_C(t) = V(1 - e^{-t/\tau}) \quad (4.18)$$

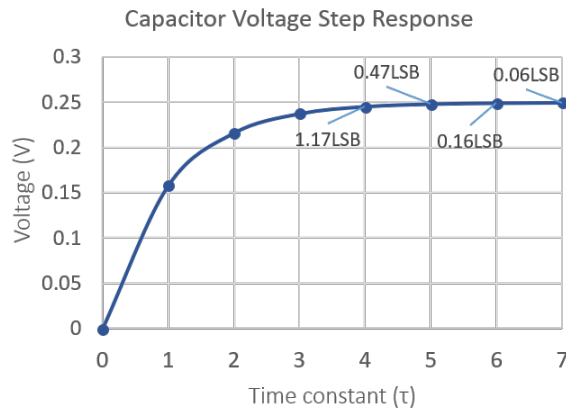


Figure 4.6: Charge Voltage Step Response.

With equation 4.17 for the different switch input values and considering the 130 nm process ($\mu C_{ox} = 612\mu\text{ A/V}^2$), result in the relationships of equation 4.19. By selecting an aspect ratio of 1 and considering the worst input situation, $V_{in} = V_{refp}$, it gives a $R_{on} \approx 10\text{ k}\Omega$, and a $\tau = 300\text{ ps}$. With this time constant, a time window of 2 ns , which corresponds to 6.667τ , is enough for the voltage in the capacitor settle with a precision of 0.01 LSB .

$$\begin{aligned} V_{refp} = 0.75 &\rightarrow R_{on} = 10.9\text{ k}\Omega \times \frac{L}{W} \\ V_{cm} = 0.5 &\rightarrow R_{on} = 4.1\text{ k}\Omega \times \frac{L}{W} \\ V_{refn} = 0.25 &\rightarrow R_{on} = 2.5\text{ k}\Omega \times \frac{L}{W} \end{aligned} \quad (4.19)$$

Considering an aspect ratio of 1, the sizes of the switches will be limited by the minimum width of the transistor, since the dummy transistor must have half of the switch aspect

ratio. With that in mind, and avoiding the minimum size to reduce the effect of local variations (VITTOZ, 2015), the sizes for length and width of NMOS switches were: $L_{all} = 800 \text{ nm}$ and $W_0 = 800 \text{ nm}$, $W_0 = W_1 = \frac{W_2}{2} = \frac{W_3}{4} = \frac{W_4}{8} = \frac{W_5}{16} = \frac{W_6}{32}$. Dummy transistors follows the same relationship, but with $W_{D0} = 400 \text{ nm}$.

4.2.2 Bootstrapped Switch

Like the switches from the DAC, the sampling switch suffers from the R_{on} variation too, which generates distortion. The bootstrapping technique minimizes the R_{on} dependency with the input signal by connecting a "constant voltage source" between gate and source of the switch. This connection fixates V_{GS} , which additionally reduces the charge injection effect. A pre-charged capacitor plays the role of the voltage source, *bootstrapping* the gate to the source, and thus allowing them to change in unison.

The bootstrapped switch topology used in this work is shown in Figure 4.7 (RAZAVI, 2015a). Transistor M_1 is the switch itself, and the additional transistors allow turning off of M_1 as well as recharging of C_B .

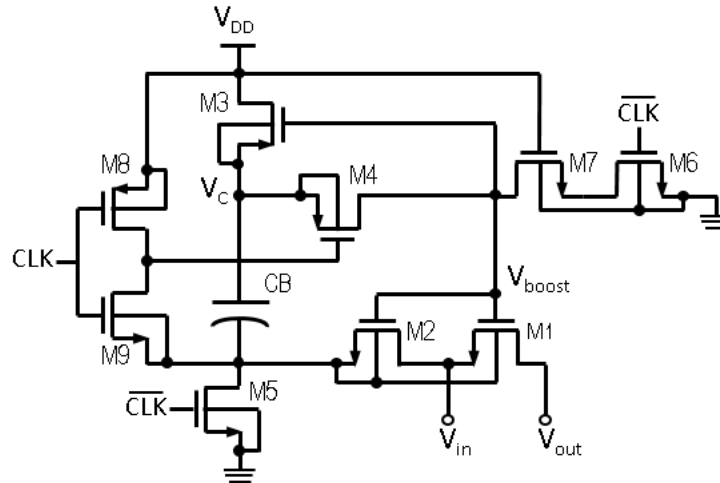


Figure 4.7: Schematic of the bootstrapped switch.

When $CLK = 0$, V_{boost} is connected to GND through M_6 ; transistors M_3 and M_5 connect top and bottom of C_B to V_{DD} and GND , respectively, charging the capacitor with V_{DD} ; transistors M_1 , M_2 and M_4 are off.

When $CLK = 1$, transistors M_5 and M_6 turn off, and transistor M_4 turns on; V_{boost} is connected to top plate of C_B , which turns on transistors M_1 and M_2 thus connecting V_{in} to the capacitor bottom plate, and turns off transistor M_3 . At this point, $V_{boost} = V_{in} + V_{DD}$, a characteristic that is advantageous to low-voltage designs.

Some important considerations of this topology are worth mentioning. First, to avoid the exchange of roles between M_3 source and drain, its gate is bootstrapped to V_{boost} instead of connected to VDD . Furthermore, transistor M_2 senses the input, just like switch M_1 . For high values of V_{in} , the transistor M_2 would not be properly switched (large on-resistance) if its gate was connected to VDD . Thus, just like M_3 , the gate of M_2 is bootstrapped. Finally, transistor M_7 was added to reduce the stress on transistor M_6 caused by V_{boost} at its drain greater than VDD . The resulting cascode device shields M_6 .

The final sizing of transistors M_{1-9} was $L_{all} = 120 \text{ nm}$, and $W_{all} = 1 \text{ }\mu\text{m}$, and the capacitor was set to $C_B = 100 \text{ fF}$. Transistors M_1 , M_2 and M_9 are isolated NMOS transistors available on the CMOS process employed.

4.2.3 Asynchronous Logic

To further reduce the power consumption, along with the efficient switching-scheme, an asynchronous structure was implemented. As mentioned in Chapter 3, an asynchronous strategy corresponds to a duty-cycling technique, which turns off comparator to reduce power consumption.

In a synchronous architecture, the A/D converter has the sampling frequency and a higher clock frequency as inputs. Usually, this higher clock, a fraction of f_S , has a fixed pulse width that keeps comparator on active state longer than necessary.

The comparator, which typically consists of a regenerative latch, generates valid results with different delays depending on the voltage difference at its inputs. The greater the difference, the faster the response. This range of possible t_{comp} is used as an advantage in an asynchronous implementation, by which a controller logic turns off the comparator as soon as a valid output is available. This logic, which was based on the work of (RABUSKE; FERNANDES, 2016), is shown in Figure 4.8.

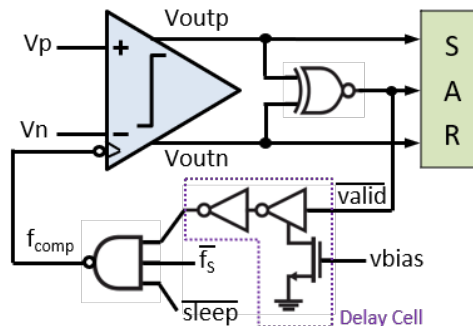


Figure 4.8: Asynchronous control logic.

It consists of a self-timed controller that regulates the binary-search algorithm and synchronizes the digital circuitry of the SAR block. Signals f_S , $sleep$ or $valid$ control the activation of the comparator. When either f_S or $sleep$ are at VDD , the comparator is inactive ($f_{comp} = "1"$), which corresponds, respectively, to the sampling phase and the moment after the completion of the binary search and $sleep$ changes state to VDD . The $valid$ signal, on the other hand, has the complementary behavior, a transition from "1" to "0" turns off the comparator. It is a self-timed loop because the comparator's outputs cause changes on $valid$. Figure 4.9 shows the timing sequence of the ADC SAR designed.

At the beginning of the sampling phase, the rising edge of f_S comes and changes the signal $sleep$ changes to zero, as indicated by the yellow arrow. Meanwhile, the inputs are sampled. At the falling edge of the sampling signal, the comparator turns on and performs the 1st comparison (red arrow on Figure 4.9).

The comparator outputs, which initially were at VDD also maintaining $valid$ at VDD , change accordingly to the inputs of the comparator causing $valid$ to transition from "1" to "0". This transition is not affected by the delay cell, and the control loop generates a rising edge of f_{comp} . The transition of f_{comp} turns off the comparator, and generates a shift on the $valid$ signal from "0" to "1". This time, the $valid$ transition from "0" to "1" at the delay cell input generates a delay on the next transition of f_{comp} and, consequently, on the activation of the comparator. Blue arrows on Figure 4.9 illustrate this procedure.

At every down-transition i of $valid$, the SAR logic stores the D_i bit generated at the comparison, where $i = 1 \dots 8$. On the last comparison, the $valid$ signal triggers the signal $done$ indicating the end of conversion, and the digital output D_{out} becomes available, both situations indicated by pink arrows. With the subsequent up-transition of $valid$ (green arrows), the DAC arrays are reset to the initial state, $done$ is set again to low, and finally, the signal $sleep$ changes its state indicating that the A/D converter is in standby waiting for the next sampling signal.

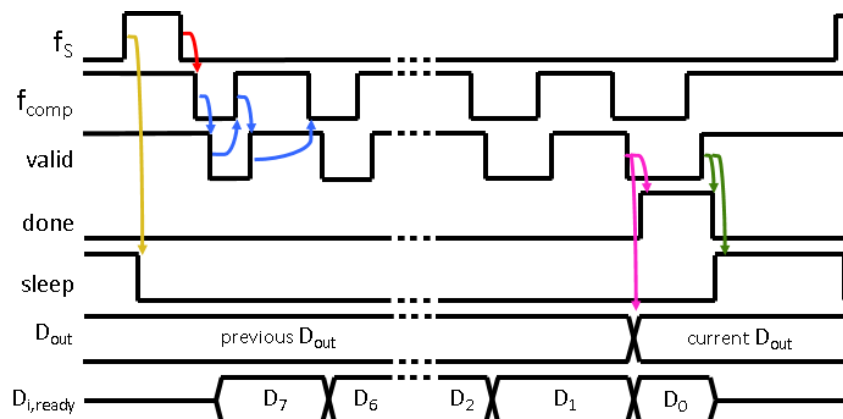


Figure 4.9: Time sequence of the asynchronous SAR control logic.

The delay cell, of Figure 4.8, is basically a *buffer* for which output delays for up- and down-transition differ, the latter being controlled by *bias*. The correct functioning of the asynchronous logic relies upon this delay, which sets the $t_{SAR} + t_{DAC}$. This delay was set around 9 ns , with $v_{bias} = 320\text{ mV}$.

4.2.4 Comparator

The comparator also contributes to the power the consumption, hence, a power-efficient topology is desirable. With that in mind, the comparator proposed (GAWHARE; GAIKWAD, 2016) was chosen for this project. The comparator is a power efficient high-speed version of the conventional dynamic double-tail comparator. Figure 4.10 presents its schematic.

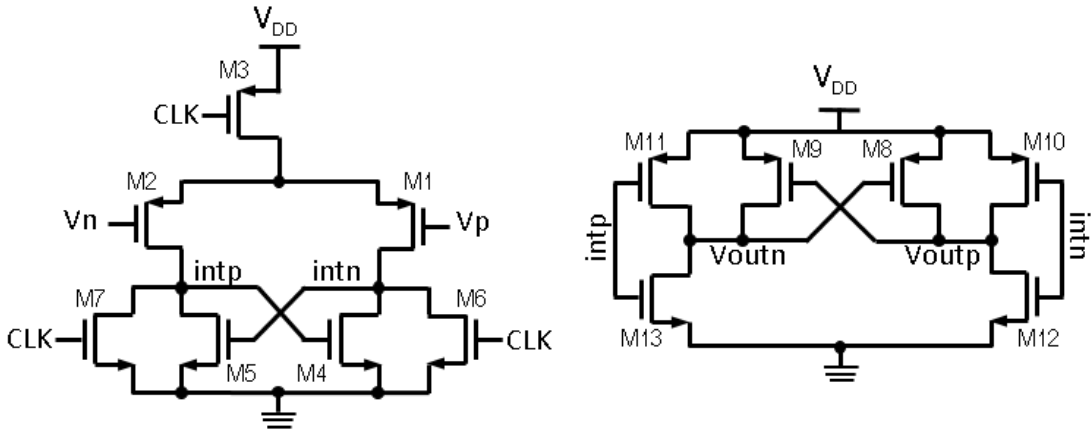


Figure 4.10: Schematic of the comparator.

It consists of two stages, each containing a regenerative latch, and a single tail transistor on the first stage. When CLK is at V_{DD} , the tail transistor M_3 is cutoff, and M_4 and M_5 are active, connecting $intp$ and $intn$ to GND . The outputs V_{outp} and V_{outn} are shorted to V_{DD} through transistors M_{10} and M_{11} . During this phase, no current flows through either one of the stages.

When CLK changes from V_{DD} to GND , current flows through M_3 , while at the same time M_6 and M_7 are cutoff. A difference at the inputs of transistors M_1 and M_2 is amplified and sensed by the regenerative latch composed of M_4 and M_5 . Then, the differential voltage of internal nodes $intn$ and $intp$ is amplified by the regenerative inverters formed by $M_{10} - M_{13}$ and V_{outp} and V_{outn} are set to either V_{DD} or GND depending on the inputs. Due to the regenerative latch composed of M_8 and M_9 , output nodes will be pulled faster to the final state.

The sizing of the comparator took into consideration mainly power consumption and delay, followed by a verification that offset and noise level were suitable. An initial sizing was

set, with most transistors with minimal sizing, and, by employing a parametric analysis, the final sizing was defined. Both power consumption and delay vary regarding the voltage difference at the input of the comparator, V_p and V_n ; the greater the difference, the faster response and the lower the current consumption. Therefore, the final sizing considered an input below the ± 0.5 *LSB* limit, as usual.

Since the asynchronous logic and SAR logic in which the current project was based (RABUSKE; FERNANDES, 2016) defined a logic based on comparator outputs at V_{DD} when idle, the topology proposed in (GAWHARE; GAIKWAD, 2016) was adjusted to provide such an output. As a consequence, input transistors resulted in a PMOS differential pair, which is inherently slower than one with NMOS transistors, due to the smaller mobility of carriers. However, even with a PMOS input pair, the comparator delay remained quite low, smaller than 1 *ns*, which was the approximately time assigned for the t_{comp} on the asynchronous logic section 4.2.3.

For a differential input of 1 *mV*, the comparator delay was $t_{comp} < 500$ *ps*, with a total average current consumption of 5.11 μA and tail current around 4.5 μA . For this scenario, the noise level was below 200 μV_{rms} for the frequency bandwidth up to 5 *MHz*. This noise level corresponds to half of the quantization noise estimated on section 4.2.1. A more thorough analysis regarding the delay, noise and offset will be explored further on Chapter 5.

Additionally, one information of interest when designing a comparator regards the metastability phenomenon. The metastability consists of the occasional inability of a comparator to resolve a small differential input into a valid logic level, within a given time interval (AGAH, 2009). This time interval is the *evaluation time*, that is, the time in which the comparator is latched, which corresponds to half of the operating period. Hence, also on Chapter 5, the comparator time constant will be estimated.

Table 4.1 summarizes the final sizing of the comparator.

$M_{1,2}$	L = 300 nm	W = 3 μm
M_3	L = 200 nm	W = 2 μm
$M_{4,5,6,7}$	L = 120 nm	W = 2 μm
$M_{9,8,10,11}$	L = 120 nm	W = 1 μm
$M_{12,13}$	L = 120 nm	W = 500 nm

4.2.5 SAR Logic

The register bank and the decoder that constitute the SAR Logic were implemented only at the behavioral level, employing the Verilog-AMS language, annexed at the end of this document (Appendix A). At first, we intended to develop custom digital logic to design those blocks at transistor level similar to what was done to the inherently analog blocks. However, the development of everything that was discussed so far posed a limitation on the project of the digital part.

The design of custom digital blocks was a goal from the beginning to optimize power consumption also on the digital side. Initially, the implementation of register bank would also be based on the work of (RABUSKE; FERNANDES, 2016), which are derived from the true-single-phased clocked register.

Another possibility would be the implementation of the register bank and the decoder with standard cells, which typically are available in CMOS processes. With the 130 nm CMOS process used in this project, however, the standard cells were available at the behavioral and physical level alone, to be used in the automatic digital design flow. The implementation of the digital design flow was not included in the original scope of this master thesis. It is, however, of great interest and relevance the study of this specific flow for the analog and mixed-signal designs, such as the converter design.

The digital cells employed in the asynchronous logic and in the generation of the complementary control signals of the switches were designed at schematic level. It included the *nand*, *xnor* and *inverter* that are present on Figure 4.9, as well as additional buffers.

The SAR logic was implemented in a mixed signal language, Verilog-AMS, with the comparators V_p and V_n as analog inputs, and *valid* signal and the sampling frequency f_S , as digital inputs. As outputs, the control switches for each capacitor were defined according to Figure 4.11, using as example the capacitor C_{P6} . Included also as outputs, there are the *done* and *sleep* signals, as well as the digital 8-bit output D_{out} . The SAR logic contains also an internal counter that count the number of comparisons.

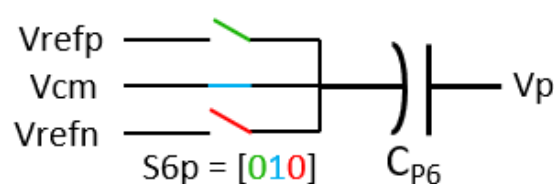


Figure 4.11: Scheme of the switches for each capacitor using as example the capacitor C_{P6} .

As illustrated in Figure 4.1, at the exception of the $C_{P0/N0}$, all the other capacitor may connect to either V_{refp} , V_{cm} or to V_{refn} , thus three switches are implemented in parallel. Each switch has its control modeled as a register within the code. Annex A contains the code implemented.

4.3 Physical Layout Planning

An important step on a large circuit design consists of the definition of a floorplan of said design. Depending on the area constraints of a specific project, the floorplan may be done as one of the initial steps, concurrently with the schematic design or even after the schematic verification. In the low power radio project in question, area constraints were not predefined, so the floorplan was only considered after the schematic design.

Typically data converters occupy a large silicon area, so, even though the current project did not include area specifications, a floorplan for the A/D Converter was defined, and is illustrated on Figure 4.12.(a). Along with the placement planning, a routing planning is also evident in Figure 4.12.(a). Symmetry was an essential aspect considered in the floorplan, as well as minimization of the interconnection of sensitive paths (VITTOZ, 2015), such as the V_p and V_n , the internal nodes between bootstrapped switch, DAC arrays and comparator.

Figure 4.12.(b) illustrates the capacitive DAC array placement planning. Layout techniques such as common-centroid and usage of dummy structures were planned for gradient compensation and better matching (VITTOZ, 2015).

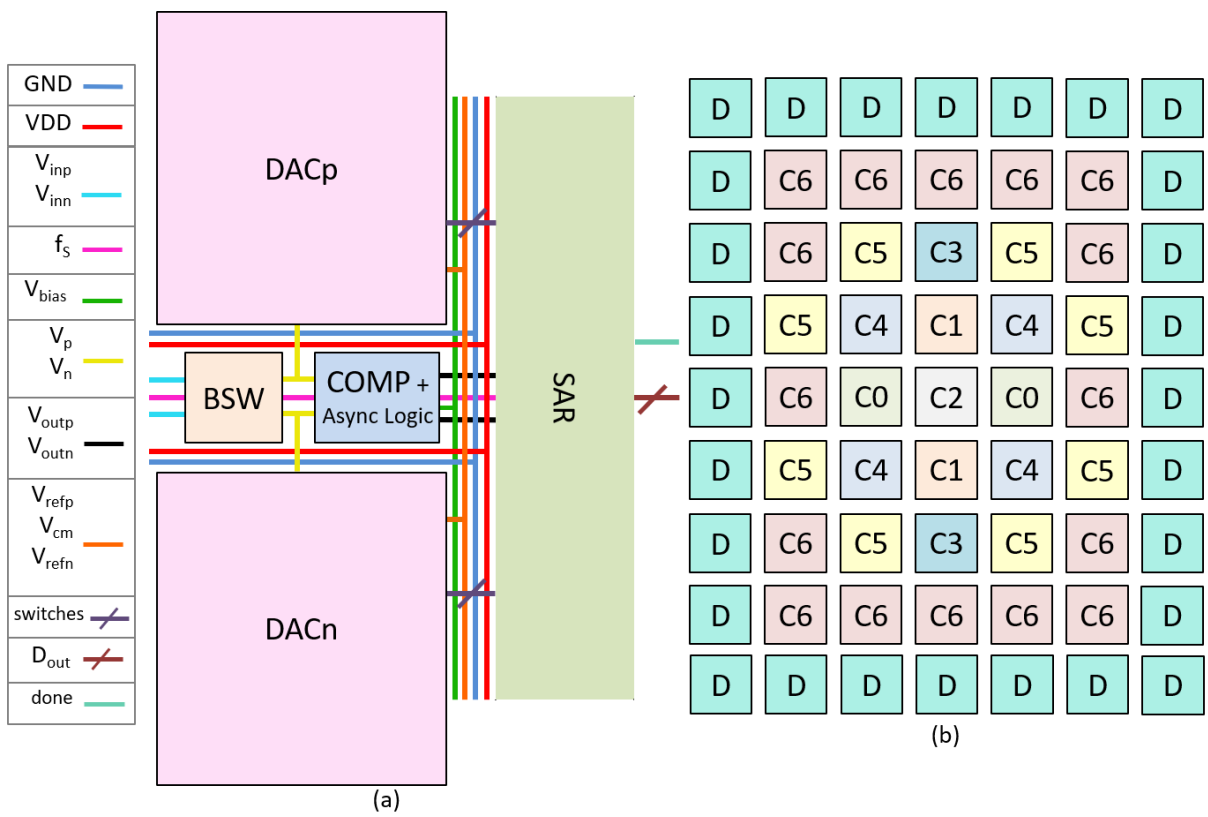


Figure 4.12: Physical layout planning: (a) placement and routing planning of the A/D Converter, and (b) placement planning for the capacitive DAC array.

5 RESULTS AND DISCUSSION

Simulation results at both schematic and physical level are presented in the next sections, starting from the ADC internal blocks, then proceeding to the results of the A/D Converter itself. Selection of the Global Foundries 130 nm CMOS process, formerly IBM, for the converter design was based on its availability on the educational program provided by MOSIS, which could potentially enable fabrication and testing of the ADC.

Along with the performances obtained while aiming the IEEE 802.11ah low power radio application, a performance exploration is also presented, considering sample rate, resolution, supply levels limits and power consumption.

All the simulation results presented in this section were done in the Cadence® Virtuoso® Design Environment Suite and extracted with Spectre®, Spectre® RF and AMS Designer® simulators. Simulations that included the SAR state machine, developed in Verilog-AMS language, were done with the AMS Designer simulator since it consisted of a mixed-signal environment. Some of the analysis for the comparator employed the Analog Periodic Steady-State Analysis (PSS); thus Spectre RF was used.

It is important to highlight, at this stage, that as part of a Master's project of the Graduate Program of Microelectronics (PGMicro) of the Federal University of Rio Grande do Sul (UFRGS), the design and analysis presented in this text were subjected to limitations of the shared resource machine environment with all the other students (disk space, memory, CPU cores, licenses, etc.). Typically Data Converters analysis require long and heavy simulations that tend to occupy great sums of disk space. With that in mind, the discussion surrounding the design space exploration of the implemented ADC is based, whenever possible, in the individual performances of its internal blocks, to optimize the machine requirements needed for the analysis.

Lastly, it is worth stressing out that, although the SAR architecture is composed of four main blocks, sampling switches, DAC arrays, comparator and SAR Logic (including switching algorithm), which were all presented in Chapter 4, in this work major effort was spent on the DAC arrays and the switching algorithm. While both comparator and sampling switches were also implemented at circuit level, they were not optimized, which leaves room for improvement as of now.

5.1 Internal Blocks

5.1.1 Bootstrapped Switch

Sampling switches contribute both in noise and non-linearity of the ADC. The noise requirement, as highlighted in Chapter 4 is not a major concern since the sampling capacitor is large enough to suppress the KT/C noise. Thus, non-linearity and power consumption were the main influences on the bootstrapped switch final sizing.

The test bench of Figure 5.1 was used to evaluate the bootstrapped switch both in time domain and in frequency domain. Since the sampling switches integrate a differential SAR ADC topology, their characterization was also done in a differential manner.

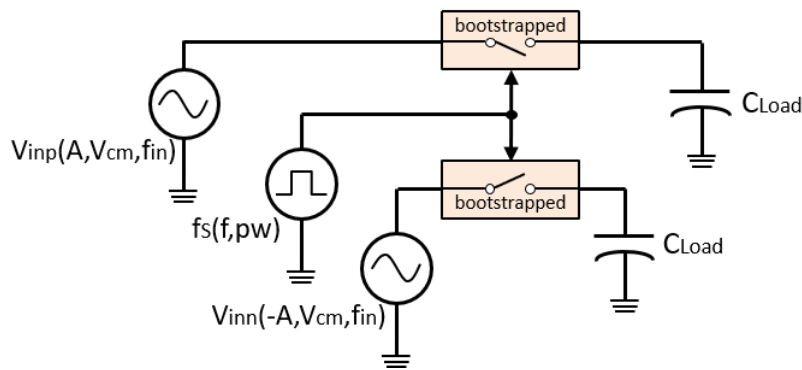


Figure 5.1: Test bench for bootstrapped switch simulation.

The test bench consists of two sinusoidal sources, with amplitude $A = 250mV$, DC level $V_{cm} = 500mV$ and frequency $f_{in} \approx 3MHz$, connected at the bootstrapped switches inputs, and a capacitive load $C_{Load} = 1.92pF$ at their outputs. The sampling clock $f_S = 10MHz$ performs activation of the switch, with a pulse width, pw of $1/10$ of the sampling period T_S (duty cycle of 10%). Supply voltage corresponds to $V_{DD} = 1V$. The low power (LP) radio application defined these test bench parameters. Moreover, to test the bootstrapped switch for the different DAC topologies discussed in Chapter 4 ($C_u = 15fF$, $30fF$ and $60fF$), the load capacitance also assumed values of $C_{Load,15f} = 960fF$ and $C_{Load,60fF} = 3.84pF$.

An initial sizing, with transistors of minimal length of $L_{all} = 120nm$ and $W_{all,init} = 750nm$, slightly smaller the final width of $W_{all} = 1\mu m$, was chosen based on the simulation results at time domain and the power consumption. Input and output voltage levels were within the $\pm 0.5LSB$ limit and the current consumption from the $1 - V$ power supply was $133nA$ for a single bootstrapped switch (differential $266nA$).

To efficiently evaluate the distortion caused by the bootstrapped switch, a frequency domain representation of the output signal was extracted by applying a Fast Fourier Transform (FFT) algorithm. The Spectrum Measurement Toolbox from Virtuoso implements the FFT algorithm that computes the Discrete Fourier Transform (DFT) and enables extraction of dynamic metrics of a circuit, such as SINAD and ENOB. More information about the FFT, and the right selection of input frequency, process known as coherent sampling, can be found in (NATIONALINSTRUMENTS, 2017; TEXASINSTRUMENTS, 2017).

Figure 5.2 shows the simulated frequency spectrum (256-point FFT) of the differential output signal, with $f_{in} = 3.086 \text{ MHz}$, for initial sizing (smaller SW) and final sizing. The non-linearity introduced by the smaller switch resulted in a $SINAD_{init} = 67.8 \text{ dB}$. Increasing the width of the transistors reduced this effect significantly, resulting in a $SINAD = 94.1 \text{ dB}$, at the cost of increasing the current consumption to 170 nA (single). The percentage of total harmonic distortion for the smaller switch, $THD_{init} = 0.036\%$, was significantly larger than for final switch, $THD = 0.001\%$. From the graph, one can see the 30 dB difference on the spurious-free dynamic range (SFDR) between initial and final sizing ($SFDR_{init} = 68.88 \text{ dB}$ and $SFDR = 100.22 \text{ dB}$, respectively). This distortion was even more evident when the capacitance load was greater, equal to 3.84 pF , as can be seen in Figure 5.3.(a).

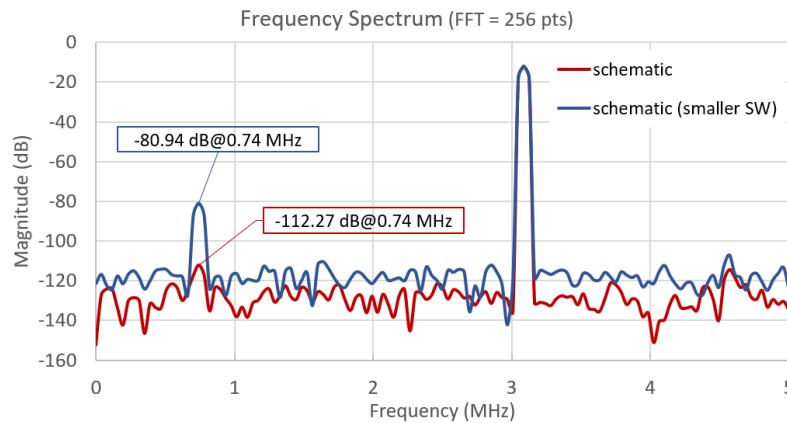


Figure 5.2: Frequency spectrum of differential output signal for both initial sizing (smaller SW) and final sizing.

Additionally to the different unit capacitors, Figures 5.3.(a) and (b) show also simulation results for distinct sampling frequencies ($f_S = 10, 15, 20$ and 32 MHz). On Figure 5.3.(a), results for both sizings are shown with f_{in} near 3 MHz . $SINAD$ did not change significantly for both switching sizes when $C_u = 60 \text{ fF}$, spanning over the range between 46 dB and 38 dB . On the other hand, the different widths and sampling frequencies had a great impact on the $SINAD$ for both $C_u = 15 \text{ fF}$ and 30 fF (ranges of 35 dB and 45 dB , respectively).

Simulations were done also for input frequencies near Nyquist-frequency, illustrated in Figure 5.3.(b), only for the final sizing. For all unit capacitors, SINAD variations surpassed 20 dB for the different sampling frequencies.

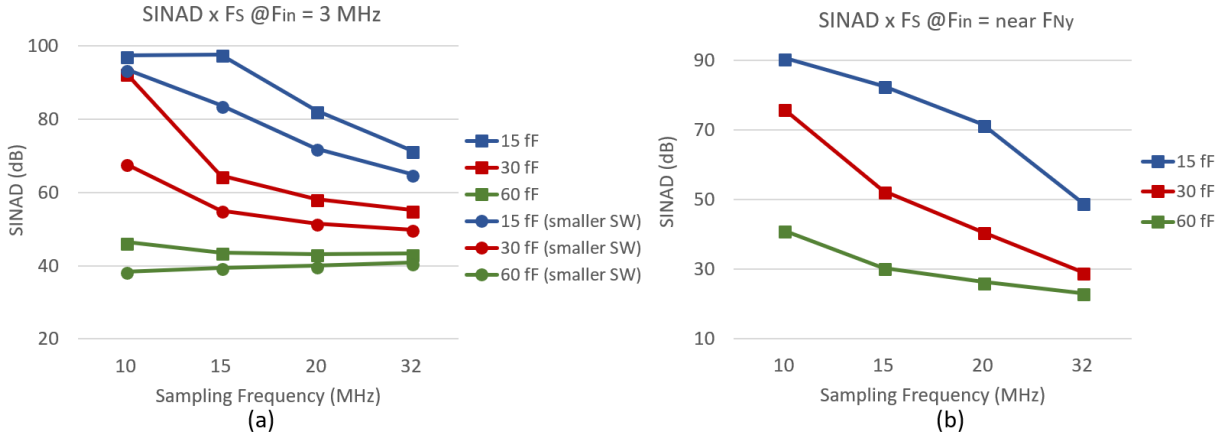


Figure 5.3: Simulated SINAD as function of the sampling frequency f_S for the different load capacitances C_{Load} : (a) for both sizings of the switch, f_{in} near 3 MHz; and (b) for the final sizing, f_{in} near Nyquist-frequency.

The 50-dB SINAD poses a limitation to the employment of this specific switch for the 8-bit resolution. That is, this design is not suitable for $C_{Load} = 3.84$ pF, and it is only suitable when $f_S < 15$ MHz for $C_{Load} = 1.92$ pF; and when $f_S < 20$ MHz for $C_{Load} = 960$ fF.

Figure 5.4 presents a sweep of the supply voltage, V_{DD} (all other variables following the LP radio application, and final sizing). Once again, by looking at the 50-dB SINAD limit, we can see that below 0.8 V, this design will already have a negative impact on the ADC resolution, not accounting for other non-idealities.

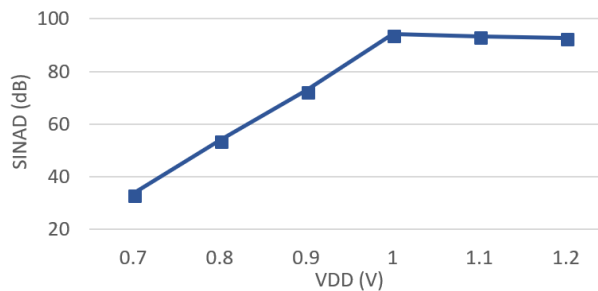


Figure 5.4: Simulated SINAD as function of the supply voltage.

Still, this limitation does not include the spread caused by process and mismatch variations. Figure 5.5 shows the results a 100-run Monte Carlo simulation (parameters in accordance to the LP radio). The spread due to process variations is much more significant than the one caused by mismatch, with a standard deviation higher than 6 dB (which, simply put, corresponds to more than 1-bit variation). Nevertheless, for the worst sample considering process

and mismatch variations, the SINAD was around 69 dB and, hence, an ENOB of 11.2 bits , which is within the requirements of the LP radio.

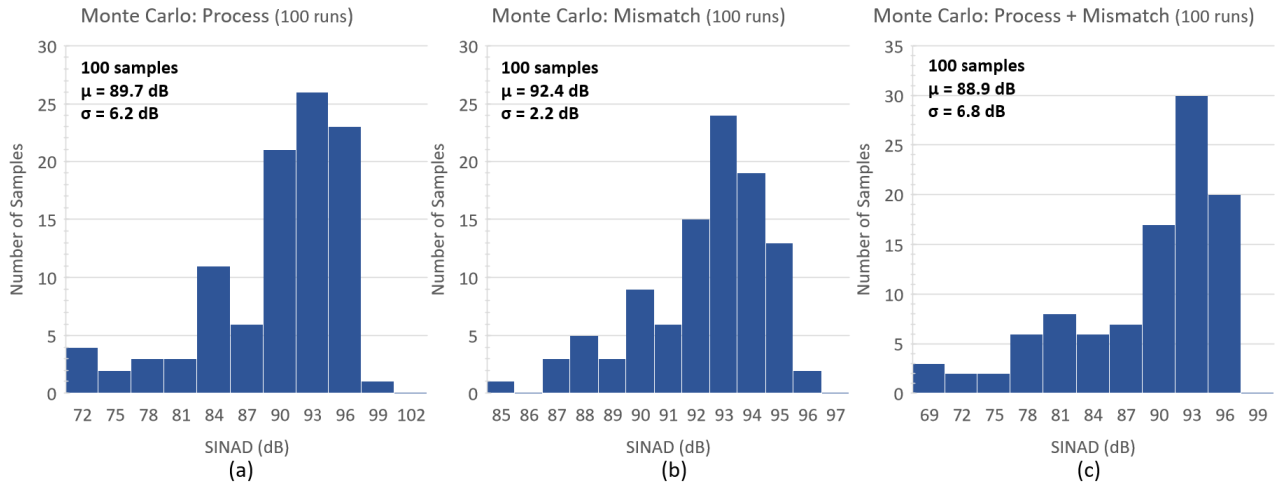


Figure 5.5: SINAD results of a 100-run Monte Carlo simulation considering (a) process, (b) mismatch and (c) process and mismatch variations.

Figure 5.6 shows the layout of the two bootstrapped switches, which occupied an area of $40\mu\text{m} \times 40\mu\text{m}$. The device and pin placement were such as to enable symmetry and to match the floorplan presented in Chapter 4.

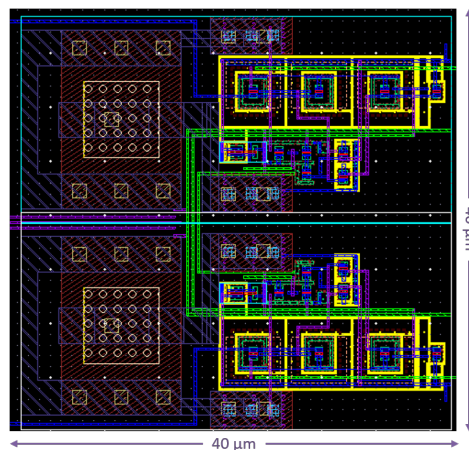


Figure 5.6: Layout of the two bootstrapped switches complying with the ADC floorplan.

Layout simulation resulted in the frequency spectrum of the differential output signal shown in Figure 5.7 (256-point FFT), alongside the reproduction of schematic result, for comparison. A reduction of 16 dB when compared to schematic is noticeable, yielding a $\text{SINAD} = 78\text{ dB}$. The inclusion of parasitics had a great impact on the non-linearity of the design, resulting in $\text{THD} = 0.012\%$. This performance, however, is still better than the schematic results obtained for the smaller switch.

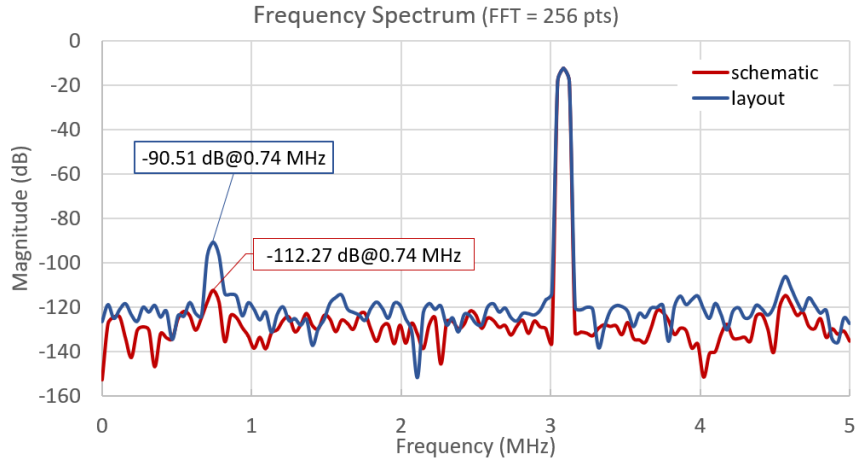


Figure 5.7: Frequency spectrum of differential output signal for schematic and layout.

Table 5.1 summarizes the results obtained in simulations with schematic and layout for the LP radio application.

Table 5.1: Simulation Results for the differential Bootstrapped Switch.

	Schematic	Layout	Units
SINAD	94.1	78	dB
THD	0.001	0.012	%
Current Consumption	170×2	177×2	nA

5.1.2 Comparator

As mentioned in the last chapter, the comparator analysis focused mainly on delay and power consumption, followed by a verification of offset and noise level.

The test bench created for delay estimate was also used for measuring the comparator metastability time-constant. The methodology for estimating the time-constant was based on the workshop of (CADENCE®, 2014). Since a dynamic comparator is a circuit without a static operating point, we can use a PSS Analysis to determine the periodic operating point, and then estimate the metastability time-constant.

The scheme of Figure 5.8 represents the test bench employed for this analysis, based on the methodology mentioned previously.

The comparator inputs were generated using an ideal balun with a pulse source at one of the inputs, and at the other input a dc source with the common mode level ($V_{cm} = VDD/2 = 0.5 V$). The goal of the pulse source is the measurement of time-constant and delay for the two possible comparator outputs. Another pulse source generates the comparator frequency,

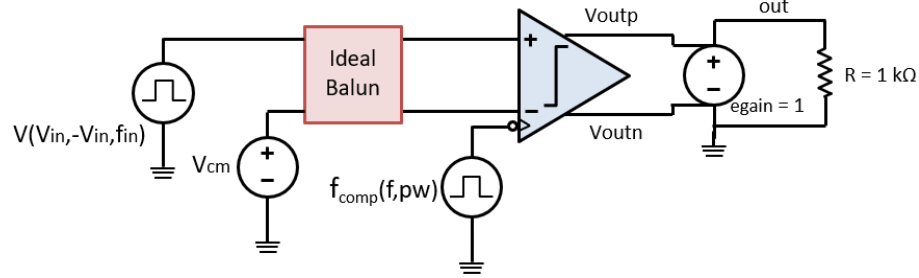


Figure 5.8: Test bench for comparator simulation and extraction of delay and comparator time-constant.

$f_{comp} = 100 \text{ MHz}$, with a pulse width, pw of $1/10$ (duty cycle of 10%), to emulate a narrower pulse width that occurs with the asynchronous logic.

To measure the dynamic comparator metastability, a small differential input V_{in} was set according to Figure 5.8, and the comparator latched. By monitoring the output waveform, and measuring the time for it to change from one voltage level V_x to $2.718 \times V_x$ ($e \times V_x$), the time-constant can be estimated (CADENCE®, 2014). Figure 5.9 represents the schematic results for a small input $V_{in} = 100 \mu\text{V}$ at $f_{in} = 10 \text{ MHz}$. The delays for the low and high transition of the differential output are illustrated in Figure 5.9.(a) and (b), respectively, and both correspond to 495 ps ($out = voutp - voutn$), with an average current consumption of $5.30 \mu\text{A}$. Figure 5.9.(c) and (c) shows the time-constant estimate for both situations, taken at the differential output. They both correspond to 28.6 ps .

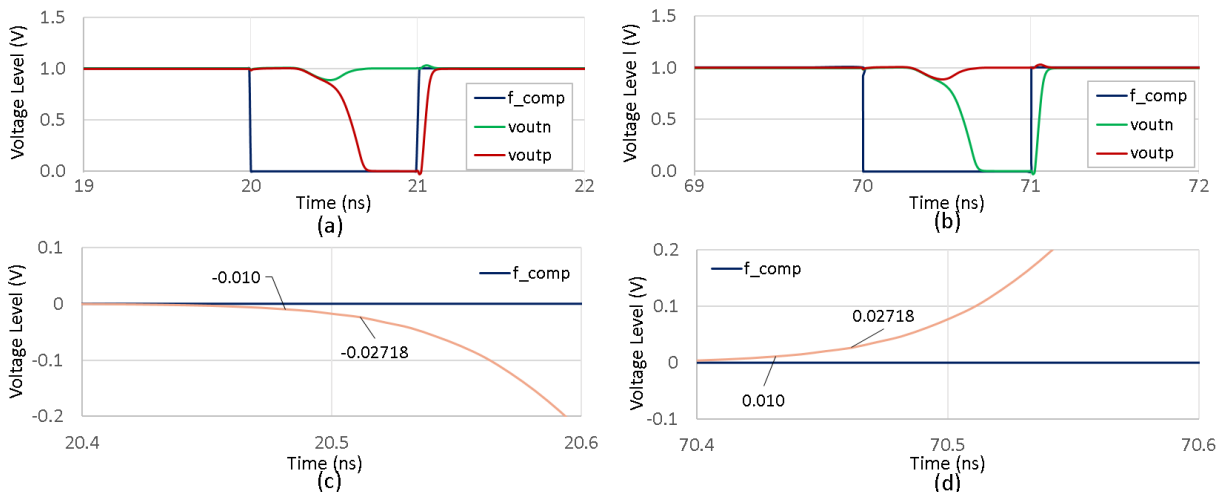


Figure 5.9: Delays for the (a) low and (b) high transition of the differential output, and methodology for estimating time-constant at (c) low and (d) high transitions of out .

Again according to the workshop, from the time-constant, the error probability can be calculated with equation 5.1, which allows the estimate of the bit error rate (BER).

$$P_{error} = \frac{2 * V_L}{Q_{step} * A_{UL}} e^{-\frac{t}{\tau}} \quad (5.1)$$

Where P_{error} is the error probability given in terms of probability of error/conversion; V_L is the minimum valid logic level the comparator must generate; Q_{step} is the step size at the input of the comparator, which is equivalent to LSB ; A_{UL} is the comparator's unlatched gain, which, for simplicity was considered the same as the strong arm latch without pre-amplifier, $A_{UL} = 1$; and t is the maximum time period the comparator has to make a decision, the evaluation-time, which is half of the operating period.

By looking at the expression 5.1, we can conclude that by increasing the operating frequency, or by narrowing the valid logic level, the probability of error increases. A higher gain reduces the probability of error. For $V_L = 80\% * V_{DD}$, $Q_{step} = 1 \text{ LSB} = 3.91 \text{ mV}$, $A_{UL} = 1$ and $t = 10 \text{ ns}/2$, P_{error} equals to 4.86×10^{-74} probability of error per conversion, which results in a $BER = 4.86 \times 10^{-66}$ bit errors per time.

Additionally, Figure 5.10.(a) shows the average delay of the comparator, at schematic level, taken by sweeping the differential input from $V_{in} = 100 \text{ uV}$ to $V_{in} = 0.5 \text{ V}$. As expected the delay increases as the differential input reduces, varying from 170 ps , when $V_{in} = 0.5 \text{ V}$, to 495 ps , when $V_{in} = 100 \text{ uV}$. For the ADC, this input should be limited to 1 LSB , thus considering a $V_{in} = 1 \text{ mV}$, the resulting delay is around 430 ps .

Likewise, the current consumption also grows with the reduction of V_{in} , since the comparator requires more time to generate a valid output. Figure 5.10.(b) illustrates the average current consumed by the comparator, varying from $2.96 \text{ }\mu\text{A}$, when $V_{in} = 0.5 \text{ V}$, to $5.30 \text{ }\mu\text{A}$, when $V_{in} = 100 \text{ uV}$. For the 1 mV differential input, the current consumed was $5.11 \text{ }\mu\text{A}$.

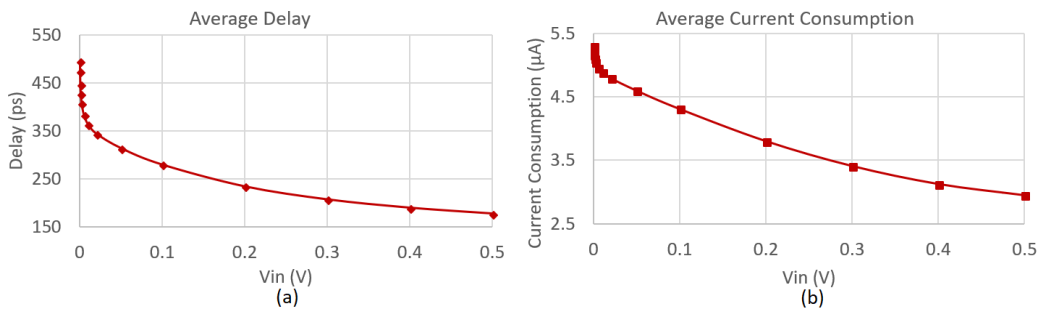


Figure 5.10: (a) Average delay and (b) average current consumption of the comparator as function of the differential comparator input.

The noise estimate also requires the PSS analysis to determine the periodic operating point and then proceed to a periodic small-signal noise analysis (PNoise) to define the noise contribution. Alternatively, a transient noise may be used for noise estimate, but for that, the Spectre Accelerated Parallel Simulator (APS) is needed. Access to APS at UFRGS is not possible; thus the estimation of noise employed the Pnoise analysis.

The test bench is similar to the one for delay in Figure 5.8, with a DC source at the input instead of a pulse source. This source was set as input noise source to evaluate the input-referred noise of the comparator. For a differential input $V_{in} = 1\text{ mV}$ and again with $f_{comp} = 100\text{ MHz}$, the input-referred noise resulted in $190\ \mu V_{rms}$, which is lower than the quantization noise of $400\ \mu V_{rms}$, estimated on section 4.2.1.

Figure 5.11.(a) and (b) present the input-referred noise as function of the differential input and the supply voltage, respectively. As can be seen, for inputs smaller than 2 mV , the noise contribution doesn't change much, which represents a lower limit for this comparator sizing, around $190\ \mu V_{rms}$. Additionally, in absolute value, a decrease in the power supply reduces noise; however, the dotted red line of Figure 5.11. (b) represents the ratio of noise and VDD which illustrates that the relative noise level increases with VDD reduction.

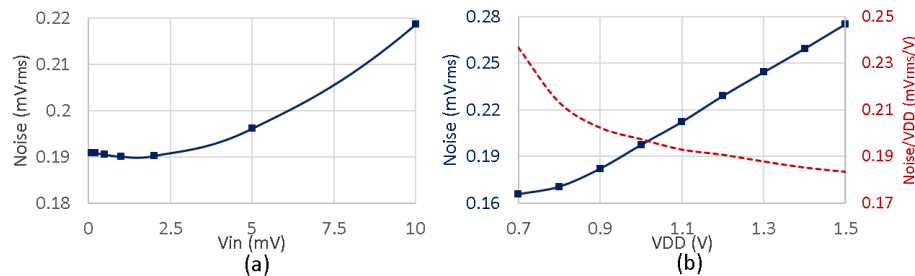


Figure 5.11: Comparator input-referred noise as a function of (a) V_{in} and (b) VDD .

Finally, the offset voltage of the comparator was evaluated using transient analysis. The test-bench, shown in Figure 5.12, is also similar to the one employed for delay measurement. At the input, there is also a pulse source, yet this time it is configured as a ramp with a rise time t_{rise} , half of the simulation time, and voltage levels from 10 mV to -10 mV .

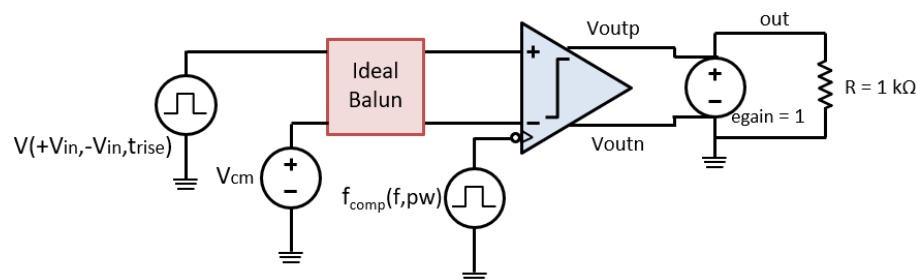


Figure 5.12: Test bench for comparator simulation and extraction of offset level.

Figure 5.13 shows the input and output waveforms that result from this test bench. The sampled input before and after the change of comparator results (from $out = 1$ to $out = -1$, and contrariwise) are saved, and the offset is defined as in the middle of this range of sampled inputs. For the schematic simulation, the sampled inputs were $+25 \mu V$ and $-25 \mu V$ for when $out = 1 \rightarrow -1$; and $-25 \mu V$ and $+25 \mu V$ for when $out = -1 \rightarrow 1$, which represents no offset.

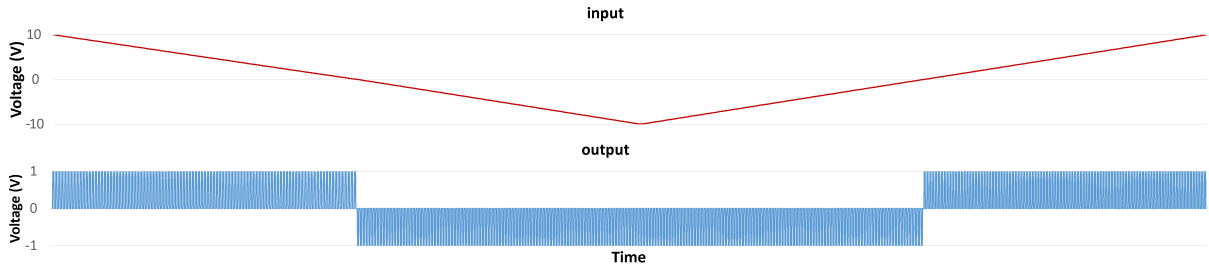


Figure 5.13: Input and output waveforms for offset extraction testbench.

A sweep of power supply showed that the offset result is maintained up until $VDD = 0.8 V$. A further reduction of VDD causes the comparator to not work correctly for this input level and not generate a valid output (V_{outp}/V_{outn} does not reach VDD or GND).

To better evaluate the offset, the spread caused by process (P) and mismatch (M) variations should be estimated. Figure 5.14 shows the results a 100-run Monte Carlo simulation, regarding mismatch variations, (Figure 5.14.(a)) and process and mismatch variations (Figure 5.14.(b)). Spread caused only by process variation did not influence negatively the offset ($\mu_P = 0$ and $\sigma_P < 1 \mu V$). However, when looking into mismatch variations, only 20 samples of 100 samples were within the $\pm 0.5 LSB$ limit (blue columns on the graph), with a standard deviation of almost two LSBs.

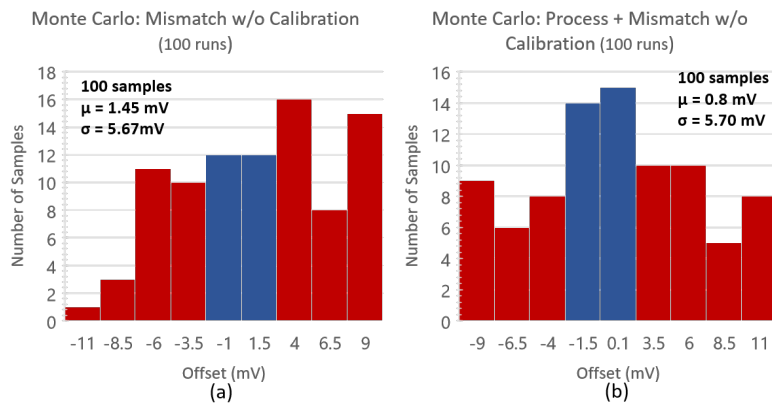


Figure 5.14: Offset results of a 100-run Monte Carlo simulation considering (a) mismatch and (b) process and mismatch variations.

The results considering both mismatch and process could not be much different from the one with only mismatch, but this time only 25 were within bounds. Although in this case the average was more centered ($\mu_{P+M} = 0.8 \text{ mV}$ when compared to $\mu_M = 1.45 \text{ mV}$) the spread was slightly larger.

A possibility for improving the comparator offset results is the implementation of calibration procedure. Mismatch unbalance occurs mainly because of the mismatch that is present at the input differential pair, impacting the response of the crossed-couple pair at the bottom. Thus, one of the possible calibration methods could be implemented by adjusting the current flow through internal nodes $intp$ or $intn$. Figure 5.15 shows ideally how this calibration could be implemented, with one ideal source connected to $intp$ and another to $intn$.

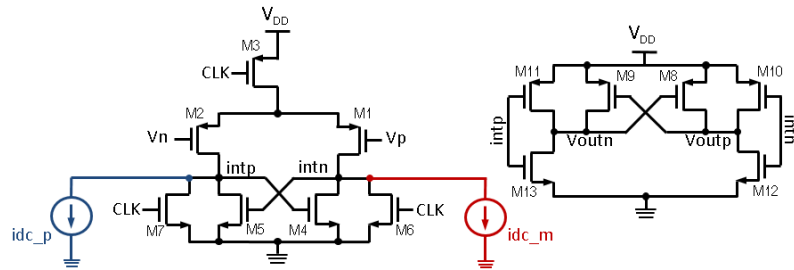


Figure 5.15: Calibration implemented in the comparator with the inclusion of two current sources in nodes $intp$ and $intn$.

Figure 5.16 shows the improvements obtained with this possible calibration, reducing significantly the spread caused by mismatch variations¹. Steps of 100 nA were considered, which still resulted in a spread, contrariwise that what is aimed when performing a calibration, where ideally the spread is zero. However, this spread is much inferior to 1 LSB , thus making it acceptable.

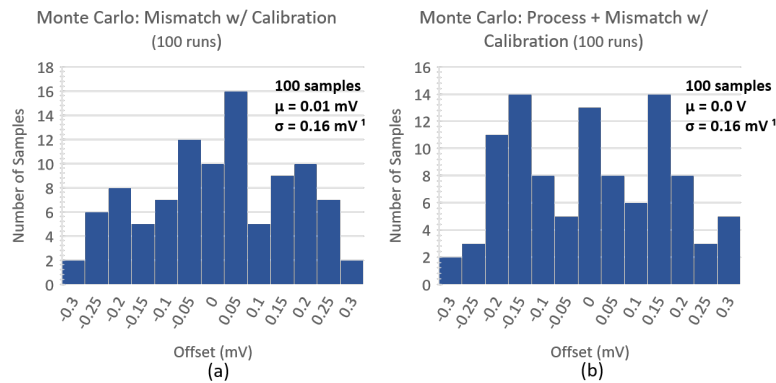


Figure 5.16: Calibrated offset results of a 100-run Monte Carlo simulation considering (a) mismatch and (b) process and mismatch variations.

¹The new σ does not represent a real statistical standard deviation, but a spread that resulted from the quantization of the calibration process. For simplicity, though, the term standard deviation and σ symbol is still used.

Although the average and variance resulting from Monte Carlo simulation of the comparator here presented are not very promising, its impact on the ADC ENOB, shown later on, was still within the margin given when for the ADC when its specifications were defined (a 1-bit margin).

Figure 5.17 shows the layout of the comparator, which occupied an area of $20\mu m \times 20\mu m$. Placement of devices and pins was such as to enable symmetry and to match the floorplan presented in Chapter 4.

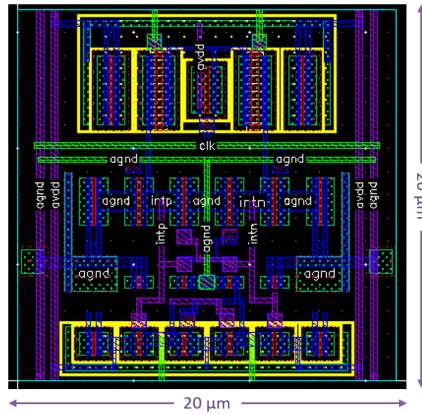


Figure 5.17: Layout of the comparator complying with the ADC floorplan.

Although symmetry was a strong consideration both in placement and routing of the comparator layout, the parasitics extraction from the resulting layout generated an imbalance in the comparator. For differential inputs lower than 1 mV , the comparator did not work correctly for the high transition (when *out* goes to 1). The 1 mV differential input, however, is still within the limit of the 0.5 LSB . Using the same calibration structure of Figure 5.15, it was possible to balance the comparator, by applying a current of 177 nA on node *intp*.

Figure 5.18 shows the delay for schematic, layout and calibrated layout with a differential input of 1 mV input, to enable comparison of delays. The *average delay* for schematic and calibrated layout were 430 ps and 520 ps , respectively, for the same 1 mV input, while the layout delay for high and low transition were 500 ps and 670 ps , respectively.

Figure 5.19 illustrates the average current consumed by the comparator, this time considering layout. As expected, the current consumed was slightly higher when compared to schematic, with a current of $5.34\mu A$, for the differential $V_{in} = 1\text{ mV}$, as opposed to the $5.11\mu A$ of the schematic.

The input-referred noise, on the other hand, was reduced at layout level, as illustrated in Figure 5.20. For a differential input $V_{in} = 1\text{ mV}$ and again with $f_{comp} = 100\text{ MHz}$, the input-referred noise resulted in $174\mu V_{rms}$.

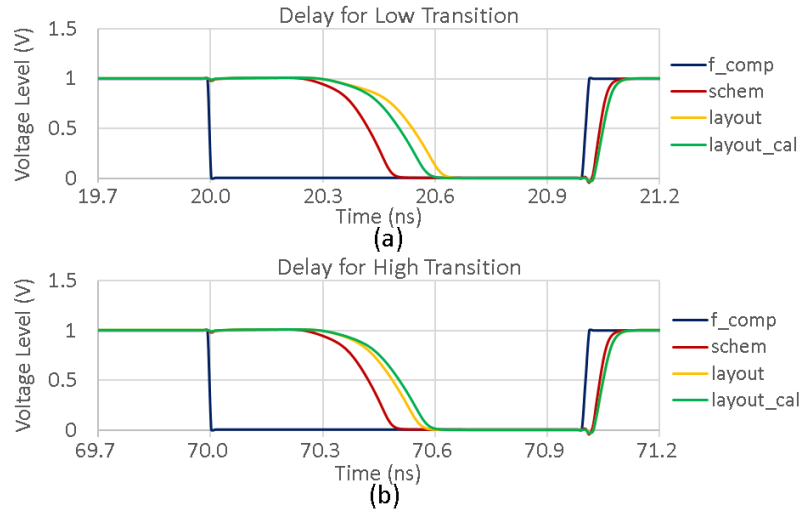


Figure 5.18: Delay for (a) low and (b) high transition of the comparator output, for schematic, layout and calibrated layout.

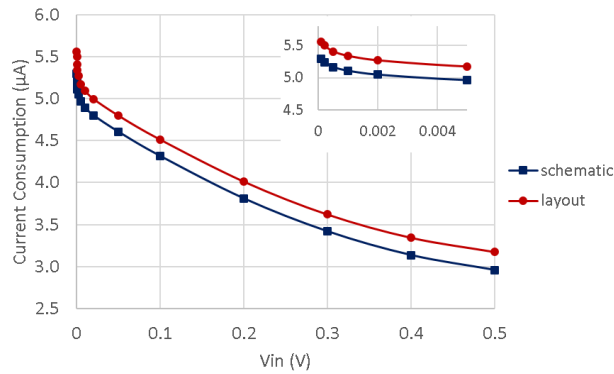


Figure 5.19: Average current consumption of the comparator as function of the differential comparator input, for schematic and layout.

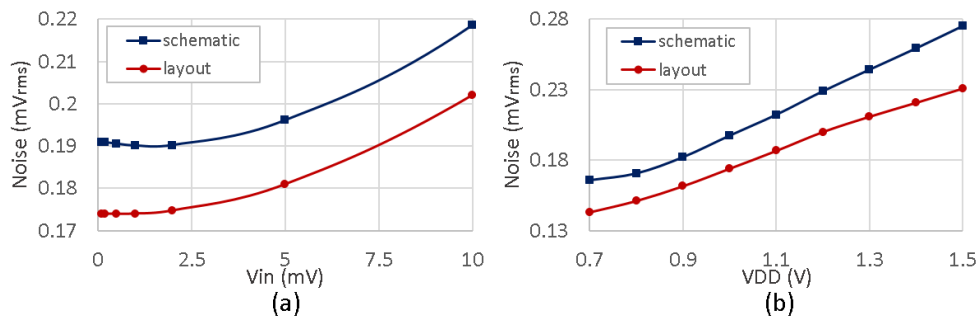


Figure 5.20: Comparator input-referred noise as a function of (a) V_{in} and (b) V_{DD} , for both schematic and layout.

Finally, the comparator was again tested for offset. For the layout simulation, the sampled inputs were -0.975 mV and -1.025 mV for both transitions of the output. The resulting offset of -1 mV is still within the $\pm 0.5 \text{ LSB}$ limit.

Table 5.2 summarizes the results obtained in simulations with schematic, layout and calibrated layout, for a differential $V_{in} = 1 \text{ mV}$ at $f_{in} = 10 \text{ MHz}$ and $f_{comp} = 100 \text{ MHz}$, with

a duty cycle of 10%. Table 5.2: Simulation Results for the Comparator.

	Schematic	Layout	Layout Calibrated	Units
Delay (av.)	430	500 _{high} /670 _{low}	522	ps
Time-constant (av.)	25	28.8 _{high} /33.0 _{low}	30.5	ps
Current Consumption	5.11	5.34	5.34	μA
Noise	190	174	174	μV_{rms}
Offset Level	< 0.025	-1.0	< 0.025	$m\text{V}$

5.1.3 SAR Logic

To illustrate the switching scheme implemented in Verilog-AMS, Figure 5.21 shows the waveforms of the switch controls, s_{ip} and s_{in} , where $i = 6 \dots 0$, along with $sleep$ and $done$ signals, and the internal counter.

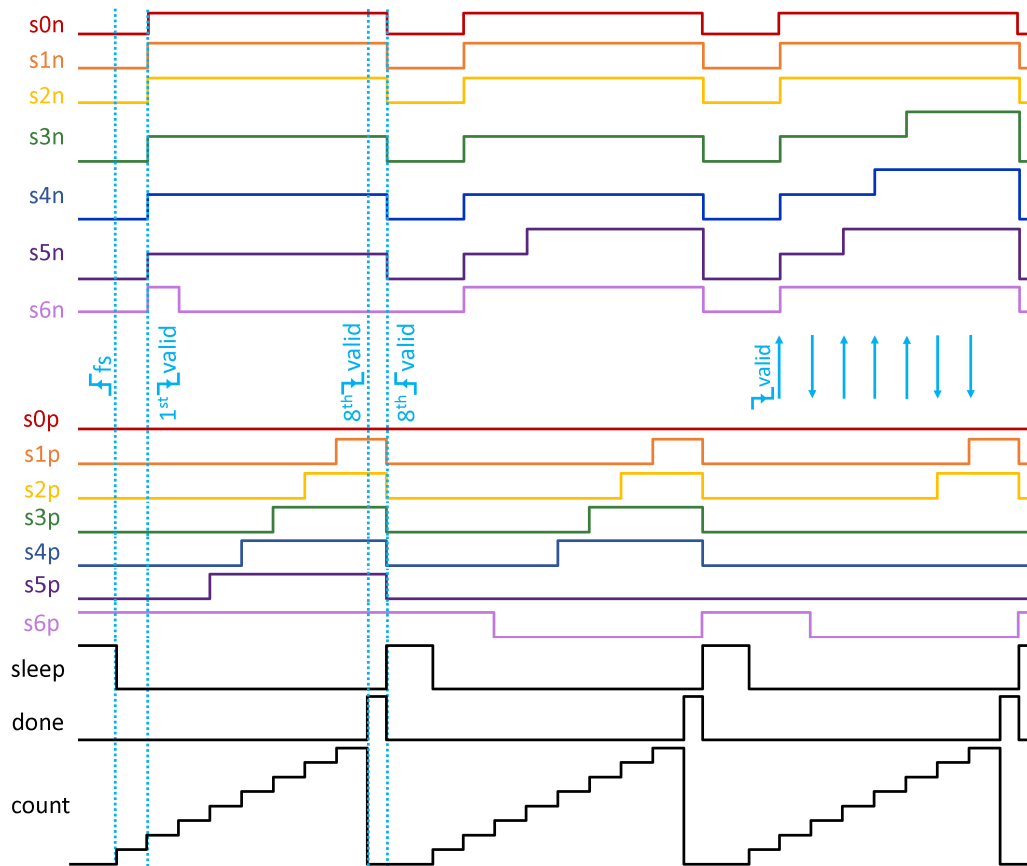


Figure 5.21: Illustration of switching procedure for $D_{out,1} = 1000000x$, $D_{out,2} = 1110000x$ and $D_{out,1} = 1111100x$.

The 1st vertical dotted line (from left to right of the image) indicates the rising-edge of f_S and down-transition of $sleep$, $count = 1$. At the down-transition from $valid$ (2nd vertical dotted line), the switching begins, represented by the change in state of all s_{in} , $count = 2$.

The 3rd vertical line indicates the last transition of *valid* from "1" to "0", in which the last comparison is stored, and D_{out} becomes available, as well as *done* goes to VDD . At the next rising edge from *valid* (4th vertical dotted line), *done* changes state and *sleep* goes to VDD . Finally, the blue arrows at the far right represent every switching.

For the three examples of conversion illustrated on Figure 5.21, digital outputs were $D_{out,1} = 1000000x$, $D_{out,2} = 1110000x$ and $D_{out,1} = 1111100x$. For these three examples, the DACn switches entirely on the 1st falling edge of *valid*. Three levels are visible for $s5n$, $s4n$ and $s3n$, representing the three reference levels of Figure 4.11; for $s6n$, the two levels visible represent V_{cm} and V_{refp} ; finally, for all the remaining controls, the two levels represent V_{refn} and V_{cm} .

5.1.4 Delay Cell

Before proceeding to the A/D Converter results, it is important to highlight the impact of the delay cell on the asynchronous logic and consequently on the converter as a whole, since it defines $t_{SAR} + t_{DAC}$.

As it was mentioned previously, the delay cell consists basically of a *buffer* for which output delays for up- and down-transition differ, the latter being controlled by *vbias*. Figure 5.22 illustrates the behavior of the delay cell, with a delay set around 9 ns for $vbias = 320 mV$.

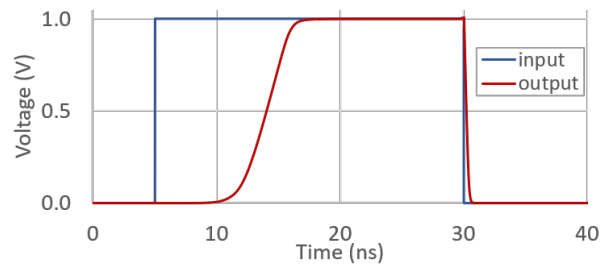


Figure 5.22: Input and output waveforms of the delay cell.

This delay is defined based on the absolute value of *vbias* and, thus, any variation on the expected response would have a significant impact on the ADC, since it impacts $t_{SAR} + t_{DAC}$, and consequently t_{cycle} . The main issue would occur when the resulting delay is large to such an extent that it doesn't allow the state machine to reach the final comparison, and thus generate D_{out} . Therefore, the design of this delay cell should be very robust to process and mismatch variations. Another possibility is making the *vbias* control as one of the external inputs that feed the A/D Converter, which is the case in this work.

5.2 ADC Results

Having presented the results for the individual blocks, we now proceed with the results of the A/D Converter itself. First, the results from the dynamic test bench are presented, followed by those obtained from the static test bench. For improving the presentation and analysis of results, the physical layout is placed in the dynamic results section, which also includes the performance exploration of ADC design presented in Chapter 4.

5.2.1 Dynamic Results

Similarly to the bootstrapped switch analysis, a frequency domain representation of the output signal is necessary for estimating the dynamic metrics. Figure 5.23 illustrates the test bench created for the ADC dynamic characterization, with parameters defined according to the low power radio application, depicted in Table 5.3. The reference levels, V_{refp} , V_{cm} , V_{refn} , are ideal sources.

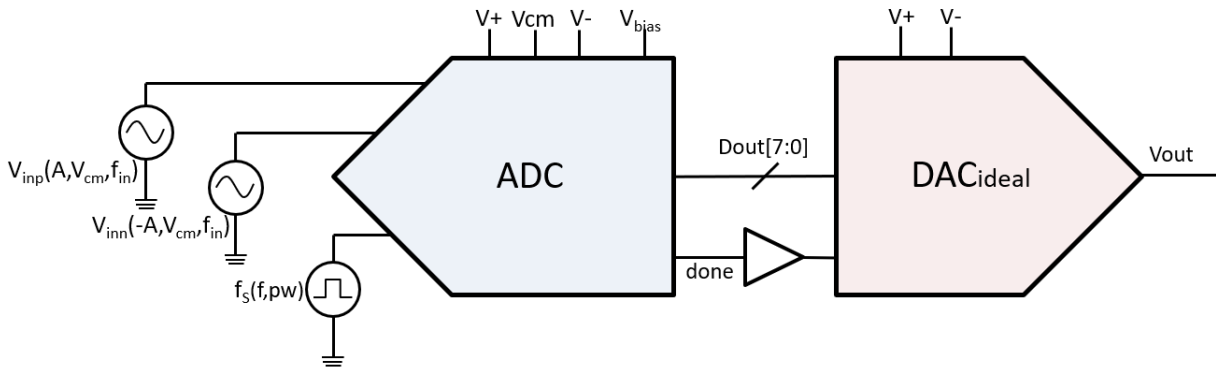


Figure 5.23: A/D Converter test bench for extraction of dynamic metrics.

Table 5.3: Dynamic Test Bench Parameters for ADC simulation

Amplitude	A	250	mV
DC Level (ideal)	V_{cm}	500	mV
V_{refp} / V_{refn} (ideal)	V+ / V-	750 / 250	mV
Sampling Frequency	f_S	10	MHz
Duty Cycle	pw	10%	-
Input Frequency	f_{in}	near 3	MHz
Supply Voltage	V_{DD}	1	V

Figure 5.24 shows the simulated frequency spectrum (512-point FFT) of the output signal $vout$, with $C_u = 30 \text{ fF}$ and $f_{in} = 2.988 \text{ MHz}$, defined complying with coherent sampling. The schematic simulation resulted in a $SINAD = 48.6 \text{ dB}$, which represents an

$ENOB = 7.78$ bits. $SFDR$ and THD were also extracted, and corresponded to 61.84 dB and 0.006% , respectively.

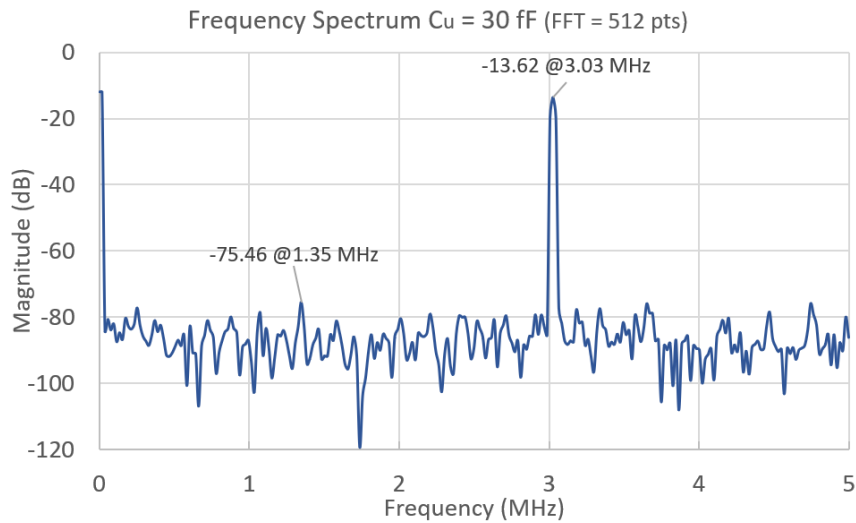


Figure 5.24: Frequency spectrum of output signal for ADC at schematic level.

The total average current consumed from the power supply was $18\mu A$, with bootstrapped switches consuming 2×177 nA, the comparator, $2.12\mu A$, and DACs $2 \times 3.82\mu A$. The percentage of current consumption for the three main blocks is illustrated in Figure 5.25.(a). The asynchronous logic, which includes the logic gates shown in Figure 4.9 and also additional buffers, accounted for a significant parcel of the total current, $7.86\mu A$, as illustrated in Figure 5.25.(b). The delay cell by itself consumed $2.66\mu A$.

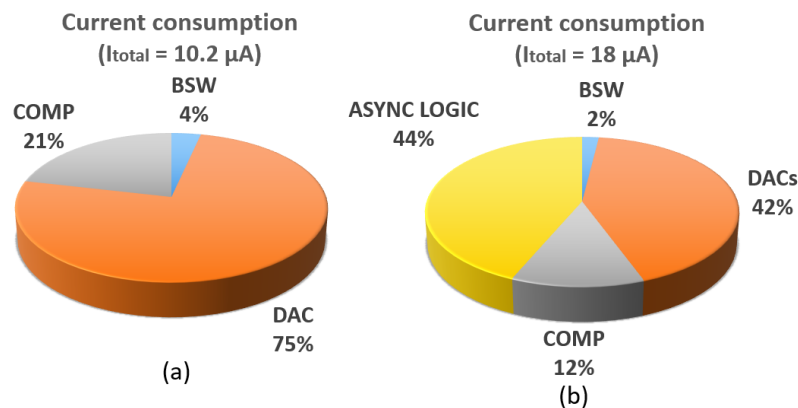


Figure 5.25: Current consumed per block (a) when only the three main blocks are considered, (b) and including the asynchronous logic.

It is important to mention that while the standard cells employed in this project were also part of the circuits designed, their implementation was not optimized regarding power consumption. A custom optimized design could potentially reduce the contribution of the asynchronous logic to the total current consumed.

Still on the topic of power consumption, one of the disadvantages of the OSSI-HBSI switching implemented in this project was the energy necessary for the reset step. To illustrate that, the average current consumed at each complete ADC conversion, for a series of inputs, was taken both considering the reset step and excluding it, which amounted for $14.7 \mu A$ and $12.5 \mu A$, respectively. While those values are not strictly accurate since they were taken considering the middle range of falling and rising edges of f_S and $done$ signals, respectively, the additional power consumed with the inclusion of the reset represents 15% of the total power, which is indeed a significant parcel.

An entire conversion step lasts $80 ns$, considering the start of the conversion (rising edge of f_S) and the end of the conversion, which includes reset of switches (falling edge of $done$). To estimate the average comparison time, the delay between each f_{comp} and $valid$ signal was taken for three input levels, $V_{inp} \gg V_{inn}$, $V_{inp} \approx V_{inn}$ and $V_{inp} \ll V_{inn}$. Those delays are gathered in Table 5.2.

Table 5.4: Dynamic Test Bench Parameters for ADC simulation

input	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	Average	Units
$V_{inp} \gg V_{inn}$	0.36	0.55	0.59	0.70	0.84	0.87	1.14	0.94	0.75	ns
$V_{inp} \approx V_{inn}$	0.56	0.49	0.50	0.63	0.76	0.87	1.01	0.96	0.73	ns
$V_{inp} \ll V_{inn}$	0.35	0.54	0.58	0.72	0.82	0.89	0.99	0.98	0.73	ns

In general, the delays increase as the dynamic range of the comparator decreases, as it was expected with the convergence resulting from the binary search. Therefore, the last comparisons have a larger delay than the first comparisons. Additionally, for the differential input close to zero $V_{inp} \approx V_{inn}$, the delay of the 1st comparison is almost twice the value of the other two input combinations. This larger delay was expected since the differential input at the comparator is small, but after the first comparison, a voltage shift of $V_{ref}/2$ occurs in one of the comparator inputs, which results in a shorter delay for the 2nd comparison.

The average $t_{comp} = 0.75 ns$ and the $9 ns$ defined for $t_{SAR} + t_{DAC}$ by the delay cell result in an average t_{cycle} slightly inferior to $10 ns$. This t_{cycle} is within the margin considered while defining the DAC array switches where a total of 10 cycles of $10 ns$ was considered for simplicity.

Although in Table 5.3, only f_{in} near $3 MHz$ is explicit, the LP radio application includes a bandwidth of $2 MHz$, for which a center frequency of $3 MHz$ was defined in Chapter 2 (intermediate frequency for the Low-IF architecture). Therefore, for correct characterization of the converter, a sweep on the input frequency is necessary. Furthermore, in the characterization

of Nyquist converters, typically the dynamic metrics are estimated for a near-Nyquist frequency. With that in mind, Figure 5.26 shows the estimate of ENOB and THD for a sweep of input frequencies spanning from 2 MHz to near 5 MHz.

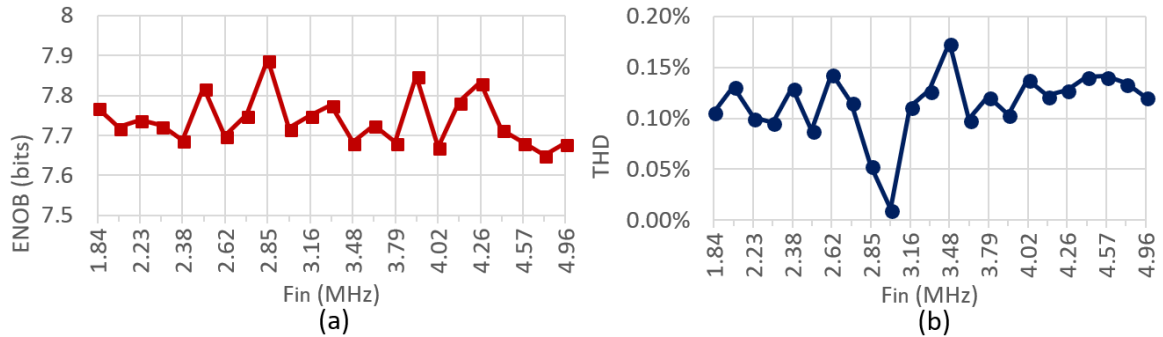


Figure 5.26: (a) ENOB and (b) THD results considering a sweep of the input frequency.

Figure 5.27 represents a sweep over temperature, for a range from 0 °C to 80 °C. For the v_{bias} considered so far, equal to 320 mV, the effective number of bits reduces to 7.3 around 70-80 °C. By increasing v_{bias} and thus reducing $t_{SAR} + t_{DAC}$, this effect is less perceptible. On the other hand, the smaller $t_{SAR} + t_{DAC}$ becomes critical for lower temperatures, causing the asynchronous logic to not work properly with the SAR state machine. For that reason, with $v_{bias} = 340$ mV for instance, a error was generated on the ENOB estimate for the range 0-10 °C. For the range between 20-60 °C and for all three v_{bias} illustrated on Figure 5.27, the ENOB was greater than 7.6 bits.

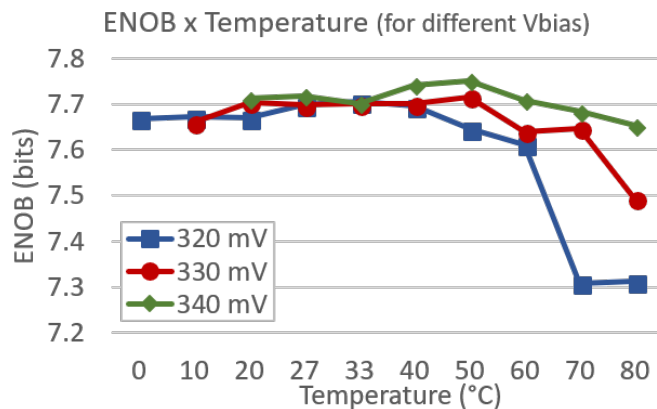


Figure 5.27: ENOB results for a temperature sweep, considering different values of v_{bias} .

To better evaluate the statistical spread, we must again run Monte Carlo simulations. While for previous situations, both bootstrapped switch, and comparator, this step could be performed straightforwardly, because simulations were faster and did not occupy much disk space, that is not the case for the entire ADC. A 256-point FFT simulation with most circuits at schematic level and state machine described in Verilog-AMS lasts around 4 hours and occupies

approximately 4 GB. Therefore, multiple Monte Carlos steps, with different seeds, had to be considered to generate the final 50 samples the will be presented next.

Figure 5.28 shows the results for all three situations, process, mismatch and the combination of both. In all cases, the average was above $\mu = 7.7$ bits, with a maximum standard deviation of $\sigma = 0.06$ bits. This combination still corresponds to a very promising result, considering the 1-bit margin given when defining the ADC specifications for the LP radio application. In view of these results, the calibration suggested for the comparator was not further investigated and implemented.

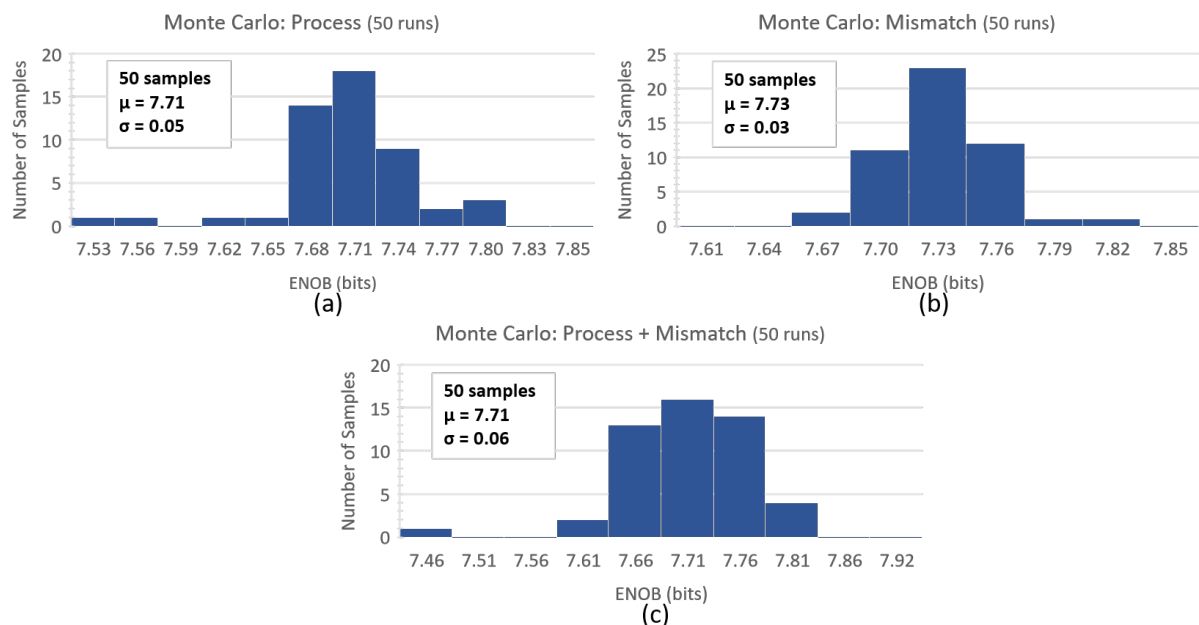


Figure 5.28: ENOB results of a 50-run Monte Carlo simulation considering (a) process, (b) mismatch and (c) process and mismatch variations.

5.2.2 Physical Design

Figure 5.29.(a) presents the layout of the DAC, with its capacitive array and multiples switches, occupying a total area of $190 \mu m \times 190 \mu m$.

The position of the switches considered that in the floorplan presented in Chapter 4 the SAR state machine will be placed at the right side of the DAC. Placement and routing of the capacitors employed the common-centroid technique as well as the addition of dummy structures.

The final layout of Figure 5.29.(b) includes the two bootstrapped switches, the comparator, and the two DACs. It occupied an area of $190 \mu m \times 420 \mu m$, with enough free area in the middle for the asynchronous logic layout.

As mentioned previously, the standard cells employed in this design were also part of the design, but only at the schematic level and not at the physical level. Therefore, the layout simulations presented henceforth did not include the asynchronous logic at the layout level, only the layout blocks presented so far.

Figure 5.30 shows the simulated frequency spectrum (512-point FFT) of the output signal v_{out} , again with $f_{in} = 2.988 MHz$ and $C_u = 30 fF$, for both schematic and layout. The layout simulation resulted in a $SINAD = 47.3 dB$, which represents an $ENOB = 7.57$ bits. $SFDR$ and THD corresponded to $58.43 dB$ and 0.02% , respectively.

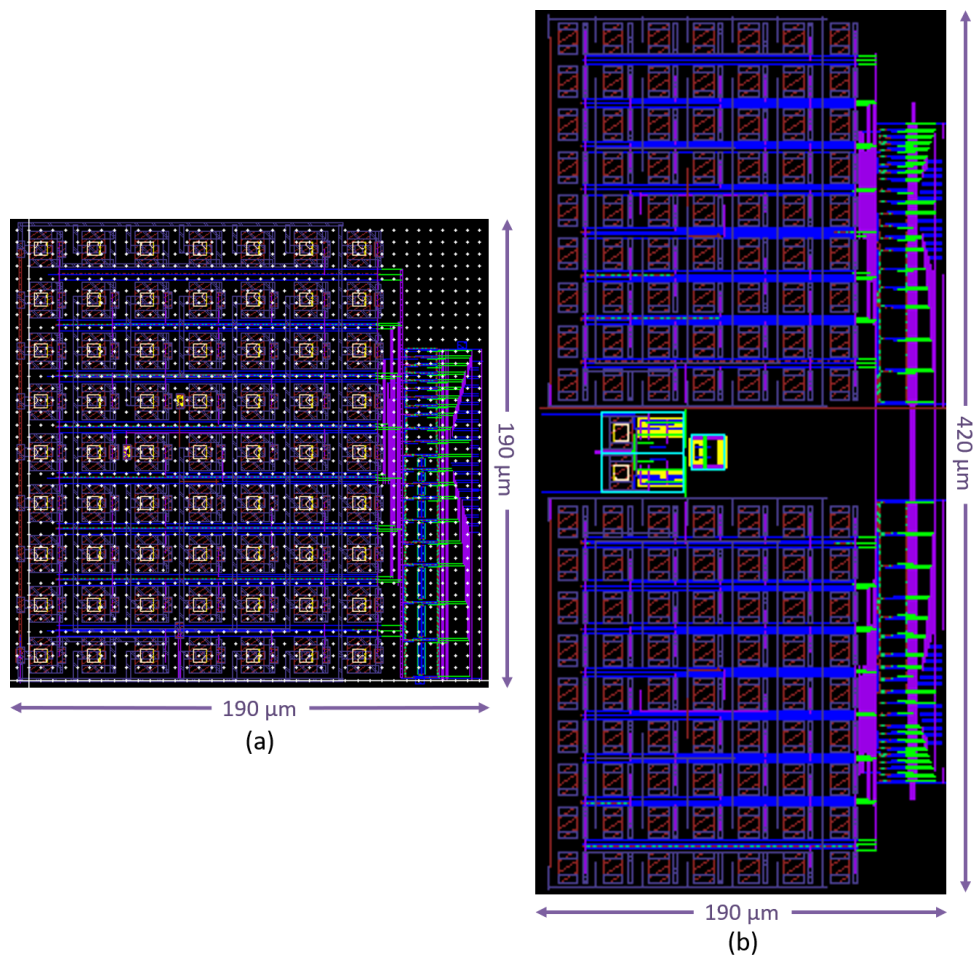


Figure 5.29: (a) DAC layout, complying with the ADC floorplan; (b) ADC layout, including bootstrapped switches, comparador and DACs, also complying with the floorplan presented earlier.

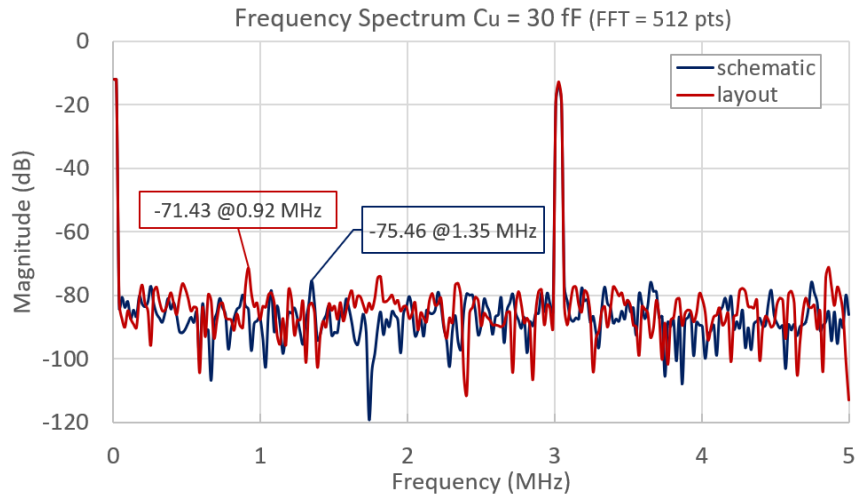


Figure 5.30: Frequency spectrum of output signal for ADC at both schematic and layout level.

The total average current consumed from the power supply was $21 \mu A$, with sampling switches consuming $2 \times 240 nA$, the comparator, $2.98 \mu A$, and DACs $2 \times 4.67 \mu A$. The asynchronous logic accounted for a total average current of $8.21 \mu A$. Table 5.5 summarizes the ADC performance results for both schematic and layout.

Table 5.5: Simulation Results for the A/D Converter.

	Schematic	Layout	Units
SINAD	48.63	47.3	<i>dB</i>
ENOB	7.76	7.57	<i>bits</i>
THD	0.006	0.02	<i>%</i>
Current Consumption (av.)	18	21	μA

Finally, dynamic metrics were estimated at layout level considering a sweep of the input frequency. Figure 5.31 shows the results of both schematic and layout.

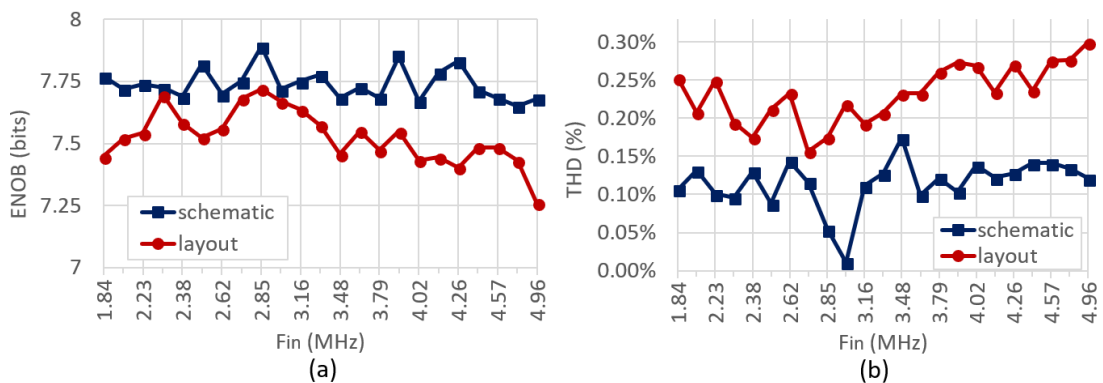


Figure 5.31: (a) ENOB and (b) THD results considering a sweep of the input frequency for both schematic and layout.

5.2.2.1 Exploring DAC topology

The exploration of DAC topology is related to the C_{unit} used in the design and, consequently, to the total equivalent capacitance. On Chapter 4, when the unit capacitance was defined, three scenarios were raised: in one $C_{unit} = 15 \text{ fF}$, generated by setting four C_{min} in series, with $C_{eq} = 960 \text{ fF}$; on another $C_{unit} = 30 \text{ fF}$, this time using two C_{min} in series with $C_{eq} = 1.92 \text{ pF}$; finally using $C_{unit} = C_{min} = 60 \text{ fF}$, with $C_{eq} = 3.84 \text{ pF}$.

Figure 5.32 represents the simulation with an input frequency sweep for all three scenarios. By looking at Figure 5.32.(a), for both $C_{unit} = 15 \text{ fF}$ and $C_{unit} = 30 \text{ fF}$, the resolution did not fall below 7.5 bits ; however, a significant variation of ENOB is present when $C_{unit} = 60 \text{ fF}$, over a range of 7.5 bits to 6.2 bits .

One of the main reasons for this variation lies on the nonlinearity introduced by the bootstrapped switch employed for sampling. If we recall, for $f_{in} = 3 \text{ MHz}$, $SINAD_{BSW,15f}$ and $SINAD_{BSW,30f}$ were greater than 90 dB while $SINAD_{BSW,60f} \approx 50 \text{ dB}$. At $F_{Ny} \approx 5 \text{ MHz}$, $SINAD_{BSW,60f}$ decreased even further, close to 40 dB , while the other two were still greater than 75 dB . This degrading effect on the topology with $C_{unit} = 60 \text{ fF}$ is reflected on the THD results illustrated on Figure 5.32.(b).

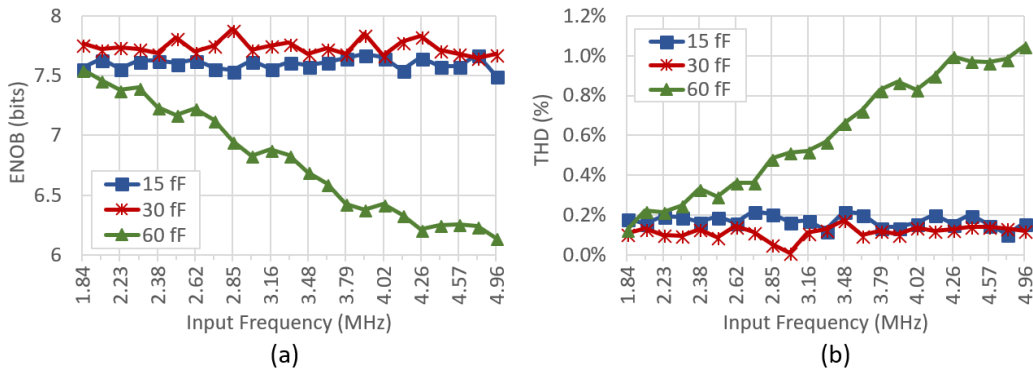


Figure 5.32: (a) ENOB and (b) THD results considering a sweep of the input frequency for the three DAC topologies, with different C_{unit} .

The different topologies however did not generate any differences regarding the power consumed, as it is illustrated on Figure 5.33.(a), with $I_{ADC} = 10.2 \mu\text{A}$, without asynchronous logic ($I_{ADC,all} = 18 \mu\text{A}$). The current consumption estimate considered so far was taken from the ADC power supply. If we look at the current supplied by the references, which consisted of ideal sources, it can be seen that there is a significant increase when the total C_{eq} is augmented, $I_{ref,15f} = 18.3 \mu\text{A}$, $I_{ref,30f} = 21.5 \mu\text{A}$, $I_{ref,60f} = 28.6 \mu\text{A}$. Figure 5.34 shows the percentage of current consumed per each block and per reference.

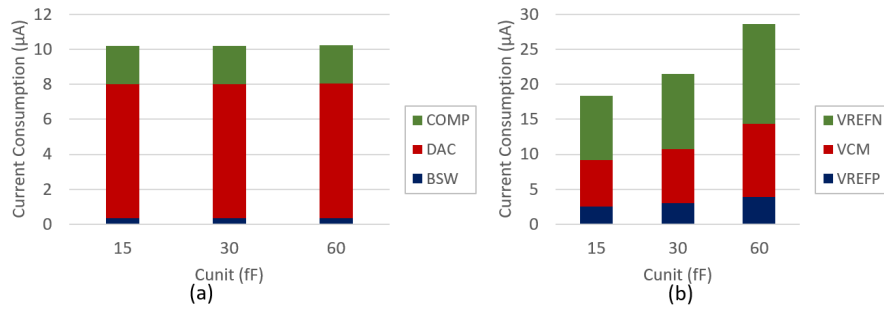


Figure 5.33: Current consumed versus C_{unit} , considering: (a) every block of the ADC and (b) the three references employed.

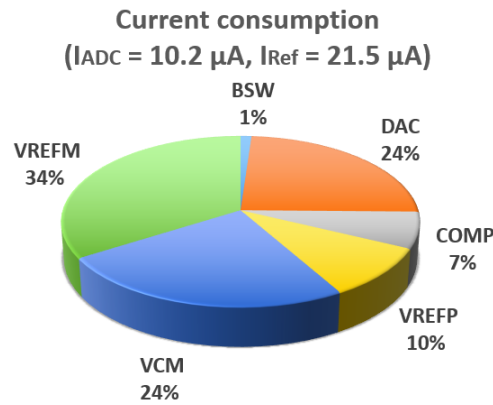


Figure 5.34: Percentage of current consumption per block and per reference, for the LP radio application ($C_{unit} = 30 \text{ fF}$, $f_{in} \approx 3 \text{ MHz}$ and $f_S = 10 \text{ MHz}$).

At this stage, it is interesting to raise a brief discussion regarding the manner in which the power consumed by the DAC arrays appears in the literature. From most of the works studied and outlined in Chapter 3, the current consumption informed was not explicitly considering the references which, as showed in Figure 5.34, represents a significant parcel of the power consumed in the ADC. While it is true that in many situations the reference is the power supply, V_{DD} and GND , in many others additional works are also present, and if not highlighted, there is no certainty as to what is taken into consideration.

For instance, in this work, if the current consumed by DAC arrays considers not only that from the input signals, buffers and switches activation, but also the references, the DAC power parcel increases to 92%, as opposed to the 24% shown on the pie chart of Figure 5.34. Since the information of current consumption often appears as if supplied by V_{DD} , also in the current work this will be considered and thus, the DACs contribution to the total current consumed does not include the references.

5.2.2.2 Exploring Sampling Frequency Limits

The same input frequency sweep presented earlier was done for the ADC with different sampling rates, with some reservations. The sampling frequencies considered were the same applied to the bootstrapped switch, $f_S = 10 \text{ MHz}$, 15 MHz , 20 MHz , 32 MHz . For each one, the LP radio application was taken into account ($f_{in} = 2 \text{ MHz}$ to 4 MHz), as well as f_{Ny} , which are distinct in each case. Again, a 256-point FFT was taken, and coherent sampling considered. Figure 5.35.(a) shows the resulting ENOB for each situation.

An increase in the sampling rate has a direct impact on the available time for each cycle ($t_{DAC} + t_{SAR} + t_{comp}$). The delay controlled by the delay cell, which accounts for $t_{DAC} + t_{SAR}$, was reduced for the different f_S ($d_{10M} = 9 \text{ ns}$, $d_{15M} = 6 \text{ ns}$, $d_{20M} = 4.5 \text{ ns}$, $d_{32M} = 2.9 \text{ ns}$).

The resolution of up to $f_S = 20 \text{ MHz}$ could be looked at as the limit if only the application bandwidth is considered. However, the delay reduction may be a source of errors when simulating the SAR logic at transistor level, and not at behavioral description any longer.

Taking the entire range of input frequencies, up to f_{Ny} , the variation of ENOB is too significant for the scenario with $f_S = 20 \text{ MHz}$ to be considered suitable. Moreover, considerable degradation of ENOB for $f_S = 32 \text{ MHz}$ was already expected due to the SINAD results from the bootstrapped switches alone, even for the input frequency range from 2 MHz to 4 MHz . Along with ENOB, Figure 5.35 shows the current consumed in each case (with $f_{in} \approx 3 \text{ MHz}$).

This exploration of a superior limit for the current ADC regarding sampling frequency did not aim reduction of power consumption since an increase of f_S augments the current consumed by every block, as it is shown in Figure 5.35.(b). For that purpose, an exploration of inferior limit would be more interesting. However, the bandwidth of the LP radio application already implicates on this inferior limit, which would be around the selected sampling frequency of $f_S = 10 \text{ MHz}$.

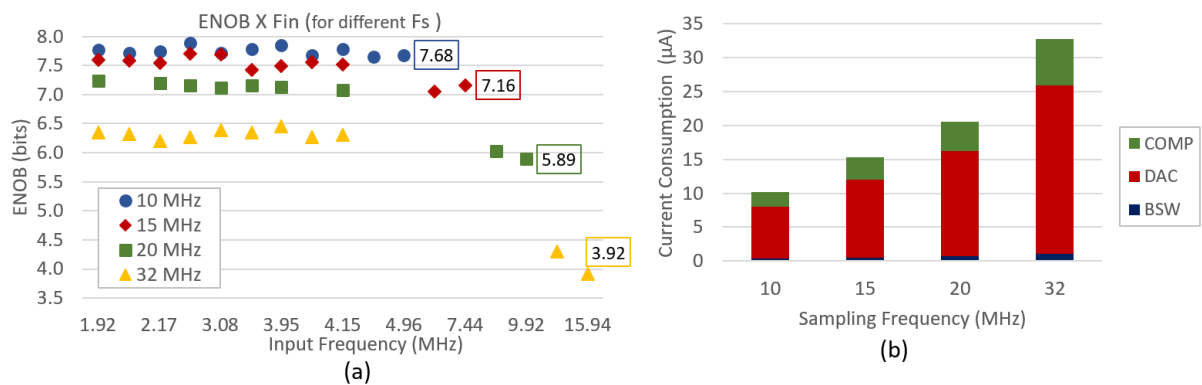


Figure 5.35: (a) ENOB results considering a sweep of the input frequency for the different f_S and (b) Current consumed versus f_S every block of the ADC.

5.2.3 Static Results

For extraction of static metrics, the test bench of Figure 5.36 was implemented. Similarly to the one used for the offset estimate for the comparator, ramps were generated at the ADC inputs, using pulse sources with a great t_{rise} . The input was swept between positive and negative levels, reversely, so that the entire dynamic range was considered. Again, $f_S = 10\text{ MHz}$ with a duty cycle of 10%, set by pw .

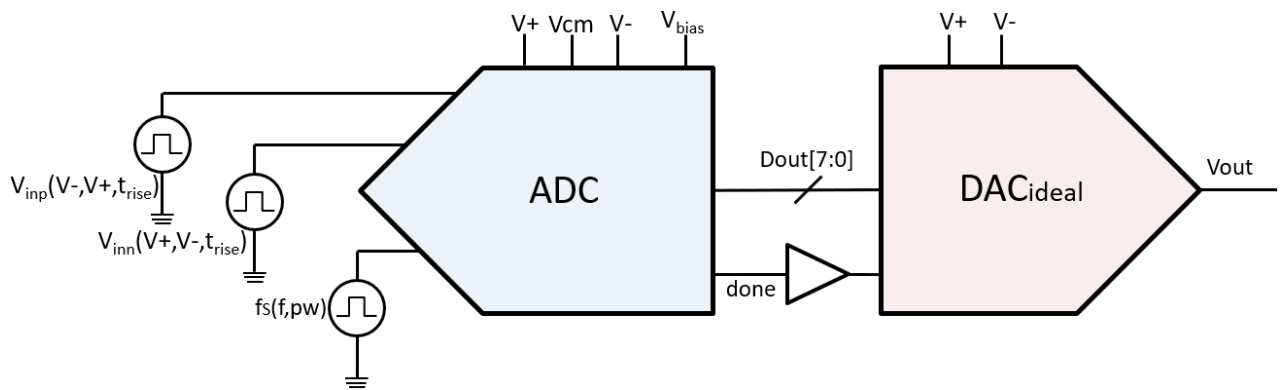


Figure 5.36: A/D Converter test bench for extraction of static metrics.

As usual in the design of analog circuits, there is a trade-off between the precision of the simulation results and the simulation time and the hard drive resources required. Remember that a range of analog inputs, that corresponds ideally to an LSB-span, results in a digital D_{out} word. By sampling the input ramp only once for each D_{out} , the resulting DNL will have a precision of 1 *LSB*. A non-linear error in such a scenario may reflect in a wrongly evaluated missing code, due to this single input sample. If the input ramp is sampled twice or four times for each D_{out} though, the precision of that DNL result will fall under 0.5 *LSB* or 0.25 *LSB*, respectively. The wrong evaluation of a missing code is illustrated in Figure 5.37 where the $D_{out} = 101_b = 5_d$ was skipped for 1x-sampling and not for 4x-sampling.

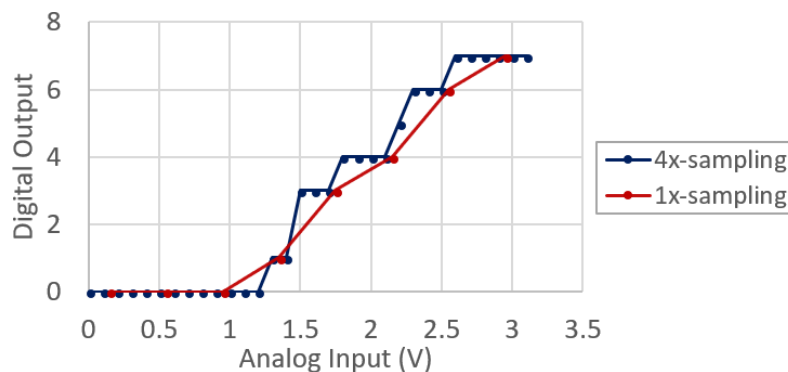


Figure 5.37: Illustration of 1x-sampling, resulting in a missing code, and 4x-sampling.

This ramp with more samples will also enable a more precise INL result. The INL can be estimated in different ways: using as reference the ideal ADC curve, but that will include gain and offset errors on the INL estimate; or using a reference that removes gain and offset errors, yet that also will include great deviation errors that occur between first and last D_{out} ; or by using as reference the curve that fits best the resulting output waveform, which is the option considered in this work. The effect of taking more samples means that this curve will more accurately fit the resulting output waveform.

The three different methods for estimating INL are illustrated in Figure 5.38. The green curve corresponds to a hypothetical real output waveform, which also includes offset error. The blue and red curves correspond to the ideal output waveform without any errors and including the same offset error as the green one. The dotted lines correspond to the three references mentioned in the last paragraph, blue for ideal ADC output, red for ideal ADC with offset correction and green for the best fit to the real ADC output.

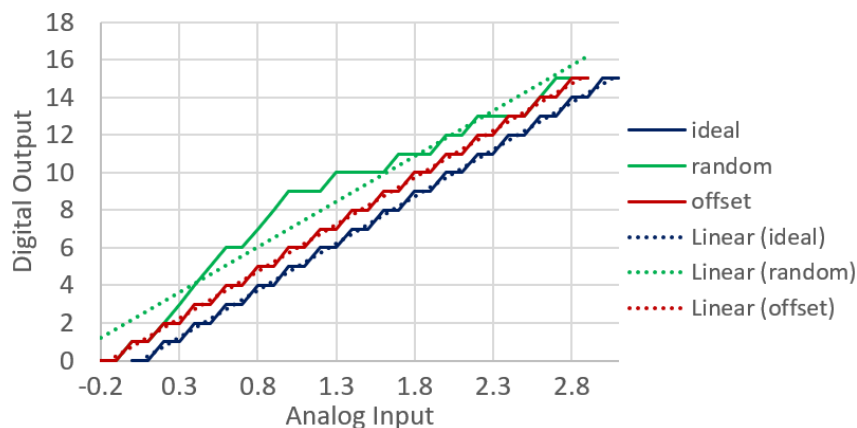


Figure 5.38: Methods for estimating INL, for three different references: the 1st taken from the ideal ADC's response (blue dotted curve); the 2nd, removing offset and gain errors (red dotted curve); and the 3rd from the curve that best fits the ADC's response (green dotted line).

A direct consequence of two samples per D_{out} is the augmented simulation time, since the input ramp will need to include two conversions for each D_{out} (at least 200 ns for one single D_{out} with $f_S = 10\text{ MHz}$), and twice the disk space. Additionally, for the converter under test, with an 8-bit resolution, a total of $2^8 = 256$ digital words should be, ideally, tested, which entails in a minimum simulation time of $51.2\ \mu\text{s}$. Ergo, the simulation time can increase quite fast with an increase of resolution or with more precise results.

Typically, a few input levels that correspond to the worst cases of DNL and INL of the switching scheme are selected. Evaluation of static nonlinearity through simulation considers, then, only this smaller scenario, while for measurements of the prototype the entire range is

taken into account. Since this work does not include a fabrication in this stage, the entire input range was considered for the ADC characterization.

Considering the discussion raised in the last paragraphs, a precision of 0.25 LSB was selected for the DNL, which corresponds to a 4-time sampling of the input ramp for the same ideal D_{out} . The simulation time for that is at least $102.4 \mu\text{s}$, which corresponded to around 12 h and close to 20 GB in space disk for schematic, and more than a day and 50 GB of disk space for the extracted layout.

Exploration of the DAC topologies, with the different unit capacitors, was also done for linearity measurements at the schematic level.

Figure 5.39 shows the simulated INL results, for the LP radio application ($C_u = 30 \text{ fF}$), as well as for $C_u = 15 \text{ fF}$ and $C_u = 60 \text{ fF}$. For $C_u = 30 \text{ fF}$, most of the INL measurements were within the $\pm 0.5 \text{ LSB}$ limit, except for one input sample (out of the 4 samples for $D_{out} = 00..00$), which was wrongly evaluated, thus a $INL_{max,30f} = 0.68 \text{ LSB}$ ($INL_{min,30f} = -0.5 \text{ LSB}$).

A similar effect occurred for the $C_u = 15 \text{ fF}$ topology, but with more samples wrongly evaluated, resulting in a $INL_{max,15f} = 1.69 \text{ LSB}$ and $INL_{min,15f} = -1.5 \text{ LSB}$. The $C_u = 60 \text{ fF}$ topology showed a different behavior altogether, with larger INL variations around $3/4$ of the Full Scale, as opposed to the other two topologies where this greater variation was around $1/2$ of the analog FS. The minimum and maximum INL was $INL_{max,60f} = 0.52 \text{ LSB}$ $INL_{min,60f} = -0.62 \text{ LSB}$, respectively.

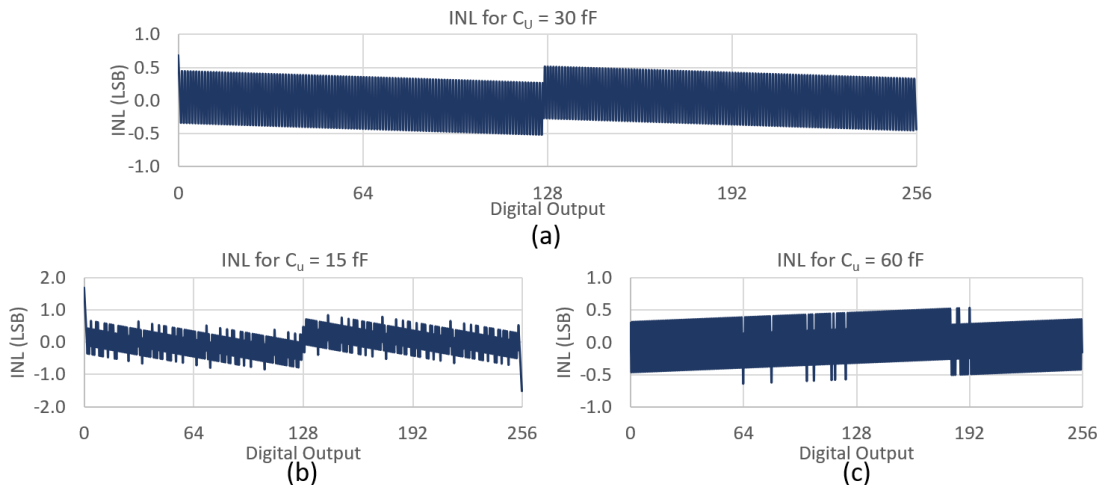


Figure 5.39: INL results at schematic level when (a) $C_u = 30 \text{ fF}$ (the LP radio application), (b) $C_u = 15 \text{ fF}$ and $C_u = 60 \text{ fF}$.

Figure 5.40 shows the DNL results. The nonlinearity that was perceptible in the INL from the $C_u = 15 \text{ fF}$ topology is also present in the DNL results, with $DNL_{max,15f} =$

1.25 *LSB*, representing one missing code, and $DNL_{min,15f} = -0.25 \text{ LSB}$. The remaining results for DNL of the other two topologies indicate no missing code, with $DNL_{max,30f} = DNL_{max,60f} = 0.25 \text{ LSB}$ and $DNL_{min,30f} = DNL_{min,60f} = -0.25 \text{ LSB}$.

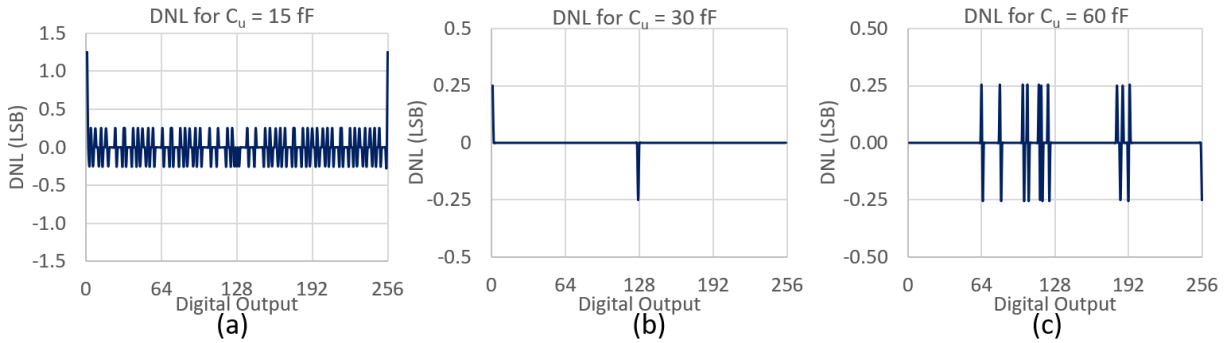


Figure 5.40: DNL results at schematic level when (a) $C_u = 15 \text{ fF}$, (b) $C_u = 30 \text{ fF}$ (the LP radio application) and $C_u = 60 \text{ fF}$.

The layout results, on the other hand, showed a much worsen INL, as can be seen in Figure 5.41.(a). The maximum and minimum results were $INL_{max} = 12.68 \text{ LSB}$ $INL_{min} = -12.90 \text{ LSB}$, respectively. Similarly to what was seen at the $C_u = 15 \text{ fF}$ topology, but much more aggravated at layout level for the $C_u = 30 \text{ fF}$ topology.

This result represents a reduction of the dynamic range of the ADC. A range of approximately 50 mV at the extremes of the dynamic range ($\Delta V_{in} = -500 \text{ mV}$ and $\Delta V_{in} = 500 \text{ mV}$) did not generate valid digital results. Figure 5.41.(b) shows zoomed version of the INL results, where it can be seen that, for most of the samples, INL results spanned between $\pm 2.5 \text{ LSB}$.

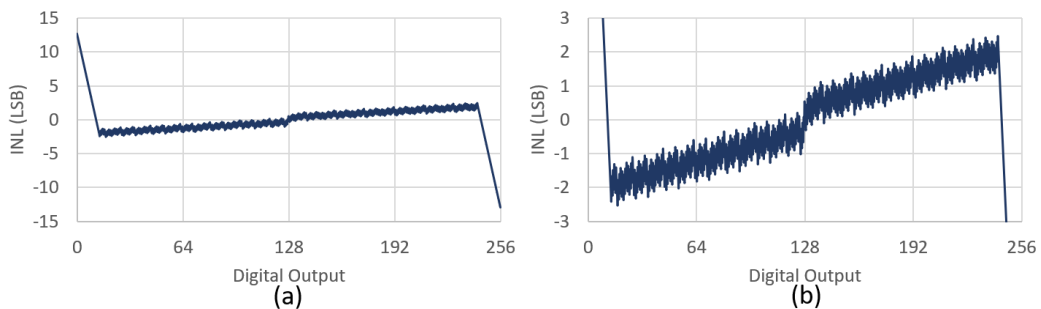


Figure 5.41: INL results at layout level (a) for the entire digital output range and (b) zoomed in a smaller range.

This effect is also present in the DNL results of Figure 5.42.(a), but oppositely to the INL, the DNL issues were limited to first and last DNL estimate, both with value $DNL_{max} = 13 \text{ LSB}$ ($DNL_{min} = -0.5 \text{ LSB}$). This maximum DNL represents 13 missing codes at both extremes, which considering the $LSB = 3.906 \text{ mV}$, corresponds to the 50 mV mentioned earlier. However, since the redundancy of 4x-sampling method was considered, it was possible

to observe that the ADC has a monotonic behavior, that is, the sweep of the input showed that all codes were generated. Hence the DNL smaller than $\pm 0.5 \text{ LSB}$ for all the remaining codes showed in the zoomed version of the DNL results of Figure 5.42.(b).

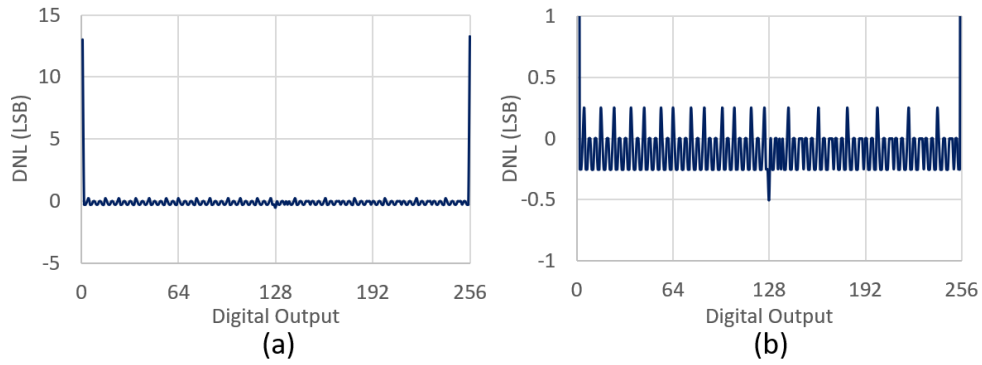


Figure 5.42: DNL results at layout level (a) for the entire digital output range and (b) zoomed in a smaller range.

Only for illustration purposes the INL estimate for a reduced dynamic range, from $\Delta V_{in} = -450 \text{ mV}$ to $\Delta V_{in} = 450 \text{ mV}$, is shown on Figure 5.43. For this reduced input range, the INL was within $\pm 1 \text{ LSB}$.

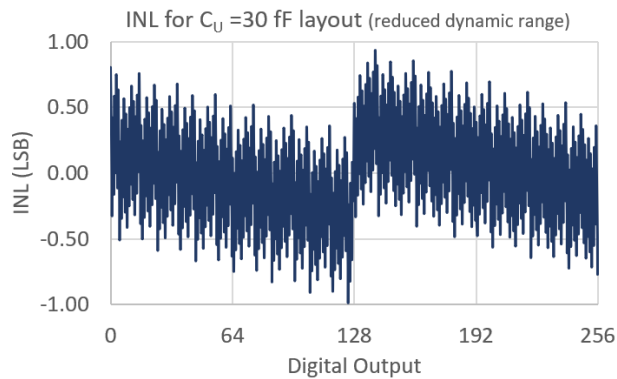


Figure 5.43: INL results at layout level for a narrower input dynamic range.

A careful and thorough investigation of the layout is necessary to pinpoint with precision which parasitics had a greater negative influence on the linearity of the ADC. One possible reason for this effect may result from the parasitic capacitance in the floating nodes of the series structure of the C_u ($= C_{min}/2$), a fact brought by (ZHANG; BONIZZONI; MALOBERTI, 2016) for their C-2C structures.

5.3 Additional Discussion

Typically, figures of merit (FoM) are one way to allow comparisons between various converters which could differ widely in architecture, application, and specifications (MANGANARO, 2011). Focusing on ADCs first, one of the most commonly used FoMs is that called "Walden's" FoM:

$$FoM_W = \frac{P}{f_S \times 2^{ENOB}} \quad (5.2)$$

Considering the results of the dynamic tests, the resulting FoM given by equation 5.2 is $FoM_{schm} = 8.18$ fJ/conversion-step and $FoM_{lay} = 11.1$ fJ/conversion-step. It is important to remind that, although it is a promising result as outlined in Table 5.6, it does not include the power consumption from the digital blocks, nor the contribution of the references. Results presented in Table 5.6 represent measured performances, thus including the SAR logic implemented at circuit level, at the exception of this work, whose results are from post-layout simulation.

Table 5.6: Comparison of Performances

	Ref. (nm)	Tech. (V)	VDD (μ W)	Power (MS/s)	f_S (bits)	Resolution (bits)	ENOB ¹ (fJ/conv-step)	FoM
Charge Average	ISSCC'13	90	0.7	11	4	10	9.05	5.2
Merge-Split	TCAS'15	90	0.5	1.8	2	10	8.97	1.78
OSSI-HBSI	TCAS'15	180	0.6	0.038	0.02	10	9.4	2.8
MOSCAP	JSSC'16	130	0.6	2.78	1	9	8.48	7.8
New-OSSI-HBSI	TCAS'16	180	1.8	820	10	12	10.82	44.2
Low Energy Radio	JSSC'11	90	1	26.3	10.24	8	7.77	12
This work ²	-	130	1	21.0	10	8	7.57 ³ / 7.26	11.1 ³ / 13.7

¹ At Nyquist rate.

² Post-layout simulation results.

³ At $f_{in} = 3$ MHz.

The results from this work are closely related to those of the **Low Energy Radio** and the **New-OSSI-HBSI**, which are closer in resolution and sampling rate. While this work does not include the power from digital blocks, it does have a narrower dynamic range when compared to the other two, which employ VDD and GND as references ($FS = 2 \times VDD$). Considering the specification of the ADC designed in this work and the asynchronous logic structure, a narrower dynamic range impacts directly on the power consumed by the comparator.

Additionally, as mentioned earlier, the employment of custom digital logic could potentially reduce the power consumed by the asynchronous logic, thus decreasing the total power

consumed.

Regarding the three different topologies discussed in this chapter, some conclusions may be drawn from both dynamic and static results. Table 5.7. summarizes the simulation results for the different topologies.

There was no significant difference with the different topologies when looking into power consumption since resolution and sampling frequency remained unchanged for all the scenarios. The current drained from the references, on the other hand, increased with the increase of the unit capacitance.

From the dynamic analysis, the DAC_{30f} showed the best performance and DAC_{60f} the worst performance. From the static analysis point of view, the roles from DAC_{15f} and DAC_{60f} were reversed, still with the best performance for the DAC_{30f} .

Table 5.7: Summary of results for the different DAC topologies

	$C_u = 15 \text{ fF}$	$C_u = 30 \text{ fF}$	$C_u = 60 \text{ fF}$	Units
ENOB	7.64	7.79	6.85	<i>bits</i>
INL	1.69 / -1.5	0.68 / -0.5	0.52 / -0.62	LSB
DNL	1.25 / -0.25	0.25 / -0.25	0.25 / -0.25	LSB
number of C_u	25	35	64	-
I_{tot}	18	18	18	μA
I_{ref}	18.4	21.5	28.6	μA

Regarding the area occupied, the DAC_{15f} employs the smaller set of C_u , while DAC_{60f} has the highest number of unit capacitors. On the other hand, the series capacitance used both in DAC_{15f} and DAC_{30f} may be a source of linearity errors, as it was seen on both schematic for the former and layout for the latter.

Considering the topology which underwent a more thorough characterization, its total equivalent capacitance corresponds to $C_{eq} = 1.92 \text{ pF}$ for an 8-bit resolution. For the same topology, a 9-bit resolution corresponds to twice this value $C_{eq} = 3.84 \text{ pF}$, which was the total capacitance considered for the DAC_{60f} . Thus, by looking at the results from the bootstrapped switch characterization for $C_u = 60 \text{ fF}$, the same attenuation will be present for a 9-bit resolution. For $f_S = 10 \text{ MHz}$ and $f_{in} = 3 \text{ MHz}$, the resulting $SINAD_{BSW}$ was 46.46 dB, or equivalently $ENOB_{BSW} = 7.43$, which means 1.5 *bits* lost only due to the sampling switch. Hence, the bootstrapped switch as it is defines a superior limitation of 8 bits to this ADC.

Still on the topic of resolution, considering the same $FS = 1 \text{ V}$ but a 9-bit resolution, the *LSB* is 1.953 mV, which results in a quantization noise of 199.34 μV_{rms} . For the comparator implemented in this work, the minimum noise level is 190 μV_{rms} , which, equivalently, sets the

ADC resolution limit for this comparator design to 9 bits.

The characterization of the bootstrapped switch regarding sampling frequency showed that its design is only suitable for frequencies below 15 MHz ($SINAD > 64\text{ dB}$). Results from the A/D Converter corroborated this result, showing a $ENOB = 7.16$ for $f_{Ny} \approx 5\text{ MHz}$.

The exploration of VDD limits for the current SAR ADC is not straightforward as it was for sampling rate or even temperature. If we recall, the DAC switches design considered that the ADC references were limited enough that they allowed the use of only NMOS-switches, instead of transmission gates ($V_{GS,sw} = 1 - 0.75 = 0.25\text{ V} > V_{th} = 0.1\text{ V}$). A small reduction of VDD would cause the DAC switches not to work properly, if a proportional reduction of dynamic range was not performed in parallel. This narrowing of analog input would require a much careful investigation due to adjustment of LSB level, and noise level, etc.

Exploration of VDD was performed for the sampling switch, though, and it was limited to 0.8 V to allow an 8-bit resolution.

6 CONCLUSIONS

The work developed as part of this Master Thesis covered a wide range of topics, not only its primary focus, which was the design of data converters, specifically the SAR ADC, but also the basics of IoT, wireless communication standards, low power radio receivers and the definition of its specifications. Although not all of those topics were covered deeply in this text, this work enabled a brief contact with radio-frequency basics, which is of great relevance nowadays, where increasingly integration is sought in modern System-on-Chips.

The bibliographic review of SAR ADCs performed for this work confirmed what is advertised nowadays, that this architecture is increasingly topic of research, especially with the popularity of WSN and IoT applications. Researches are approaching the power efficiency matter in several manners, the switching scheme being one of them, which was the focus of this Master Thesis.

Implementation of this power-efficient switching scheme, as well as the design of the charge redistribution SAR ADC main blocks were presented in the previous chapters. In this subject, the DAC arrays were also an important topic of investigation and discussion, along with the asynchronous working of the SAR ADC. The circuit level design of the asynchronous logic relied mainly on standard cells, which were not available for the GF 130nm CMOS process employed, thus making it not as power efficient as intended since the standard cells used were not optimized for that goal.

Improvements are also possible for the other three important blocks, which are sampling switch, comparator and the SAR state machine. Although the bootstrapped switch was not a concern in the ADC presented, its implementation could be further improved to a more robust version. Unlike the bootstrapped switch, the comparator does present issues that certainly had a negative impact on the final results of the SAR ADC simulation, which leaves great room for improvement. The current SAR state machine corresponds to a behavioral description in verilog-AMS, and its implementation at circuit level is necessary for generating more precise results.

In spite of all the aforementioned limitations, simulation of the SAR ADC showed promising results, especially in the context of the low power receiver, which left some margin for the ADC resolution. Dynamic results obtained from simulation of the physical layout presented an ENOB of 7.57 bits at $f_{in} = 3 \text{ MHz}$ (RX IF) and $f_S = 10 \text{ MHz}$, while consuming $21 \text{ } \mu\text{A}$ from a 1-V supply voltage. This corresponded to a FoM of 11.1 fJ/conv-step, which is quite promising when compared to the other works of similar resolution and sampling rates

presented previously. The layout occupied a die area of $190 \mu m \times 420 \mu m$.

Although static results from simulation at schematic level were also reasonable, with INL of $0.68/ - 0.5 \text{ LSB}$ and DNL of $0.25/ - 0.25 \text{ LSB}$, those obtained from layout outlined significant non-linearity errors. Since the redundancy was employed when extracting the static results, it was noticeable that all codes were present, and the non-linearity errors represented a narrowing of the dynamic range of the ADC.

6.1 Future Works

As pointed out in the previous paragraphs, there is much room for improvements. Starting with the comparator, its sizing considered mainly delay and power consumption, not focusing on offset, for instance. Improvements regarding offset are proven essential, as noted from the Monte Carlo results regarding mismatch variations. The calibration procedure presented merely is one optimization possibility for this comparator, enhancement of the circuit sizing, especially of the differential pair and the tail transistor are another.

As mentioned, the bootstrapped switch was not a source of much concern, since its dynamic results were fit to the ADC resolution of the low power radio application. However, non-linearity issues were also present at the layout level, which leaves room for investigation and improvements. Like any other switch, the sampling switch may need compensation for charge-injection as well as clock-feedthrough effects, characteristics which were not explored in depth for the bootstrapped switches, and could also be explored in future works.

Regarding the SAR state machine, its implementation at circuit level is necessary, for correct characterization of the ADC. It would include the study of the automatic digital design flow, or possibly the design of custom power optimized standard cells. The latter would also be of value for enhancement of the current consumption of the asynchronous logic.

Additionally, careful investigation of the delay cell, to evaluate its variation impact on the ADC behavior. The decision whether to keep the *vbias* control as an external output should also consider the system as a whole and the availability of input pins. Otherwise, a calibration method for this delay would surely be necessary to ensure the correct functioning of the ADC, which could also be potential future work.

Moreover, the voltage references used thus far have been ideal models and, consequently, not source of noise and nonlinearity. The transistor level implementation of the reference levels is a mandatory step on finalizing the ADC in its entirety, and in considering all source of non-idealities.

Last but not least, the layout requires a careful and in-depth investigation. Some possibilities arise for the issues that surfaced especially on the static analysis, such as: the DAC switches were all implemented as NMOS-only switches, and could be part of the cause for the narrowing of the dynamic range of the ADC; the DAC topology employed, with the series capacitor structure creates an internal floating node, from which the parasitic capacitances could worsen the linearity; finally, improvements in placement and routing of final layout could potentially generate better results, and thus should also be investigated.

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APPENDIX A — VERILOG-AMS FOR SAR STATE MACHINE

```

module adc_sar_8b (
    vinm, vinp, clk, sample, done, dout, cont, sleep,
    sw0n, sw0p, sw1n, sw1p, sw2n, sw2p, sw3n,
    sw3p, sw4n, sw4p, sw5n, sw5p, sw6n, sw6p);

input  vinp, vinm;
//clk = valid, and sample = fs
input  clk, sample;

output [1:0] sw0n, sw0p ;
output [2:0] sw1n, sw1p, sw2n, sw2p, sw3n, sw3p, sw4n, sw4p, sw5n, sw5p,
        sw6n, sw6p;
output [8:0] dout;
output      done, sleep;
output [3:0] cont;

electrical vinp, vinm;

reg [2:0] sw1n, sw1p, sw2n, sw2p, sw3n, sw3p, sw4n, sw4p, sw5n, sw5p,
        sw6n, sw6p;
reg [1:0] sw0p, sw0n;
reg [7:0] dout_int;
reg [8:0] dout;
reg      ip_data, sleep, done;
reg [3:0] cont;

parameter width_data = 10;
integer temp;

initial
    begin
//initial configuration
        sw6p = 3'b010;
        sw6n = 3'b010;
        sw5p = 3'b001;
        sw5n = 3'b001;
        sw4p = 3'b001;
        sw4n = 3'b001;

```

```

sw3p = 3'b001;
sw3n = 3'b001;
sw2p = 3'b001;
sw2n = 3'b001;
sw1p = 3'b001;
sw1n = 3'b001;
sw0p = 2'b01;
sw0n = 2'b01;
done = 1'b0;
dout_int = 7'b000_0000;
dout = 8'b0000_0000;
ip_data = 1'b0;
cont = 4'd0000;
sleep = 1'b0;

```

```
end
```

```
always @(posedge clk) begin
```

```
    if (cont == 0) begin
```

```
        //reset of switches and internal dout, done goes to zero, sleep goes to one
```

```

sw6p = 3'b010;
sw6n = 3'b010;
sw5p = 3'b001;
sw5n = 3'b001;
sw4p = 3'b001;
sw4n = 3'b001;
sw3p = 3'b001;
sw3n = 3'b001;
sw2p = 3'b001;
sw2n = 3'b001;
sw1p = 3'b001;
sw1n = 3'b001;
sw0p = 2'b01;
sw0n = 2'b01;
done = 1'b0;
dout_int = 7'b000_0000;
sleep = 1'b1;

```

```
    end
```

```
end
```

```
always @(posedge sample) begin
```

```
    //counting starts, sleep goes to zero
```

```

        sleep = 1'b0;
        cont = 1;
        dout_int = 7'b000_0000;
end

always @(negedge clk) begin
//assigning ip_data with result from comparator
    temp = V(vinp,vinm);
    if (temp>0) ip_data = 1;
    else if (temp<0) ip_data = 0;

    case (cont)
//1th cycle - BIT 7 MSB
        1: begin
            if (ip_data==1) begin
                dout_int[7] = 1;
                sw6n <= 3'b100;
                sw5n <= 3'b010;
                sw4n <= 3'b010;
                sw3n <= 3'b010;
                sw2n <= 3'b010;
                sw1n <= 3'b010;
                sw0n <= 2'b10;
            end
            else begin
                sw6p <= 3'b100;
                sw5p <= 3'b010;
                sw4p <= 3'b010;
                sw3p <= 3'b010;
                sw2p <= 3'b010;
                sw1p <= 3'b010;
                sw0p <= 2'b10;
            end
            cont = cont+1;
        end
//2th cycle - BIT 6
        2: begin
            if (ip_data ==1) dout_int[6] = 1;
            else begin
                dout_int[6] = 0;

```

```

sw6p[2] = (~dout_int[7]) & (~dout_int[6]);
sw6p[1] = (dout_int[7] ^ dout_int[6]);
sw6p[0] = dout_int[7] & dout_int[6];
sw6n[2] = dout_int[7] & dout_int[6];
sw6n[1] = (dout_int[7] ^ dout_int[6]);
sw6n[0] = (~dout_int[7]) & (~dout_int[6]);
cont = cont+1;
end
//3th cycle - BIT 5
3 : begin
if (ip_data ==1) dout_int[5] = 1;
else begin
dout_int[1] = 0;

sw5p[2] = (~dout_int[7]) & (~dout_int[5]);
sw5p[1] = (dout_int[7] ^ dout_int[5]);
sw5p[0] = dout_int[7] & dout_int[5];
sw5n[2] = dout_int[7] & dout_int[5];
sw5n[1] = (dout_int[7] ^ dout_int[5]);
sw5n[0] = (~dout_int[7]) & (~dout_int[5]);
cont = cont+1;
end
//4th cycle - BIT 4
4 : begin
if (ip_data ==1) dout_int[4] = 1;
else begin
dout_int[3] = 0;

sw4p[2] = (~dout_int[7]) & (~dout_int[4]);
sw4p[1] = (dout_int[7] ^ dout_int[4]);
sw4p[0] = dout_int[7] & dout_int[4];
sw4n[2] = dout_int[7] & dout_int[4];
sw4n[1] = (dout_int[7] ^ dout_int[4]);
sw4n[0] = (~dout_int[7]) & (~dout_int[4]);
cont = cont+1;

end
//5th cycle - BIT 3
5 : begin
if (ip_data ==1) dout_int[3] = 1;
else begin

```

```

        dout_int[4] = 0;

        sw3p[2] = (~dout_int[7]) & (~dout_int[3]);
        sw3p[1] = (dout_int[7] ^ dout_int[3]);
        sw3p[0] = dout_int[7] & dout_int[3];
        sw3n[2] = dout_int[7] & dout_int[3];
        sw3n[1] = (dout_int[7] ^ dout_int[3]);
        sw3n[0] = (~dout_int[7]) & (~dout_int[3]);
        cont = cont+1;
    end
//6th cycle - BIT 2
    6 : begin
        if (ip_data ==1) dout_int[2] = 1;
        else begin
            dout_int[5] = 0;

            sw2p[2] = (~dout_int[7]) & (~dout_int[2]);
            sw2p[1] = (dout_int[7] ^ dout_int[2]);
            sw2p[0] = dout_int[7] & dout_int[2];
            sw2n[2] = dout_int[7] & dout_int[2];
            sw2n[1] = (dout_int[7] ^ dout_int[2]);
            sw2n[0] = (~dout_int[7]) & (~dout_int[2]);
            cont = cont+1;
        end
//7th cycle - BIT 1
    7 : begin
        if (ip_data ==1) dout_int[1] = 1;
        else begin
            dout_int[6] = 0;

            sw1p[2] = (~dout_int[7]) & (~dout_int[1]);
            sw1p[1] = (dout_int[7] ^ dout_int[1]);
            sw1p[0] = dout_int[7] & dout_int[1];
            sw1n[2] = dout_int[7] & dout_int[1];
            sw1n[1] = (dout_int[7] ^ dout_int[1]);
            sw1n[0] = (~dout_int[7]) & (~dout_int[1]);
            cont = cont+1;
        end
//8th cycle - BIT 0 LSB;
    8 : begin
        if (ip_data ==1) dout_int[0] = 1;

```

```
        else begin
            dout_int[0] = 0;
            //counter reset, dout is available, done goes to one
            cont = 4'd0000;
            dout[7:0] = dout_int;
            done = 1'b1;
        end
    endcase
end
endmodule
```

APPENDIX B — LIST OF PUBLICATIONS

Publications related to Master Thesis

ANDRADE, N.; GUIMARÃES, G.; **DORNELAS, H.**; TOLEDO, P.; FABRIS, E.; KLIMACH, H. and BAMPI, S. **Low Power IEEE 802.11ah Receiver System-Level Design Aiming for IoT Applications**. In: *Proceedings of the 30th Symposium on Integrated Circuits and Systems Design (SBCCI'17)*. Fortaleza, CE, Brazil. September 2017.

Publications related to Master Works

DORNELAS, H.; SCHMIDT, A.; STRUBE, G.; FABRIS, E.; **New Technology Migration Methodology for Analog IC Design**. In: *Proceedings of the 5th Workshop on Circuits and Systems Design (WCAS'15)*. Salvador, BA, Brazil. August-September 2015. – **1st Place Best Paper Award**.

DORNELAS, H. U.; ZAMPARETTE, R. L. B.; MONSALVE D., J. C.; FABRIS, E. E.; **A 10-Bit $\Sigma\Delta$ A/D Converter for the SBCD in 180nm CMOS Technology**. In: *Proceedings of the 5th Workshop on Circuits and Systems Design (WCAS'15)*. Salvador, BA, Brazil. August-September 2015.

Publications unrelated to Master Works

ANDRADE, N.; TOLEDO, P.; CORDOVA, D.; NEGREIROS, M.; **DORNELAS, H.**; TIMBO, R.; SCHMIDT, A.; KLIMACH, H.; FABRIS, E. BAMPI, S. **Analysis and Design of 180nm CMOS Transmitter for a New SBCD Transponder SoC**. In: *Proceedings of the 6th Workshop on Circuits and Systems Design (WCAS'16)*. Belo Horizonte, MG, Brazil. August-September 2016.

MARTINELLI, B.; TOLEDO, P.; **DORNELAS, H.**; NEGREIROS, M.; KLIMACH, H.; FABRIS, E. BAMPI, S. **A 52 dB THD 3rd-Order Gm-C CMOS Filter for a New SBCD Transponder SoC**". *Proceedings of the 6th Workshop on Circuits and Systems Design (WCAS'16)*. Belo Horizonte, MG, Brazil. August-September 2016.