UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM MICROELETRÔNICA

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A 130nm CMOS UHF Satellite Receiver Front-End for the Brazilian Environmental Data Collecting System

Thesis presented in partial fulfillment
of the requirements for the degree of
Master of Microelectronics

Advisor: Prof. Dr. Hamilton Duarte Klimach

Porto Alegre
May 2019

CIP — CATALOGING-IN-PUBLICATION

Timbó, Renê Moreno

A 130nm CMOS UHF Satellite Receiver Front-End for the Brazilian Environmental Data Collecting System / Renê Moreno Timbó. – Porto Alegre: PGMICRO da UFRGS, 2019.

102 f.: il.

Thesis (Master) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Microeletrônica, Porto Alegre, BR–RS, 2019. Advisor: Hamilton Duarte Klimach.

1. RF Circuits. 2. Microelectronics. 3. Front-end. 4. Satellite. 5. SBCDA. 6. LNA. 7. Mixer. I. Klimach, Hamilton Duarte. II. Título.

ACKNOWLEDGMENTS

During the development of this thesis, I had the opportunity to meet incredible people in my way. Each of them somehow gave some contribution that helped me to finish this work.

First, I would like to thank my family, my parents João Parente Timbó and Denise de Deus Moreno Timbó, my brother Renan Moreno Timbó, my sister Renata Moreno Timbó and my brother-in-law Pablo Cassas and sister-in-law Shenna Araújo for supporting me whenever I need with a talk, advice or even with financial support.

I would like to thank my advisor Hamilton Duarte Klimach to give me the opportunity to obtain my master degree, for having patience with me and for guiding me through this whole process.

My friends and colleagues of NSCAD microeletrônica, Nelson Andrade, William Medeiros, Alonso Schmidt, Pedro Toledo, David Cordova, Helga Dornelas, Diogo Santana, Jhon Caicedo, Marcelo Negreiros, Jerson Guex, Thiago Nagel, Tatiana Costa and Luís Benitez that aid me technically and supported me in many moments during my trajectory.

To the NSCAD IT team, Márcia Silva and Felipe Formiga, for providing excellent support with Cadence, WicKeD and Keysight tools whenever I needed.

To the students of IC-Brazil training program that indirectly made some contribution to this work by making me study harder to teach them, to solve their problems or in some cases to propose partial solutions to this project.

To all students and professors of UFRGS Analog/RF GME group who contributes with discussions and suggestions during the meetings about this work. Also, to the friends of UFRGS LOGICS group.

To all professionals that work on administrative of Instituto de Informática and in the Microelectronics Post-Graduation Program.

To CNPq, CAPES, and LSITEC for financial support and MOSIS for the available PDK used in this work.

To all other people that directly or indirectly contributed to this work and was not mentioned.

ABSTRACT

The Brazilian Environmental Data Collector System (SBCDA) has the objective to collect, by using satellites, data for environmental applications like meteorological forecast, pollution control, firefighting, and others. The SBCDA is composed of satellites, data collector platforms (DCP) that are distributed all over the country and a Control Center for data processing. By using more advanced technology nodes, it is expected even more integration of all components of the satellite, reducing the utilized total area and power consumption of the device as well. It is therefore proposed to design an RF receiver front-end for a transponder satellite to work at a UHF frequency of 401.635MHz with the technology of 130nm provided by IBM to accomplish this objective. It has a total gain of 39 dB, distributed between an LNA and a Mixer, 4.5 dB of NF and IIP3 of -32.5 dBm with 10.4 mW of power consumption.

Keywords: RF Circuits. Microelectronics. Front-end. Satellite. SBCDA. LNA. Mixer.

UM *FRONT-END* DE UM RECEPTOR PARA SATÉLITE UHF NA TECNOLOGIA 130 NM CMOS PARA O SISTEMA BRASILEIRO DE COLETA DE DADOS AMBIENTAIS

RESUMO

O Sistema Brasileiro de Coleta de Dados Ambientais (SBCDA) tem o objetivo de coletar, via satélite, dados para aplicações como previsão meterológica e climática, controle de poluição, combate a incêndios, entre outras. O SBCDA é composto por satélites, plataformas de coleta de dados (PCD) ambientais distribuídas ao longo do país e de um Centro de controle de missão para processamento dos dados. Com a utilização de nós tecnológicos mais avançados, procura-se cada vez mais uma maior integração dos componentes, reduzindo a aŕea total utilizada, bem como o consumo total do dispositivo. É proposto, portanto, o projeto de um receptor do front-end RF para o transponder de um satélite na tecnologia de 130nm, fornecida pela IBM para realizar este objetivo. Ele fornece um total de 39 dB de ganho, distribuídos entre o LNA e o mixer, 4.5 dB de figura de ruído e um IIP3 de -32.5dBm consumindo 10.4mW de potência.

Palavras-chave: Circuitos RF, Microeletrônica, Front-End, Satélite, SBCDA, LNA, Mixer.

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LIST OF ABBREVIATIONS AND ACRONYMS

1dBCP	1 dB Compression Point
ADC	Analog-to-Digital Converter
ADS	Advanced Design Software
AGC	Available Gain Circles
ARGOS	Advanced Research and Global Observation Satellite
BA	Bahia
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CBERS	China Brazil Earth Resources Satellite
CMOS	Complementary Metal Oxide Semiconductor
CONASAT	Environmental Nano Satelite Constelation
CTAT	Complementary to the Absolute Temperature
DC	Direct Current
DCP	Data Collector Platform
DSB	Double Side Band
DSP	Digital Signal Processing
ENOB	Effective Number Of Bits
ESD	Electrostatic Discharge
FoM	Figure of Merit
FSF	Frequency Scaling Factor
GHz	Giga Hertz
GEO	Geostationary Earth Orbit
HEO	High Earth Orbit

IBM	International Business Machines
IF	Intermediary Frequency
IIP3	3^{rd} order Input Intermodulation Products
IM	Image Signal
IM3	3^{rd} order Intermodulation
INPE	National Institute of Spatial Researches
INMET	National Institute of Meteorology
KHz	Kilo Hertz
LNA	Low Noise Amplifier
LEO	Low Earth Orbit
LO	Local Oscillator
MC	MonteCarlo
MEO	Mid Earth Orbit
MHz	Mega Hertz
MIM	Metal-Insulator-Metal capacitors
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NF	Noise Figure
NMOS	N-type metal-oxide-semiconductor
PAC	Periodic Alternated Current
PMOS	P-type metal-oxide-semiconductor
PSS	Periodic Steady State
PTAT	Proportional to the Absolute Temperature
PVT	Process, Voltage and Temperature
QPSS	Quasi-Periodic Steady State
QPNoise	Quasi-Periodic Noise
RF	Radio Frequency

RX	Receiver
SBCDA	Brazilian Environmental Data Collector System
SC	Santa Catarina
SCD-1	Data Collector Satellite - 1
SINDA	Environmental Data Integrated System
SNR	Signal-to-Noise Ratio
TC	Temperature Coefficient
UFRGS	Federal University of Rio Grande do Sul
UHF	Ultra High Frequency
VSWR	Voltage Standing Wave Ratio

CONTENTS

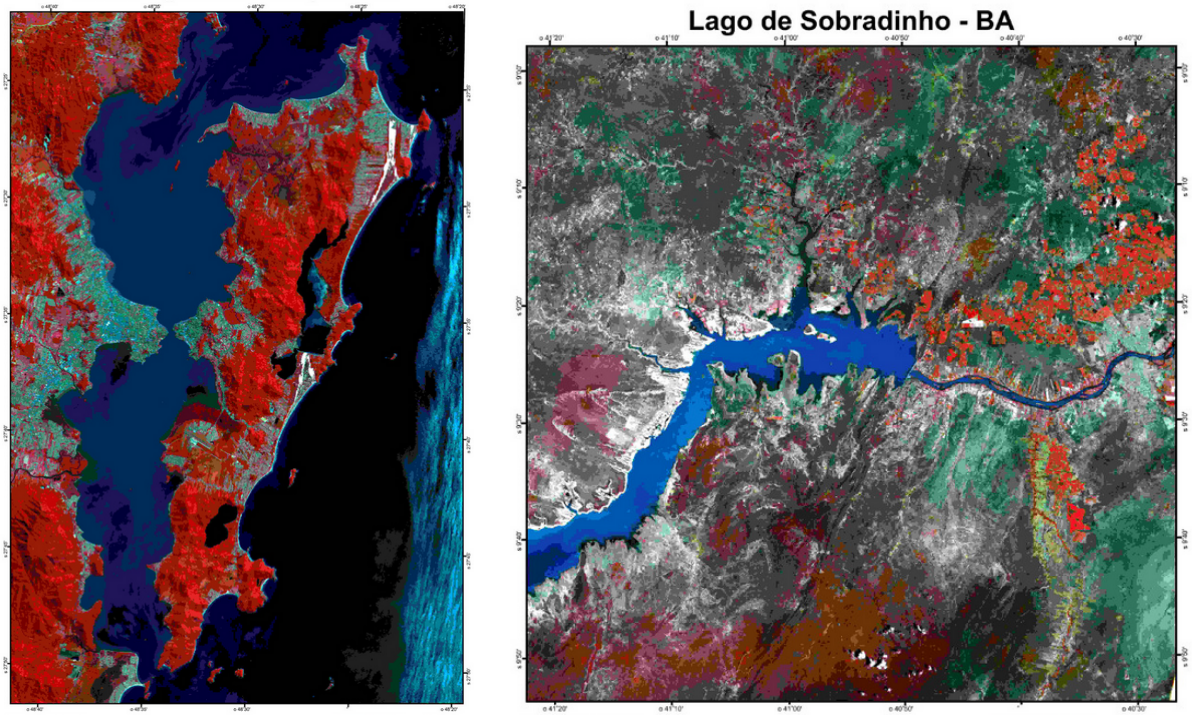
1 INTRODUCTION

It is an industry demand to produce innovations on existent products with the advance of technology. In general, the new structures to be proposed aim to miniaturize even more the electronic circuits, allowing a higher integration between them, improving its coupling efficiency and achieving better frequency response for a given passing band.

In the case of telecommunications systems, the development of a robust and reliable integrated system becomes essential to guarantee that all data or information is received and re-transmitted correctly. In this way, this work has as primary objective the development of a Radio-Frequency(RF) integrated front-end for Brazilian Environmental Data Collect System Satellite (SBCDA) using a 130 nm technology provided by IBM.

Figure 1.1: Examples of application of Satellite images

(a) City growth of Florianópolis- SC (b) Hidrographic basin monitoring in Sobradinho-BA



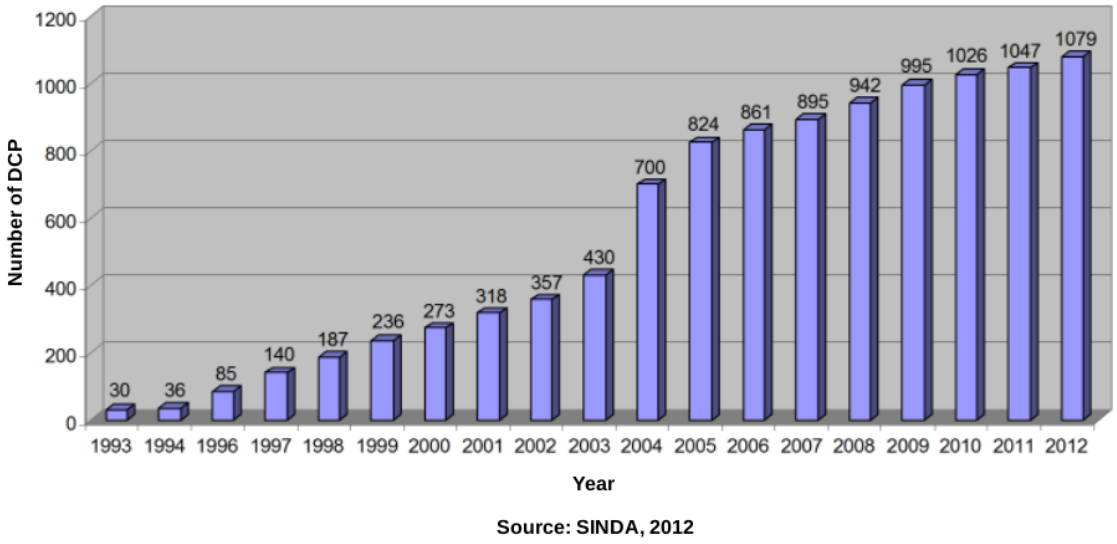
Source: INPE

This system has the objective to collect data for applications like climatic and weather forecast, pollution control on cities, firefighting, oceanography, wildlife monitoring, cities growth, and others. Figure 1.1 (a) shows an example of the expansion of the city of Florianópolis - Santa Catarina (SC), marked in green, with the relief area or vegetation that has not yet been occupied, marked in red. Figure 1.1 (b) exemplifies a monitoring result of the São Francisco river, marked in blue, in the city of Sobradinho - Bahia (BA) which compounds an essential hydrographic basin in the Brazilian Northeast.

1.1 SBCDA

Initially, through a partnership between the governments of China and Brazil, it was launched the CBERS (**C**hina-**B**razil **E**arth **R**esources **S**atellite) program to develop a satellite technology that could make feasible remote sensing and monitoring of large depopulated areas and with extensive agricultural and environmental potential that both countries have.

Figure 1.2: Number of DCP all over the years



On February of 1993, it was launched the first data collector satellite (SCD-1) to accomplish this objective and started to install some data collector platforms (DCP) in the country. Altogether six satellites have already been launched, due to the lifetime of each satellite, but all of them have the same final objective: the environmental data collection. (SCD−1..., 2018)

The DCPs might provide hydrological and meteorological information of the country. The number of installed DCPs is continually increasing, as showed in figure 1.2, but due to lack of maintenance, not all installed DCP's are active. Approximately 54% of the total number of DCPs are operating, and they divide themselves between hydrological ($\approx$ 43%) and meteorological ($\approx$ 38%) platforms. (LIMA; JOTHA; BIONDI, 2011)

The satellites can operate on different orbits depending of their altitude (LEO - Low Earth Orbits, MEO - Mid Earth Orbits, GEO - Geostationary Earth Orbits, and HEO - High Earth Orbit). Table 1.1 shows that low Earth orbit satellites operate in the range of 150 Km to 900 Km of altitude, and suit better for weather/climatic applications using

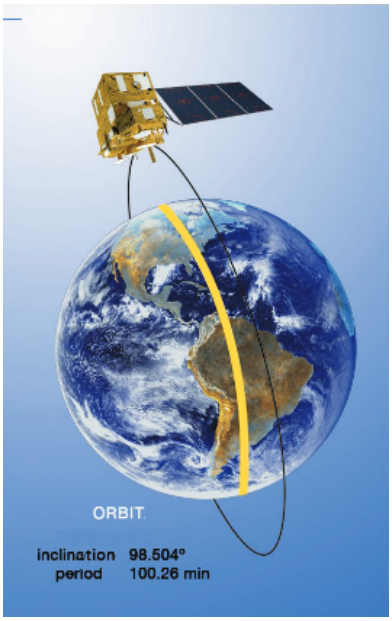
Table 1.1: Orbit types

Orbit Type	Mission	Altitude	Period	Tilt
LEO				
Polar sun-synchronous	Remote sensing/ weather	150-900 Km	98-104 min	98°
Inclined nonpolar	International Space Station	340 Km	91 min	51.6°
Polar non-sun-synchronous	Earth observing, scientific	450-600 Km	90- 101 min	80 - 94°
MEO				
Semisynchronous	Navigation, communications, Space environment	20100 Km	12h	55°
GEO				
Geosynchronous	Communication, early warning	35786 Km	24h	0°
Geostationary	Nuclear detection, weather	35786 Km	24h	0°
HEO				
Molniya	Communications	Varies from 495 Km to 39587 Km	12h	63.4°

source: (CHATTERS; EBERHARDT; WARNER, 2009)

satellites with polar trajectories (with inclination $\approx 90°$) with low orbit inclination (about $8°$).

Figure 1.3: Satellite with low inclination orbit for higher coverage in the country



Source: INPE

The satellite uses low inclination orbits (figure 1.3) to obtain a higher coverage in the country because besides getting more satellite passages per day ($\approx$ 14 passages), it provides a satisfactory covering of south region on Brazil.(SANTOS; FRANCISCO; YAMAGUTI, 2013)

The Brazilian environmental data collection system is, therefore, composed of satellites of the CBERS program and DCPs (figure 1.4). The DCP transmission range is chosen in the way to guarantee that each DCP has at least one favorable passage per day on it.

Figure 1.4: Example of a Data Collector Platform

Source: SINDA/INPE

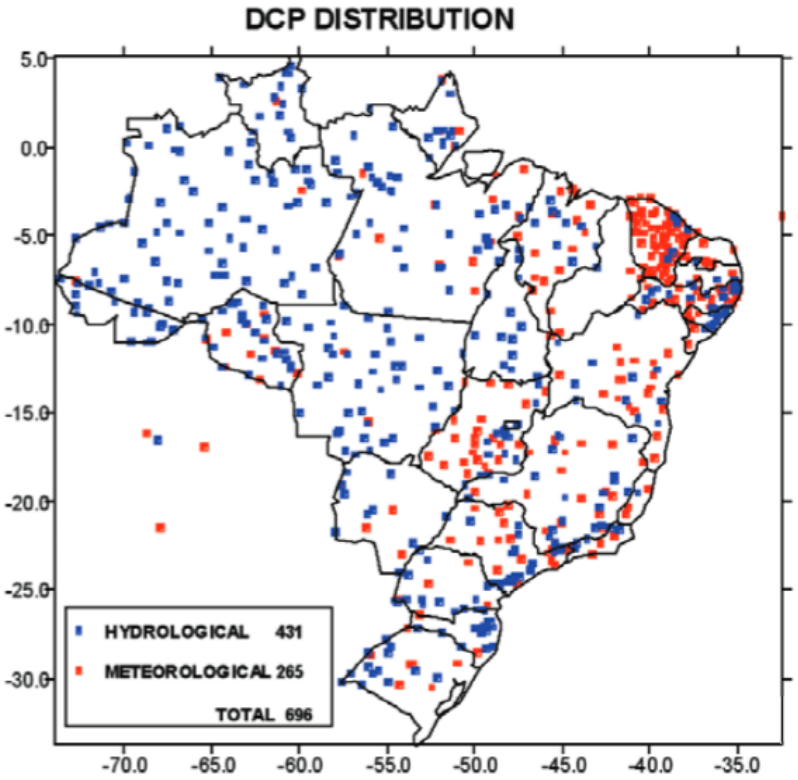
The satellites have the function to collect data from hydrological and meteorological platforms distributed all over the country, as shown in figure 1.5 (a), to obtain for example information of the total annual precipitation in the country (figure 1.5 (b)).They will be relayed to ground station located on cities of Alcântara - Maranhão, and Cuiabá - Mato Grosso to be re-transmitted to a control center located in Natal- Rio Grande do Norte.

Besides this, the program disposes of satellites that comes from ARGOS (Advanced Research and Global Observation Satellite) organization, that has a polar trajectory, to acquire global positioning data with similar operation principle, but that works with an operational frequency of 401.65 MHz.

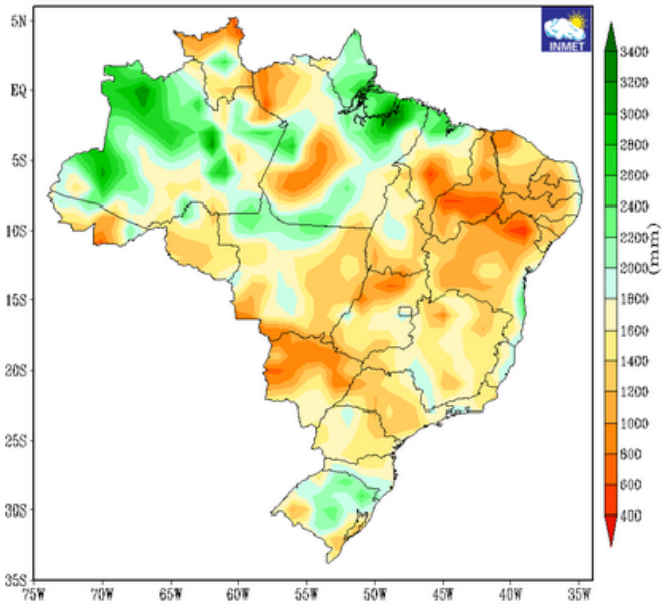
The DCP's have random access to the satellites, and they work with two channels, one that acts on ARGOS international frequency (401.65 MHz) and any other DCP that do not use a foreign satellite uses a frequency of 401.62 MHz (TUDE et al., 1986). Therefore, it will be used as an operation frequency a mean of these two values, i.e., a 401.635 MHz.

Figure 1.5: Data Collector Platforms distribution

(a) Ground DCP



(b) Annual precipitation in 2018



Annual total precipitation map in 2018

Source: (a) INPE (b) INMET

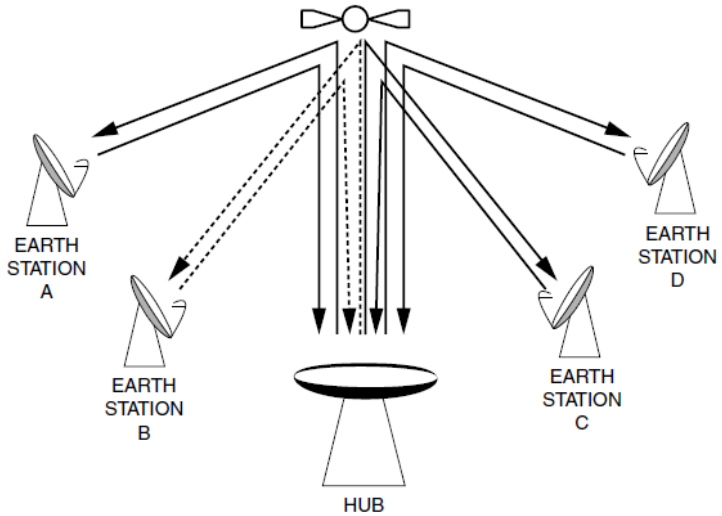
1.2 Transponder

Transponders are electronic blocks that compose the communication subsystems of satellites and their functions are receiving, processing and re-transmitting RF signals that come from different sources. Receiving and transmitting use different frequencies for uplink and downlink and signal could be moved to intermediary frequencies or even to baseband through the downconversion phase.

The primary function of the transponder, therefore, is to receive the signals from DCP, modulate the information and relay it in a different frequency range to specific ground stations and it must also perform the following functions:

- To capture from the network all carrier frequencies transmitted by ground stations;
- To avoid interferers that appear in other frequencies, different from the desired frequency range;
- To amplify the receiving signal limiting the noise and distortion at most;
- To change the carrier frequency from uplink to downlink;
- To provide the required power on the antenna interface;
- To relay the signal to ground stations on Earth.

Figure 1.6: Transponder functionality



Source: (MARAL; BOUSQUET, 2002)

A transponder receiver can be implemented using different strategies, being the single conversion the simplest, because filtering, amplifying and equalization are done in a relatively low frequency when compared to the uplink frequency. For a low value

of intermediate frequency, it is necessary to provide an RF filter with high selectivity tuned to the frequency of the carrier to remove an undesired image frequency that the conversion generates. Dual conversion receivers offer improved characteristics than the single, assuring more filtering, but it uses a second mixer stage to move signal to an intermediary frequency.

The frequency conversion of mixers causes an increase of total noise in the system, so it is necessary to use a low noise amplifier (LNA) at receiver input to provide a high power gain without generating too much noise. By doing this, reduces the total noise produced by mixers,and the noise obtained in the receiver is limited practically to the noise of the first stage. Besides this, the mixer will produce image frequencies on desired frequency range that can compromise the signal response, so it is necessary to use an image rejection architecture or to include an image rejection filter in the architecture to avoid this problem.

1.3 Thesis Organization

The work presented in this document is a part of the design of a superheterodyne receiver that operates at 401.635 MHz and makes a downconversion to 23.715 MHz frequency. The text is organized as follows.

Chapter 2 presents a comparison of receiver topologies and reports what have already been developed by other researchers and the objectives of this work.

Chapter 3 presents all calculations for superheterodyne receiver specifications for a satellite communication system.

In chapter 4, it is shown the proposed Low Noise Amplifier (LNA) topology with some matching design techniques, including post-layout nominal, corners, and Monte-Carlo results.

Chapter 5 analyzes the effects of the image rejection filter in the architecture.

Chapter 6 details the proposed mixer design and presents the post-layout nominal, corners, and Monte-Carlo results.

Chapter 7 shows the effect of cascaded blocks and the final result expected in this project.

Chapter 8 shows conclusions and future works.

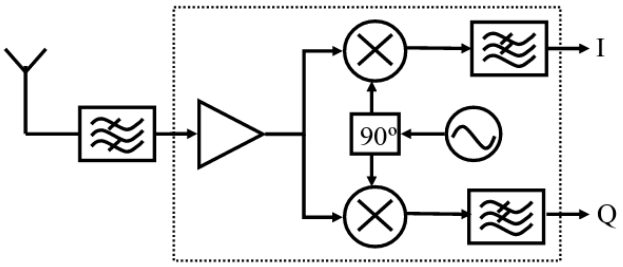
2 RECEIVER TOPOLOGIES AND STATE-OF-ART

2.1 Receiver topologies

Many receiver topologies can be implemented to attend the system requirements in the desired frequency range. The choice of receiver topology must comply with factors like cost, power consumption, noise, linearity, power gain, available area, and operational frequency.

The direct conversion receiver (figure 2.1) makes a single conversion to the baseband frequency, it is low cost and does not need an image rejection filter on its architecture, but there are some noise sources at DC level that sums to the desired signal and corrupts it (e.g., flicker noise). It might also be present a DC offset and some DC products resulting from second-order nonlinear distortion in the amplifier and mixer. If in the frequency range exist relevant interfering signals, the problem might become even worse. Besides that, the local oscillator signal could leak through the mixer back out to the input antenna using devices capacitance of the mixer or either resistances/capacitance between the input and output of the LNA requiring high isolation in the mixer and the amplifier or coupling to pads through the substrate because the LO employs large spiral inductors (BESSER, 2003).

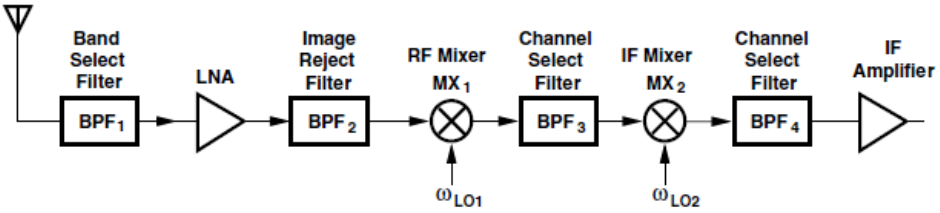
Figure 2.1: Direct conversion architecture



Source: (RAZAVI, 2011)

The superheterodyne receiver (figure 2.2) downconverts the input signal to an intermediary frequency to perform bandpass filtering, amplification and then does a second translation to a baseband frequency (RAZAVI, 1998). It provides a higher gain and lower noise figure, when compared to direct conversion receiver, but suffers from an image problem that appears due to mixing process. It is necessary to include a high-quality factor filter to eliminate this image, which becomes difficult to obtain a total integration of the receiver.

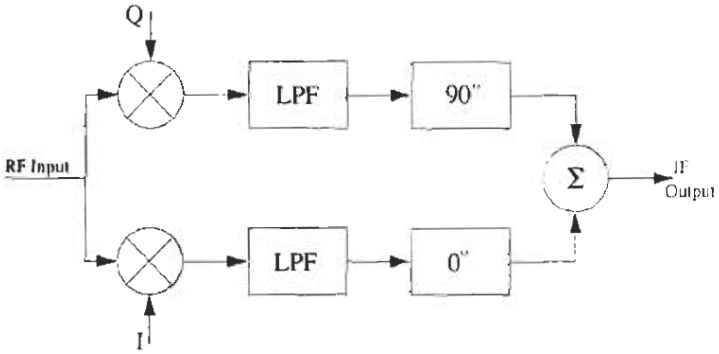
Figure 2.2: Superheterodyne architecture



Source: (RAZAVI, 2011)

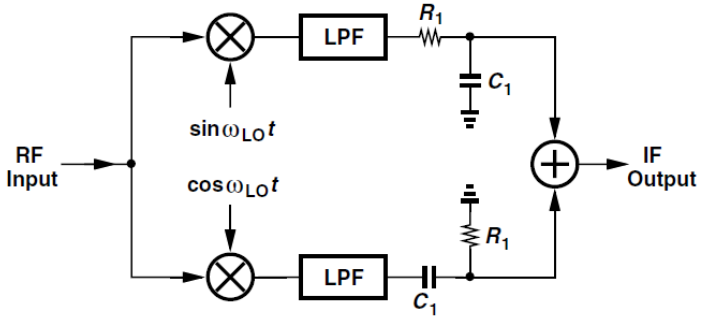
An image rejection receiver uses two branches with a phase difference of 90° (in-phase and quadrature signals) that sum themselves after the mixing process (figure 2.3). If the two pairs of LO signals are in quadrature and the gains are perfectly matched there will be a cancellation of the image (LEE, 2003). The low-pass filters are inserted to remove the unwanted high-frequency components generated by the mixers. The most used topologies are Hartley and Weaver architectures. The principal drawback of the Hartley architecture stems from its sensitivity to mismatches. It is a common practice to use a 45° and a -45° phase deviation on branches using RC networks (figure 2.4).

Figure 2.3: Hartley image reject architecture



Source: (LEE, 2003)

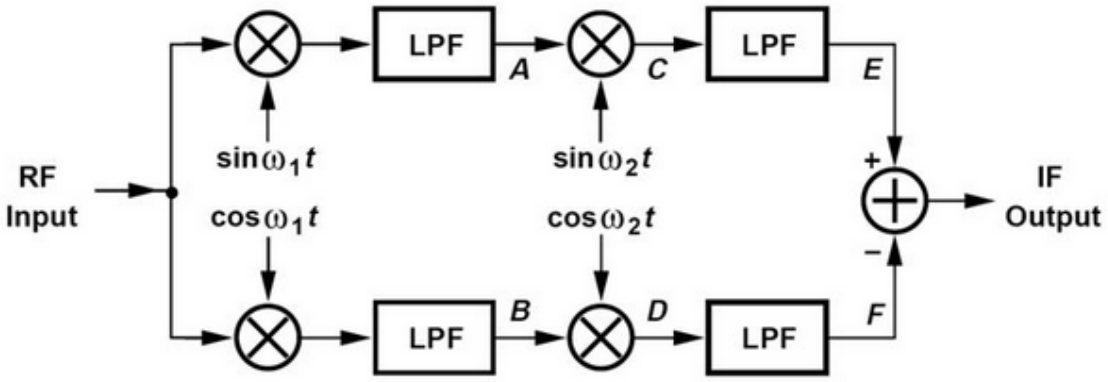
Figure 2.4: 90 ° shift in Hartley receiver



Source: (RAZAVI, 2011)

Weaver image rejection receiver (figure 2.5) is a variation of Hartley architecture that uses a second mixing stage instead of the 90° shift of Hartley architecture to avoid some issues that are present in the Hartley architecture.

Figure 2.5: Weaver image reject architecture



Source: (RAZAVI, 2011)

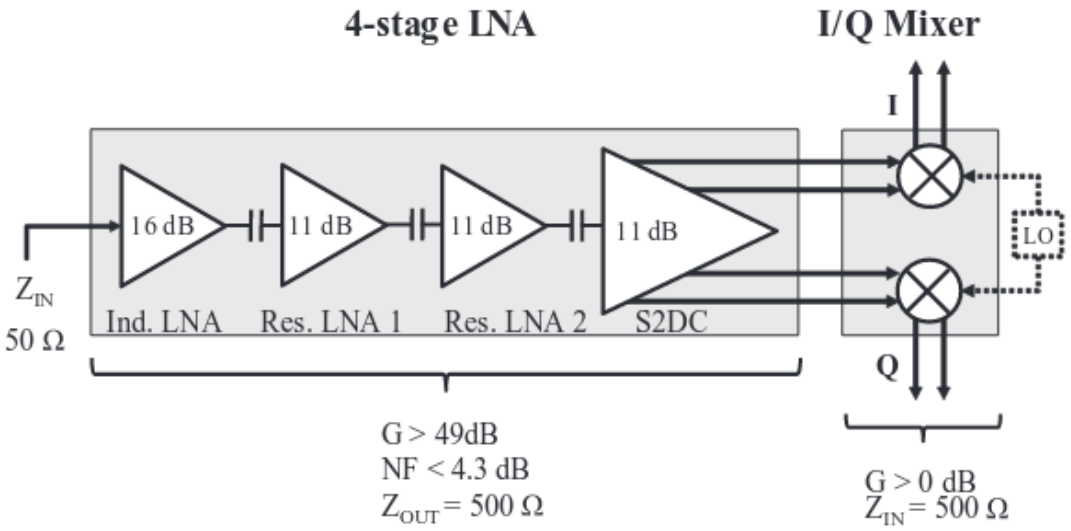
With a proper choice of the LO frequencies of both mixers, it is possible to produce the signal suppressing the image as well. The Weaver topology also suffers from mixing spurs in both downconversion steps (RAZAVI, 2011).

2.2 State-of-art

It is possible to find different solutions for this satellite environment looking at the already published works in the literature.

In (JUNIOR et al., 2016), the authors work with the same application (a receiver front-end for data collection satellites to the SBCDA) and use an in-phase and quadrature low IF architecture that compounds a four stage low noise amplifier, and two mixers using a 130 nm standard CMOS process. The operation frequency is also 401.635 MHz.

Figure 2.6: Low IF image rejection architecture

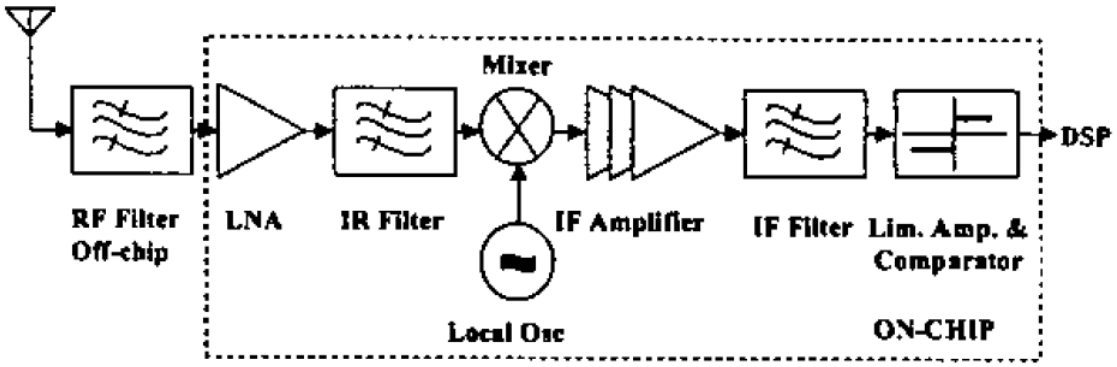


Source: (JUNIOR et al., 2016)

The authors use a four-stage LNA and a mixer in their receiver (figure 2.6). The first stage is an inductively degenerated LNA with an LC tank load, the second and third stages are two resistive LNAs with a resistor as a load, and the fourth stage is a single-to-differential LNA structure to avoid the use of an external balun providing gain and isolating the quadrature signals. It provides -64.75 dBm of IIP3, a total power gain of 49 dB and NF of 2.1 dB and uses a power-constrained simultaneous noise and input matching technique to achieve these gain and noise figure values using an off-chip inductor to provide input matching. An active double balanced mixer with DC coupling resistive matching and a current steering load with a buffer stage provides 5 dB of gain and NF less than 49 dB and IIP3 of -47.7 dBm is used to pass on linearity specifications of the receiver. The final front-end provides a total IIP3 of -63 dBm, a power gain of 54dB and a Noise figure of 2.3 dB consuming 48 mW.

In (ZENCIR N. S. DOGAN, 2002), the authors expose a low power and low IF Receiver architecture (figure 2.7) that works at the frequency of 435 MHz using a 500 nm CMOS process for deep space communications. This receiver uses a differential cascode LNA to reject any eventual substrate noise that may arise from other components of the integrated receiver and an active double balanced mixer to perform the frequency conversion to a 2MHz intermediary frequency having low power dissipation and low LO input power. The LNA uses a classical inductor degeneration to obtain a proper matching and uses a capacitor to couple with the mixer stage. The adopted mixer is a typical Gilbert cell topology without extra circuitry. This receiver achieves a simulated noise figure of 3.8 dB, a conversion gain of 54 dB, 1-dB compression point of -42 dBm and an IIP3 of -34 dBm and a total of 15 mW of power consumption.

Figure 2.7: Low IF homodyne architecture

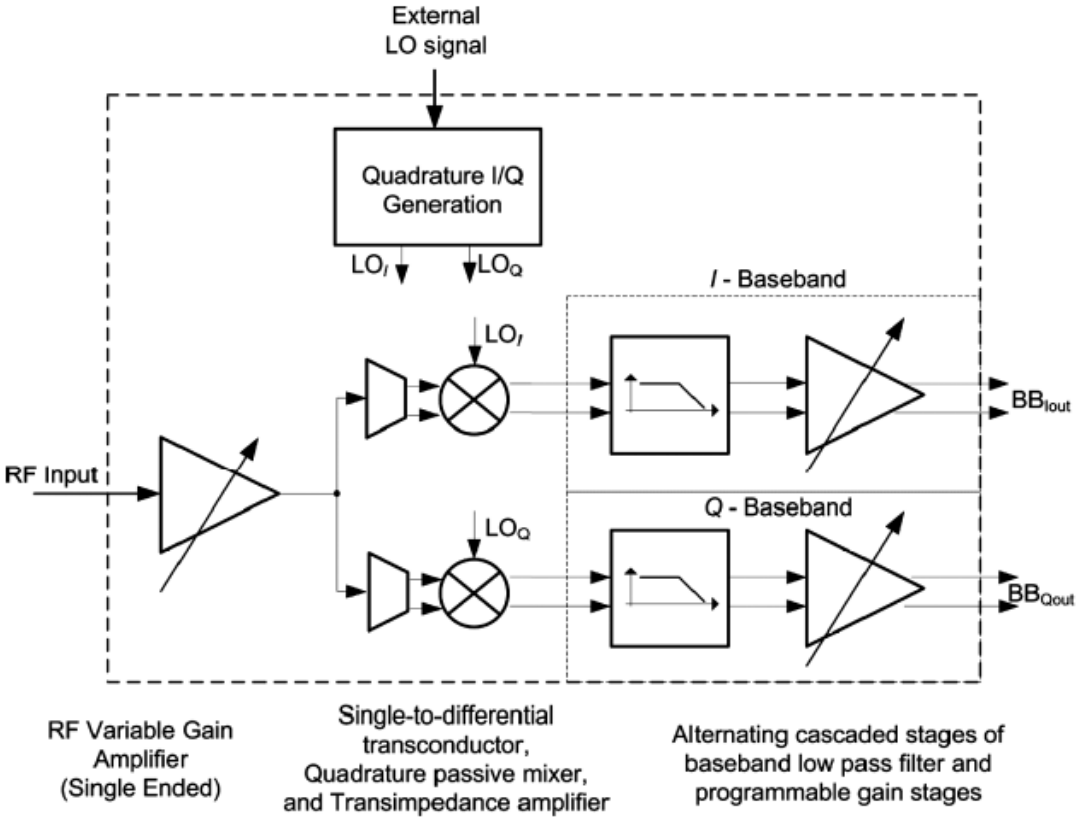


Source: (ZENCIR N. S. DOGAN, 2002)

In (KULKARNI et al., 2012) the authors propose an integrated UHF receiver for digital video broadcasting (DVB-H) using a direct conversion architecture (figure 2.8). The receiver has a single-ended RF input to provide gain-independent matching. The single-to-differential signal conversion uses two I/Q linear transconductors which in turn drive passive mixers. An RF variable gain amplifier composes the first stage with 30 dB of gain range values that helps to maximize the output signal-to-noise-distortion-ratio (SNDR). The matching network uses a shunt-feedback scheme without a shunt peaking inductor. It uses five identical Gm stages with 6dB each and a control block to select an adequate total gain (from -14 dB to +16 dB), targeting a Noise Figure of 3dB at maximum gain and an IIP3 of 20 dBm at minimum gain. The receiver also uses a single-to-differential conversion at the RFVGA output to connect with a passive mixer terminated at the virtual ground of a transimpedance amplifier (TIA) stage exhibiting higher linearity

than the active Gilbert cell topology. The combination of the gm stage, passive switches, and the TIA have an IIP3 of 13 dBm with 18 dB of gain and 12 dB of NF, using a sinusoidal LO. This receiver works at the frequency of 470 MHz to 862 MHz in a 0.18 μm RF CMOS technology provided by IBM and obtained measured results of 80 dB of gain 7.9 dB of NF IIP3 of 2 dBm and power consumption of 120 mW.

Figure 2.8: Direct conversion architecture



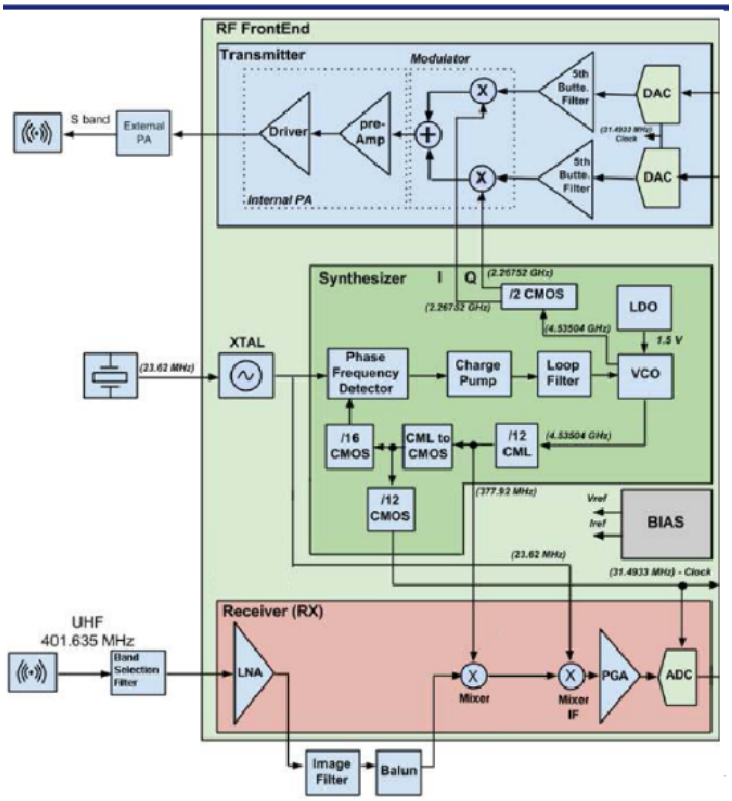
Source: (KULKARNI et al., 2012)

It will be adopted in this work a superheterodyne receiver topology to make a performance comparison among different topologies of receivers for this specific application because this topology provides a high gain (necessary for this application) with low effect of second order interferers (IP2). The direct conversion architecture would provide too tight results for each block. The receiver uses a cascode LNA and an active double balanced mixer for the RF front-end.

3 SUPERHETERODYNE RECEIVER

The transponder project composes a receiver and transmitter structures, a synthesizer (figure 3.1) and a digital block that do some signal processing (DSP). The primary objective of this work is to detail only the receiver, specifically the RF front-end.

Figure 3.1: Analog transponder architecture



Source:(NEGREIROS et al., 2015)

The receiver not only has the task of demodulating the incoming modulated signal but it must perform other functions like carrier frequency tuning, filtering, and amplification. It consists of a radio-frequency section, composed by a low noise amplifier, a mixer and a local oscillator, and an intermediary frequency section with another mixer and filters and a baseband section with amplifiers and an analog-to-digital converter.

The superheterodyne receiver architecture often has several frequency translation stages (IF frequencies) to optimize selectivity, dynamic range and image rejection. The incoming amplitude modulated wave is picked up by the receiving antenna and amplified in the RF section that tunes to the carrier frequency of the incoming wave. Multi-IF stages relax the image filtering problem. Instead of moving to such a low IF where the image filtering is difficult (or expensive and bulky), it is common to downconvert twice, using successively lower IF frequencies.

3.1 Receiver specifications

The receiver translates signals that come from the DCPs to a frequency range of 65 KHz to 125 KHz. An intermediary frequency of 23.715 MHz allows that all frequencies in the complete transceiver come from a single reference oscillator in the synthesizer architecture (TUDE et al., 1986). The main specifications for a superheterodyne receiver with dual conversion are total gain, noise figure, linearity (1dBCP and IIP3) and frequency range. The following subsections will detail each of them.

3.1.1 Receiver Gain

The gain specification depends on the analog-to-digital converter (ADC) requirements at the end of the receiver chain. A delta-sigma converter topology offers power reduction, and needs a minimum signal amplitude on its input to guarantee a full-scale range operation. A 2^{nd} order $\Delta\Sigma$ ADC composes a modulator and a decimator. The baseband amplifier of the receiver must provide to the ADC a common mode voltage of 800mV (DORNELAS et al., 2015). The peak-to-peak signal is limited to 70% of full scale (600mV) to avoid the ADC modulator overdrive, resulting in maximum peak amplitude of approximately 210 mV(DORNELAS et al., 2015). The input signal that comes in the receiver antenna varies between -123 dBm to -98 dBm. Considering the worst case scenario for the ADC input saturation, i.e., maximum input power, the power that reaches the ADC input must be around -3 dBm, resulting in a maximum gain for the receiver chain of 95 dB. The total gain composes the sum of the gains of each of the receivers blocks: LNA, the mixers, and the baseband amplifier. The ADC might provide an Effective Number Of Bits (ENOB) equal to eight. When the antenna receives the minimum power (-123 dBm), it expects that the minimum resolution of the ADC becomes five bits (assuming the SNR error introduced by quantization is negligible)(NEGREIROS et al., 2015), causing a loss of 3 bits of resolution in the ADC, but even with this loss, the system might work properly.

This project aims a total gain of 30 dB for the RF front-end (LNA + RF mixer), which leaves 65dB of gain for the IF mixer and the baseband amplifier (table 3.1).

Table 3.1: Gain estimation for all receiver blocks

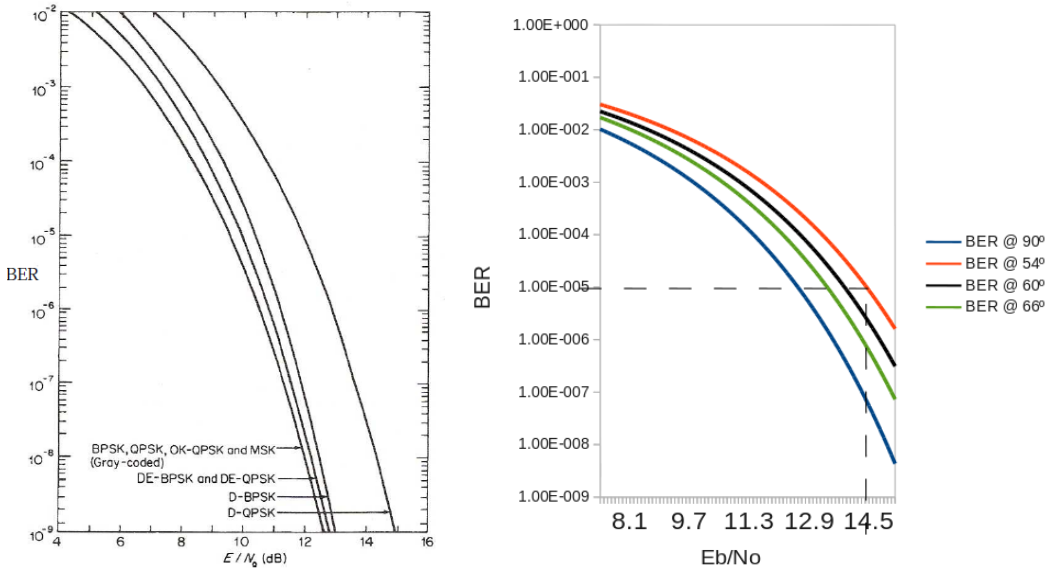
Block	Estimated Gain	Unit
LNA	25	dB
Filter	-5	dB
First Mixer	10	dB
Second Filter	-5	dB
Second Mixer	10	dB
Baseband amplifier	60	dB
Total Gain	95	dB

3.1.2 Noise Figure

It must be analyzed, at the first moment, the modulation scheme that the system will work with, to estimate the noise figure. The type of signal defines which parameter will be observed and analyzed. Regarding analog transmission, the signal-to-noise ratio must be observed, on digital transmission, the Bit Error Rate (BER). The BER measures the performance of the demodulator by counting the number of bits in error, n, in a stream of N received bits (MARAL; BOUSQUET, 2002). Depending on the adopted modulation, the relationship between BER and $\frac{E_b}{N_o}$ (bit energy over noise spectral density) parameter will have different behaviors. Figure 3.2 (a) shows examples of curves of different digital modulation schemes.

Figure 3.2: Bit Error Rate for different phase deviation

(a) BER for different modulation schemes (b) BPSK modulation with phase deviation



Source: (a)-(HAYKIN, 2001); (b)-the author

The SBCDA uses a Binary Phase Shift Keying (BPSK) modulation with a phase

deviation varying between $54°$ and $66°$ (COSTA, 1984). Figure 3.2 (b) shows a relation between BER and $\frac{E_b}{N_o}$ parameter for different incident angles for a BPSK modulation given by equation (3.1).

$$BER = \frac{1}{2} \cdot erfc(\sqrt{\frac{1}{2} \cdot (sin^2(\theta) \cdot \frac{E_b}{N_o})}) \tag{3.1}$$

where $erfc(x) = \frac{2}{\sqrt{\pi}} \cdot \int_x^\infty e^{-z^2} dz$ denotes the complementary error function.

Considering the worst case presented in figure 3.2 (b) in which the incident angle is equal to $54°$ from DCP, it is possible to estimate a value of $\frac{E_b}{N_o}$ for a given BER. For a BER of $1 \cdot 10^{-5}$, according to figure 3.2 (b), we have a ratio $\frac{E_b}{N_o}$ ratio approximately equal to 14.4 dB. With this parameter, it is possible to calculate the signal-to-noise ratio at the output.

The symbol transmission rate R_S, defined as symbols/sec or baud, is given by:

$$R_S = \frac{1}{T_s}$$

The output Signal-to-Noise Ratio (SNR) might be estimated considering a bit rate R_S of 400 bits per second (bps) and a bandwidth of 1.6 KHz (TUDE et al., 1986), according to equation 3.2.

$$SNR_{out} = \frac{E_b}{N_o} \cdot \frac{R}{BW} \tag{3.2}$$
$$SNR_{out} = 14.4 + 10log\frac{800}{1600} = 11.39dB$$

Where:

- R is the Data rate;

- BW is the bandwidth.

The following expression can calculate the noise floor, and it has a value of -141.78 dBm.

$$Noise_{Floor} = kTB \tag{3.3}$$

Where:

K is the Boltzmann constant $= 1.38 \cdot 10^{-23} \frac{J}{K}$;

T is the temperature in Kelvin $= 300.15$ K;

B is the bandwidth = 1.6 kHz.

To calculate the noise figure, we can use the expression:

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{\frac{P_{sig}}{KTB}}{SNR_{out}} \tag{3.4}$$

The minimum input signal that goes to the receiver antenna is -123 dBm, the noise floor has a value of -141.78dBm, so the required noise figure for the receiver is the difference between SNR_{in} and SNR_{out}.

$$NF = Psig_{in}(dB) - Noise_{FLOOR}(dBV) - SNR_{OUT}(dB) \tag{3.5}$$
$$NF = (-123 - 30) - (-171.78) - 11.39 = 7.4dB$$

Table 3.2 shows an estimation of noise figure values for each block of the receiver considering the cascaded effect on each receiver block. The total NF calculation follows the Friis equation (eq. 3.6) which shows that the noise figure of subsequent stages is reduced due to the gain of previous stages, where F (noise factor) is the absolute value of the noise figure and G is the gain of each stage.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \frac{F_4 - 1}{G_1 \cdot G_2 \cdot G_3} + ... \tag{3.6}$$

Table 3.2: NF estimation for all receiver blocks

Block	Estimated NF	Unit
LNA	4	dB
Filter	5	dB
First Mixer	10	dB
Second Filter	5	dB
Second Mixer	10	dB
Baseband amplifier	38	dB
Total NF	6.8	dB

The satellite systems are very susceptible to noise due to their low received signal power. Noise is all undesired signal that comes to the receiving system, impairing the correct reproduction of desired information modulated by the carrier. The noise sources might be: external to the system, through natural sources located on the receiver antenna, or internal sources, generated by the satellite receiver system itself.

3.1.3 Linearity

Signals that come from other communication systems or other carriers in the same frequency domain are called interferers, and they might corrupt the information signal and must be avoided. Table 3.3 lists in the susceptibility field some interferers that appear

in the operating frequency range with their respective power levels (TOSETTO; CIVIDANES, 2014).

Table 3.3: Receiver specifications

Specification	*Limits*	*Unit*
BER	$\leq 1 \cdot 10^{-5}$	
Input Frequency Range	401.635 ± 0.06	MHz
Input Power Range	-123 to -98	dBm
Input impedance	50	Ω
Noise Figure	7	dB
	Susceptibility	
10 MHz to 100 MHz	-75	dBm
200 MHz	-85	dBm
300 MHz	-98	dBm
354 MHz	-112	dBm
462.5 MHz	-45	dBm
600MHz	-85	dBm
800 MHz to 2400MHz	-75	dBm
Max. input power level	-50	dBW

Source: (TOSETTO; CIVIDANES, 2014)

The most significant blocker appears in the frequency of 462.5 MHz with a power of -45 dBm. This project will have as objective a signal at least 10 dB higher than the worst interferer, i.e., -35 dBm of IIP3.

4 LOW NOISE AMPLIFIER

The RF amplifier stage increases the signal power to a level suitable for input to the mixer, and it helps to isolate the local oscillator from the antenna. The increase in signal power level before mixing is desirable due to the noise that the mixer stage introduces is high. The ideal RF amplifier should exhibit a high power gain, a low noise figure, a linear transfer function with wide dynamic range, good dynamic stability, low reverse gain, and sufficient selectivity to prevent the IF image amplification. (KRAUSS; BOSTIAN; RAAB, 1980)

For this narrow band satellite application, the LNA must attend the requirements described in table 4.1 (TOSETTO; CIVIDANES, 2014). In LNA designs, a Common Gate topology exhibits better linearity, reverse isolation and bandwidth than the Common Source topology. However, it suffers from a lower power gain and a high noise figure (HASAN, 2010). A Cascode LNA promises high power gain, satisfactory noise performance, low power consumption and high reverse isolation (ABIDI, 1988) (SONG et al., 2008). In this sense, a tuned Common Source Cascode topology with a conjugate noise matching network at its input is proposed to accomplish the specifications. The output of the LNA connects to an external filter, and a buffer stage was also included to guarantee that the output impedance is close to 50Ω (next stage filter input impedance) without compromising the gain of the amplifier.

Table 4.1: LNA specifications

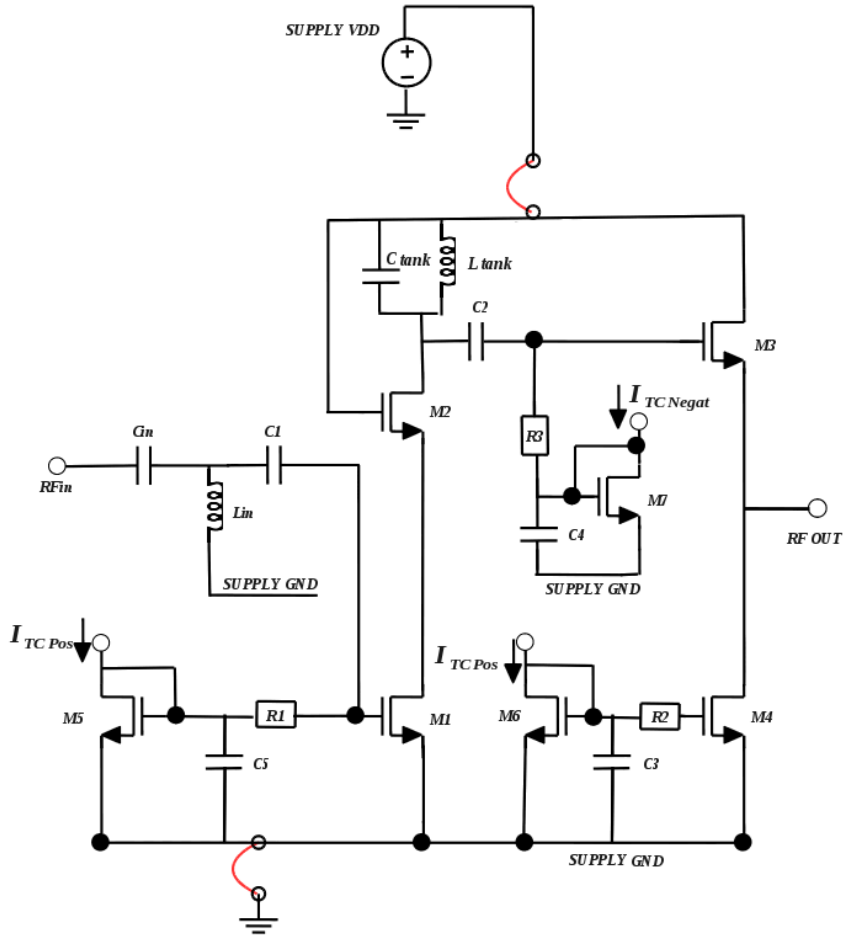
Specification	*Limits*	*Unit*
Input Frequency	401.635	MHz
Input Power Range	-123 to -98	dBm
Input/output impedance	50	Ω
IIP3	≥ -30	dBm
Noise Figure	≤ 4	dB
Gain	≥ 25	dB
Out-of-band gain (@354.2MHz)	$<$ 5dB of the central frequency gain	
Out-of-band gain (@462.5MHz)	$<$ 5dB of the central frequency gain	
Return Loss	$\leq$ -10	dB

Source: (TOSETTO; CIVIDANES, 2014)

4.1 Schematic project

The schematic project composes the cascode project, the buffer and the matching networks (input and output).

Figure 4.1: Common source cascode LNA



Source: The author

4.1.1 Common source Cascode

It was used a gm over I_d approach in order to define a proper polarization of the cascode for the 130nm process, using the following steps:

- To determine a gm that might attend the block specifications;
- To define a proper length;
- Choose a $\frac{gm}{I_d}$ for a given polarization. Large $\frac{gm}{I_d}$ implies in low power and larger signal swings. A smaller $\frac{gm}{I_d}$ provides a high transition frequency (f_T);

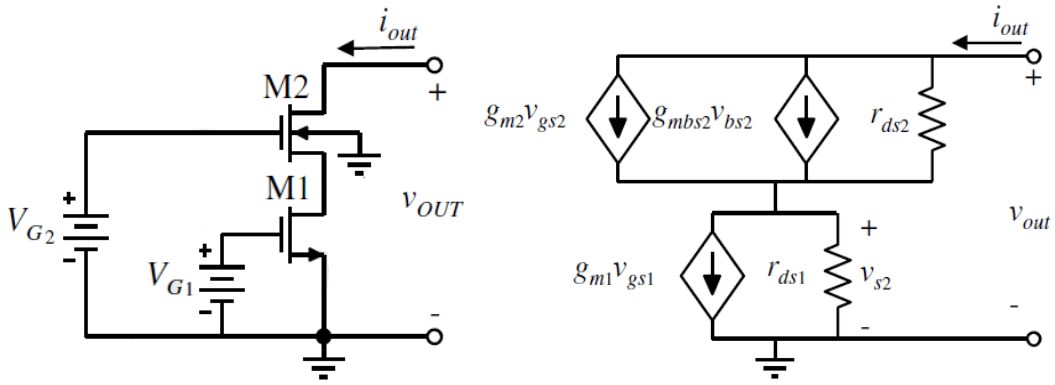
- Determine the initial width of each transistor.

It is possible to make an initial estimation for the transconductance gm of each transistor using as reference the gain specification. Equation 4.1 gives the gain of the Cascode.

$$A_v = gm_{M1} \cdot R_{out} \approx gm_{M1} \cdot gm_{M2} \cdot r_{ds1} \cdot r_{ds2} \tag{4.1}$$

Figure 4.2: Common Source Cascode

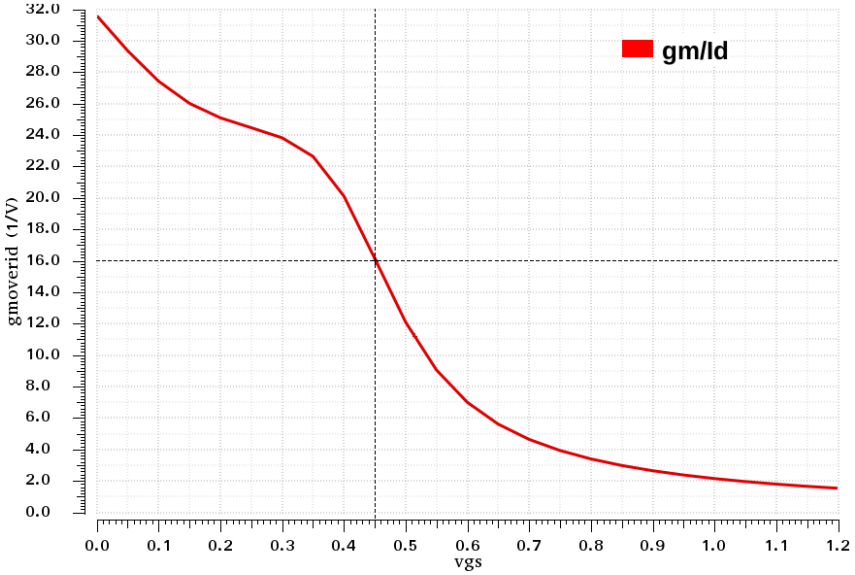
(a) Cascode structure (b) Equivalent Model



Source: the author

The first step is to choose an inversion level for a given V_{gs}. In this project, it was adopted a moderate inversion level for the transistors, so that it will be chosen any value for V_{gs} between 400mV and 600 mV. So, for an initial approach, a value of $V_{gs} = 450mV$ which leads to a $\frac{gm}{I_d} \approx 16$ (figure 4.3).

Figure 4.3: gm over Id curve



Source: the author

Using an initial current of 0.5 mA and a gm of 8 mS, and applying the quadratic model (equation 4.2) of the transistor, it is possible to calculate the value of width (W) of both cascode transistors for a given current (I_d). It was used the minimum length (130 nm) for all transistors to maximize the transit frequency(f_T). The value of $\mu \cdot C_{ox}$ was obtained by parameter extraction procedure on Virtuoso for both NMOS and PMOS transistors.

$$I_d = \frac{1}{2} \cdot \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \tag{4.2}$$

where:
μ is the magnetic permeability;
C_{ox} is the oxide capacitance;
V_{th} is the threshold voltage.

$$\begin{aligned} I_d &= \frac{1}{2} \cdot \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \\ 0.5m &= \frac{1}{2} \cdot 384\mu \cdot \frac{W}{120n} \cdot (618m - 540m)^2 \\ W_{cascode} &= \frac{2 \cdot 0.5m \cdot 120n}{384\mu \cdot (618m - 540m)^2} \\ Wcascode &= 51\mu m \end{aligned} \tag{4.3}$$

The buffer was designed to have an output impedance close to 50 Ω (input filter impedance that comes in the next stage). Equation 4.4 shows the total equivalent impedance at the output of the LNA.

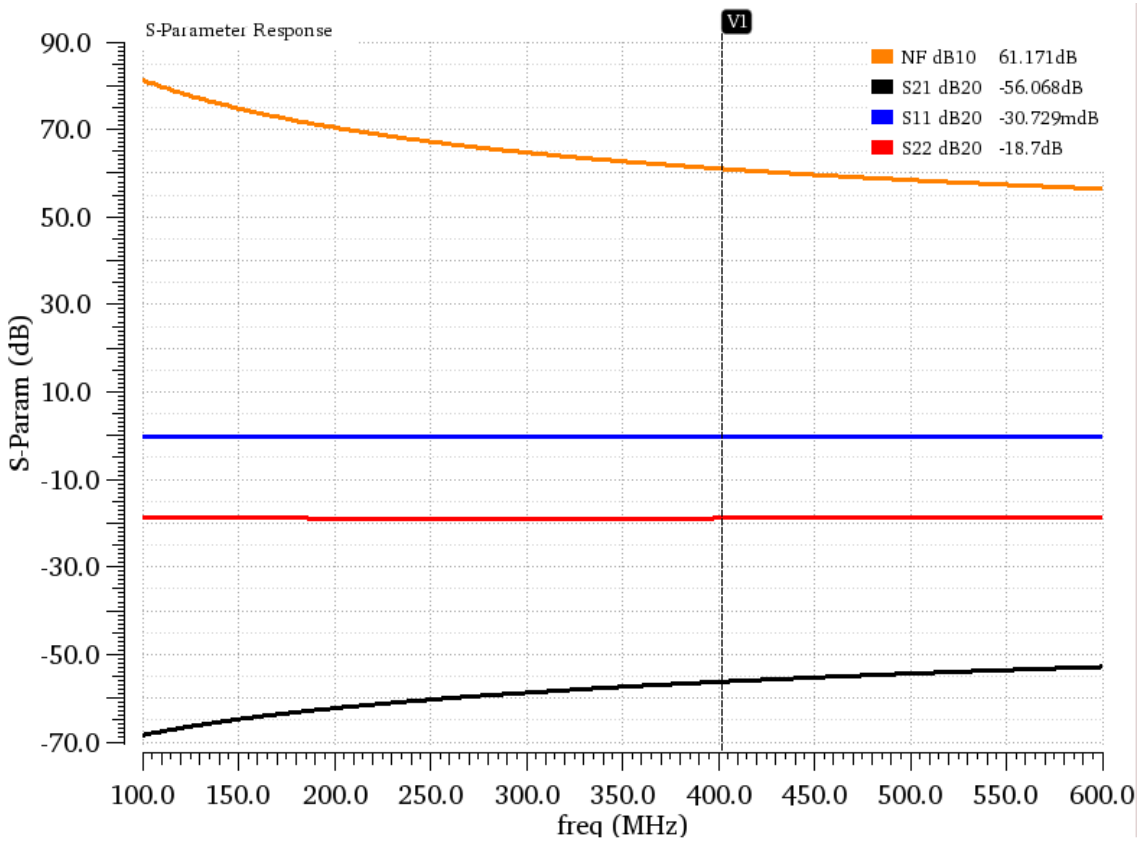
$$R_{out} = \frac{1}{gm_3} // r_{DS4} \approx \frac{1}{gm_3} \tag{4.4}$$

$$\begin{aligned} g_m &= \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th}) \\ 20m &= 384\mu \cdot \frac{W}{180n} \cdot (0.3) \\ W_3 &\approx 30\mu m \end{aligned} \tag{4.5}$$

Transistor M_4 was designed similarly. According to equation 4.5, but using a channel length of 500nm and a V_{on} of 100 mV we have:

$$\begin{aligned} g_m &= \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th}) \\ 20m &= 384\mu \cdot \frac{W}{500n} \cdot (0.1) \\ W_4 &\approx 170\mu m \end{aligned} \tag{4.6}$$

Figure 4.4: LNA results without matching networks



Source: the author

With this initial value, it was possible to make some initial simulations of the main S-parameters. It is possible to see in figure 4.4 that the circuit does not present good results using only the transistors.

It is necessary to tune the input and output to the operating frequency using two different matching networks at the input and output. With the inclusion of matching networks in the project, all of the specifications will achieve proper values. After a few simulation iterations, a modification in the width of transistors to 64 μm for both cascode transistors was necessary, and an S-parameter simulation was performed to extract the Z-parameters to obtain the value of the input and output impedance. Those iterations were necessary due to the limitation of the value of all passive components (inductors and capacitors) that are available in this technology. The following subsections will show the design of the matching networks.

4.1.2 Output Matching Network

The output matching network is intended to tune the output at the operational frequency of 401.635 MHz. An LC tank circuit is connected in the drain of the cascode transistor M2 to achieve this objective. So it is necessary to choose proper values for the inductor and capacitor in a way that the equivalent impedance would be centered as close as possible to the resonance frequency of 401.635 MHz, according to equation (4.7). The final matching value might present a small deviation from the hand designed value due to the value of real components that the technology provides and some parasitic capacitance of the NMOS transistor M_2 (C_{dd}), but the obtained tuning frequency is still close to the desired one.

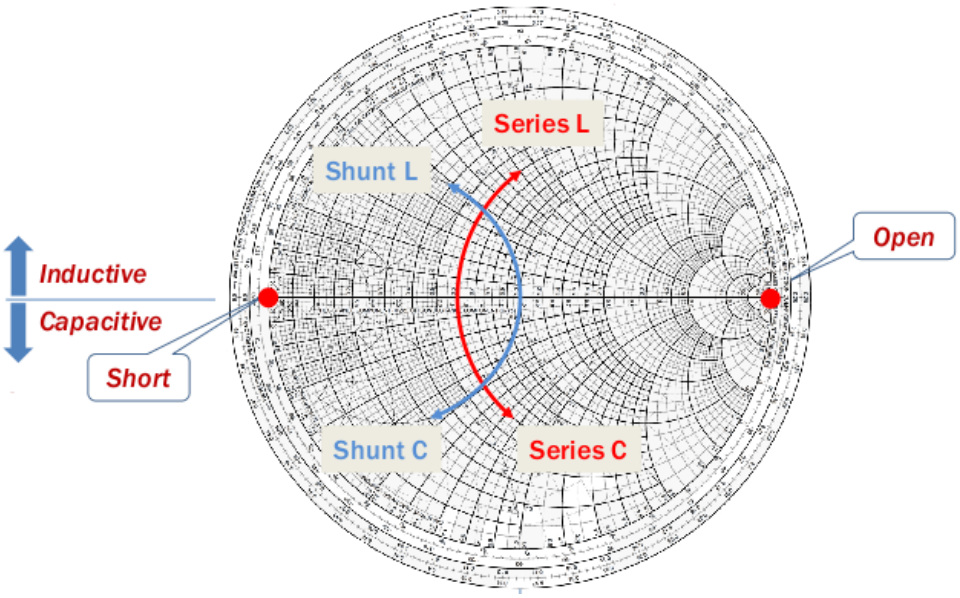
$$\begin{aligned} \omega_{out} &= \frac{1}{\sqrt{L_{tank} \cdot C_{eq}}} \\ 2 \cdot \pi \cdot f_{out} &= \frac{1}{\sqrt{L_{tank} \cdot (C_{tank} + C_2 + C_{dd}(M_2))}} \\ 2 \cdot \pi \cdot f_{out} &= \frac{1}{\sqrt{70.472nH \cdot (2.02pF + 262fF + 8.24fF)}} \\ f_{out} &= 396.26MHz \end{aligned} \tag{4.7}$$

4.1.3 Input matching network

The input matching network was designed using the noise circle methodology in the Smith Chart. Capacitors connected in parallel and inductors connected in series are inclined to increase the total impedance. Similarly, capacitors connected in series and inductors connected in parallel are inclined to increase the total admittance. Resistors dislocate the point to the extremities of the chart (open and short circuit points). Figure 4.5 exemplifies the behavior of passive components in the chart moving from load to the generator. In particular, for the Virtuoso Cadence software, the circles are plotted considering the opposite direction, i.e., from the generator to the load, so the circle's displacement goes in the opposite direction of the ones that figure 4.5 indicates, but the final result remains the same.

Running an S-parameters simulation without a matching network, it is possible to plot noise circles that vary its values from 1dB (inner circle) to 10dB (outer circle) as shown in figure 4.6. Each circle represents a locus of constant NF value for different

Figure 4.5: Passive components behavior on Smith Chart



Source: Department of Electronic Engineering, NTUT (adapted)

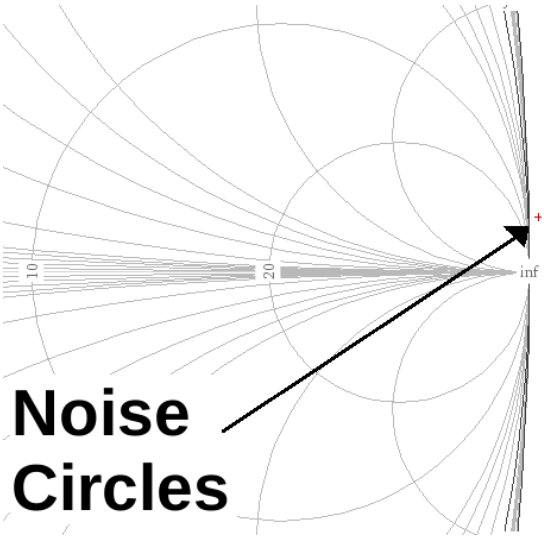
input impedance. It is necessary to move the center of the desired noise circle, adding increasing passive components, going as close as possible to the center of Smith Chart to achieve proper impedance matching.

Besides this, the input matching network also affects the available gain of the circuit. It is possible to use the same strategy that was used to achieve a desired noise figure to obtain a proper gain. In this case, with the same S-parameters simulation, it is possible to plot Available Gain Circles (AGC) (figure 4.7), which represents a locus of constant power gain for different input impedance. The ideal matching network must satisfy a trade-off of maximizing the power gain while minimizing noise figure.

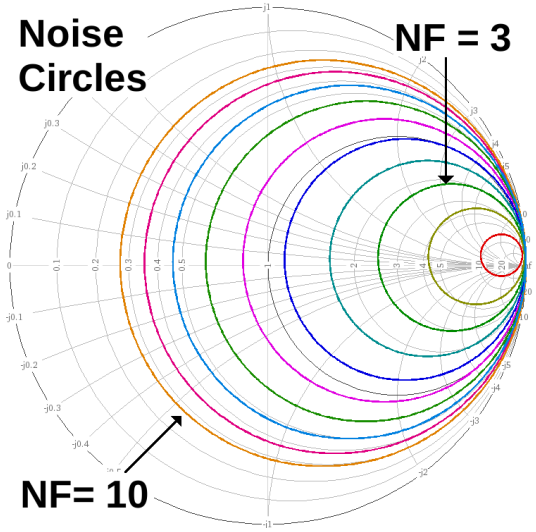
Choosing a noise figure value of approximately 3 dB and a power gain of 25 dB we can choose in the Smith Chart a start impedance point that will be used to reach the center of the chart which has a normalized impedance of 50 ohms.

Figure 4.6: Noise circles (dB)

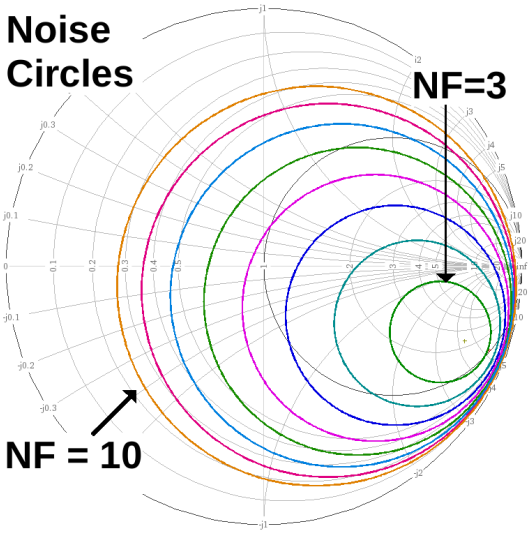
(a) Without a matching network



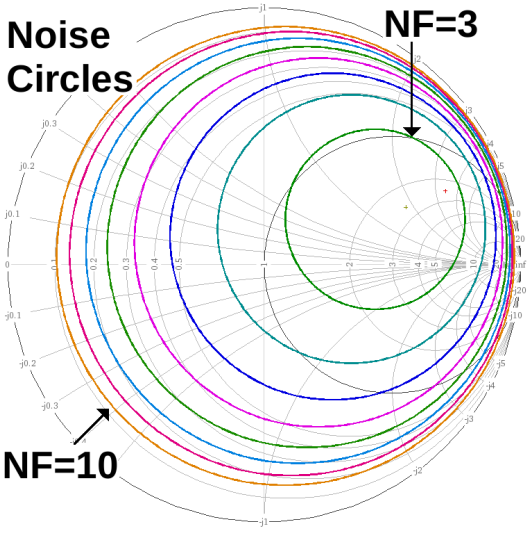
(b) 1^{st} Series capacitor (C_1)



(c) Parallel inductor (L_{in})



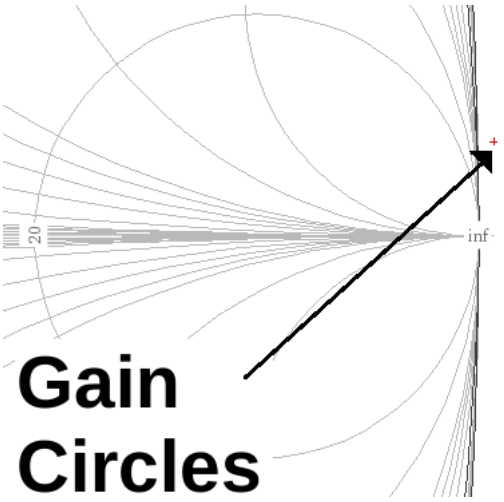
(d) 2^{nd}Series capacitor (C_{in})



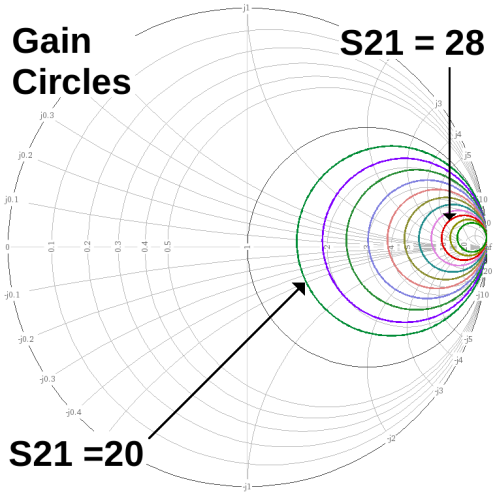
Source: the author

Figure 4.7: Available Gain circles (dB)

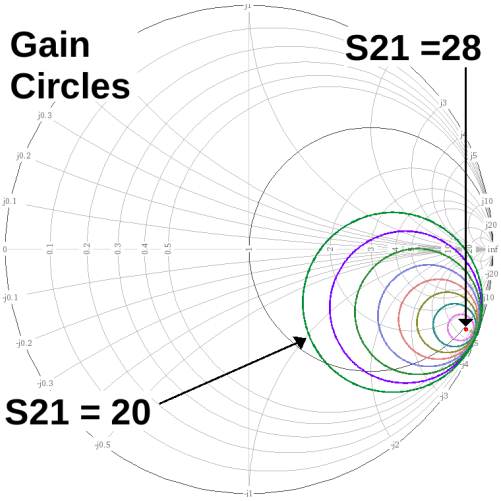
(a) Without a matching network



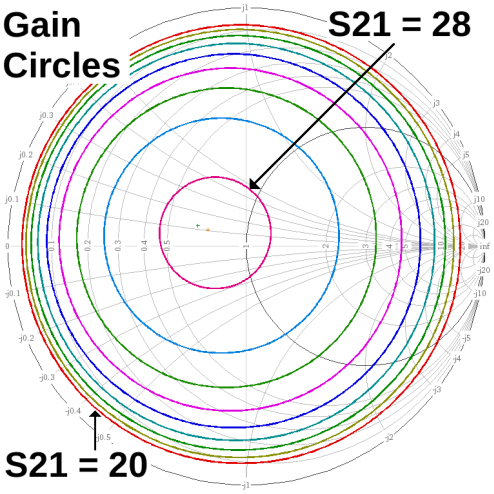
(b) 1^{st} Series capacitor (C_1)



(c) Parallel inductor (L_{in})



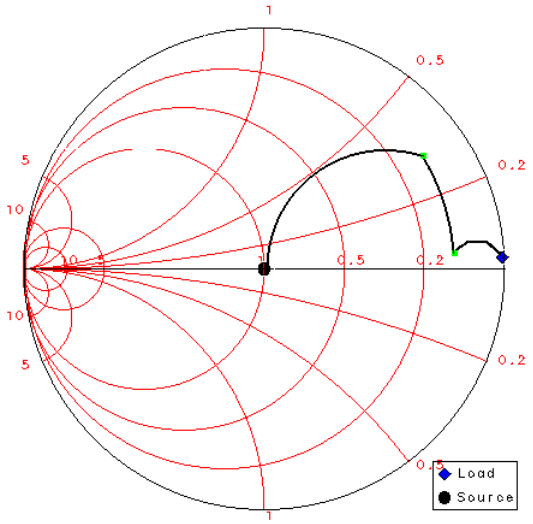
(d) 2^{nd}Series capacitor (C_{in})



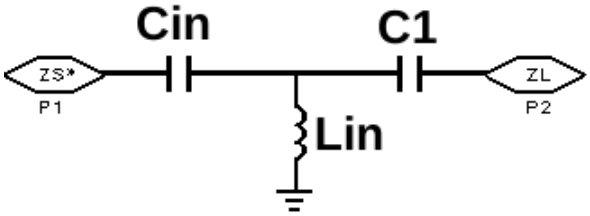
Source: the author

Figure 4.8: Choice of passive components in the Smith Chart for the input impedance matching

(a) Impedance displacement in the Smith Chart



(b) Final input matching network



Source: the author (extracted from ADS software)

Z_{in} is the input impedance of 50 ohms (typical impedance of an antenna), and Z_L is the impedance seen from the decoupling capacitor connected at the gate of the cascode transistor of the LNA. With an S-parameter simulation, it is possible to quickly obtain the input impedance of the LNA using the Z-parameters results (Z_{11}). This LNA has an impedance $Z_L = 163.5 + j500$, which results in a normalized impedance of $\overline{Z_L^*} = 3.27 + j10$, it must be defined which matching network will dislocate this impedance to the center of the chart. Many combinations of matching networks are possible to implement. The choice of components, or the matching network, will depend on technology restrictions (e.g., components that cannot vary its nominal value), available area, quality factor.

For this work, the addition of LC components makes the the input impedance close to 50 Ω using the path described in figure 4.8(a). Figure 4.8(b) shows a similar circuit that corresponds to this matching network.

The following steps are needed, to determine the value of each component of the matching network:

1. To determine the load impedance (circuit impedance);

   With an S-parameter simulation, it was plotted some noise circles to obtain the initial impedance point for the load. This project aims a final noise figure of $\approx$ 3.5 dB. In the Smith Chart, the initial point that might provide this value of noise figure is the center of correspondent noise circle, i.e., an impedance point $Z_L =$

$240 + j36.5\Omega$

2. To normalize the load impedance to 50 Ω (Smith Chart impedance);

$$\overline{Z_L^*} = \frac{Z_L}{50} = 4.8 + j0.73\Omega \tag{4.8}$$

3. To choose in the Smith Chart a proper impedance point that results from the displacement caused by the addition of a passive component (figure 4.5);
   Selecting the impedance points Z_L, Z_{P1}, and Z_{P2}, using the Smith chart and figure 4.8 (a) as a reference:

$$Impedances = \begin{cases} \overline{Z_L} = 4.8 + j \Rightarrow (Y_L = 0.2 - j41.6m); \\ \overline{Z_{P1}} = 2.77 - j2.51 \Rightarrow (Y_{P1} = 0.2 + j0.18); \\ \overline{Z_{P2}} = 2.77 + j1.4 \Rightarrow (Y_{P2} = 0.287 - j0.145); \end{cases}$$

4. To calculate a denormalized value of each element of the matching network.

   - Shunt inductor (L_{in}) To calculate the value of shunt inductor it must be measured the difference between the imaginary parts of the **admittance** of P_1 ($Y_{P1} = \frac{1}{Z_{P1}}$) and the load ($Y_L = \frac{1}{Z_L}$) and denormalize it, as shown in equation (4.9)

$$\begin{aligned} \Delta ImY_{P1_L} &= 0.18 - (-41.6m) \approx 0.22 \\ \Delta ImY_{P1_L} &= \frac{50}{\omega \cdot L_{in}} = 0.22 \\ 0.22 &= \frac{50}{2 \cdot \pi \cdot 401.635M \cdot L_{in}} \\ L_{in} &= 89.41nH \end{aligned} \tag{4.9}$$

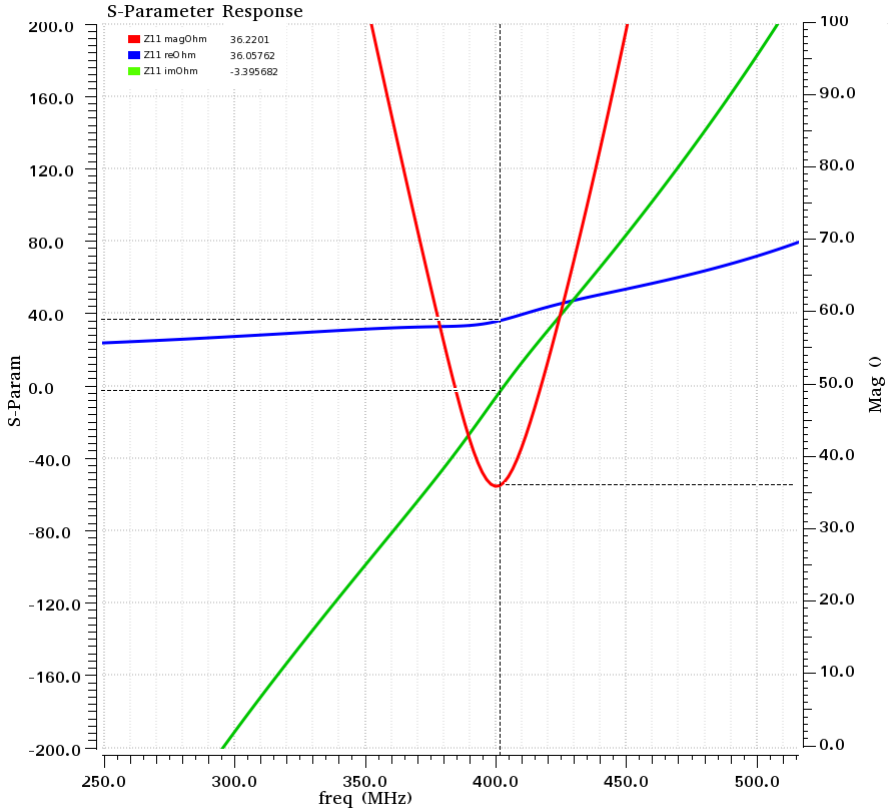
   - Series Capacitor (C_{in}) It must be measured the difference between the imaginary parts of the **impedance** of P_2 (Z_{P2}) and P_1 (Z_{P1}) and denormalize it to calculate the value of the series capacitor, as shown in equation (4.10)

$$\begin{aligned} \Delta ImZ_{P1_{P2}} &= 1.4 - (-2.51) = 3.91 \\ \Delta ImZ_{P1_{P2}} &= \frac{\frac{1}{\omega \cdot C}}{50} = 3.91 \\ 3.91 &= \frac{1}{2 \cdot \pi \cdot 401.635M \cdot C_{in} \cdot 50} \\ C_{in} &= 2pF \end{aligned} \tag{4.10}$$

With the insertion of the passive components in the circuit, the location of noise circles and the power gain circles will also change. Figures 4.6 and 4.7 exemplify this behavior. It is possible to say just by inspection on both graphs that the LNA provides an NF of $\approx$ 3.5 dB and a power gain of $\approx$ 28 dB using this matching network.

Trade-offs that were adopted to achieve all the specifications compromises the perfect matching. Figure 4.9 shows the final input impedance. The initial idea was to match the circuit to a 50 Ω impedance but due to the possible values of the component that IBM technology provides it was achieved with this matching network an input impedance of $\approx$ 36 Ω. The capacitor value changed to 1.42 pF after simulations, and the inductor value was the same as calculated. Although the circuit deviates from the perfect matching to an impedance of 50 Ω, it still will work correctly.

Figure 4.9: Input impedance after the inclusion of matching network

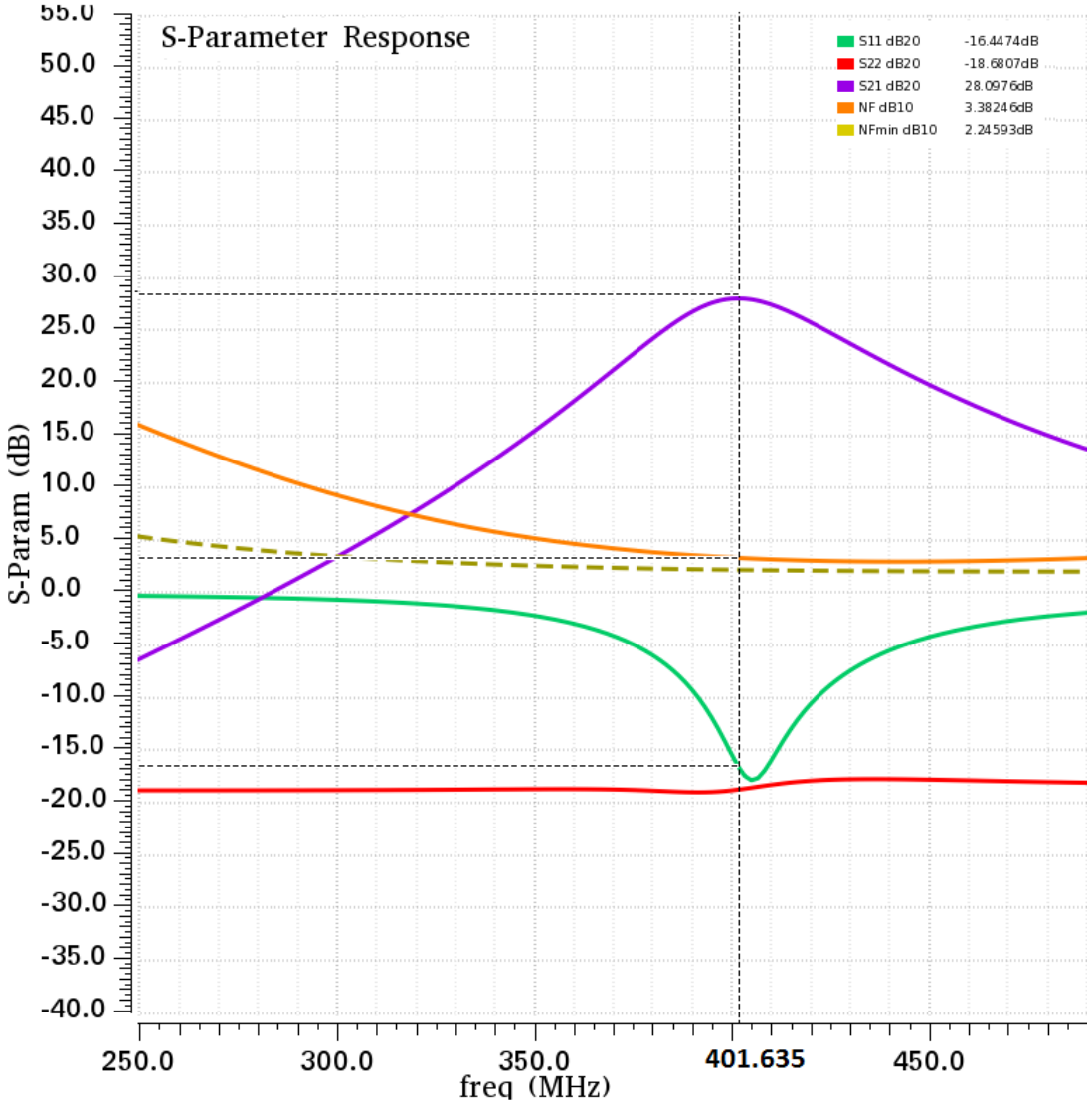


Source: The author

4.1.4 Nominal results

After defining all of the components, it was performed an S-parameter simulation to evaluate the performance of Low noise amplifier. The S-parameter simulation provides information on power gain, Noise Figure, Return Loss and stability of the LNA. Figure 4.10 summarizes the result. After the inclusion of the matching networks, the power gain, noise figure and return loss specifications achieved the initial objectives listed on table 4.1. It must be set a two-tone test to measure the linearity specification of the LNA.

Figure 4.10: Schematic nominal results



Source: The author

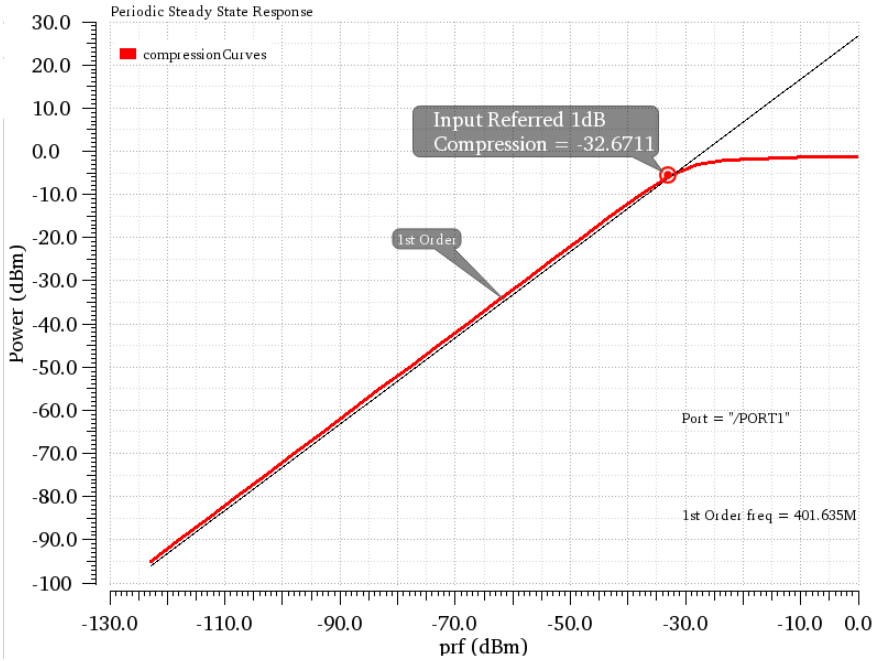
It was necessary to run a two-tone test with a Periodic Steady State (PSS) analysis and a Periodic Alternated Current (PAC) analysis to measure the 1dB compression point (1dBCP) and the third order input intermodulation product (IIP3). Both tones have the

same amplitude, and 1 MHz separate them from each other, so the first tone was defined at the frequency of 401.635 MHz and the second tone at the frequency of 402.635 MHz.

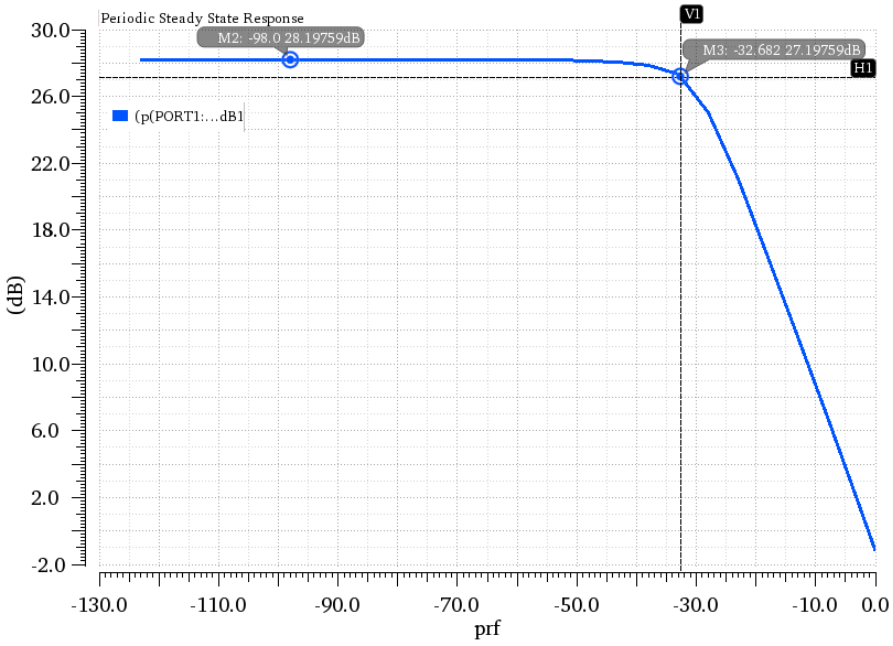
The 1dBCP is the power value that corresponds to a decrease of 1dB from the 1^{st} order curve as shown in figure 4.11(a). Alternatively, it can be measured directly from the power gain curve marking the point that falls 1 dB from the maximum power gain value, as shown in figure 4.11(b).

Figure 4.11: 1dBCP

(a) Typical 1dBCP plot



(b) 1dBCP using power gain curve



Source: The author

If we apply to a nonlinear system two interferers at ω_1 and ω_2, the output generally exhibits components that are harmonics of these frequencies. Let us assume that $x(t) = A_1 \cdot cos(\omega_1 t) + A_2 \cdot cos(\omega_2 t)$. Thus:

$$y(t) = \alpha_1 \cdot x(t) + \alpha_2 \cdot x(t)^2 + \alpha_3 x(t)^3 \tag{4.11}$$

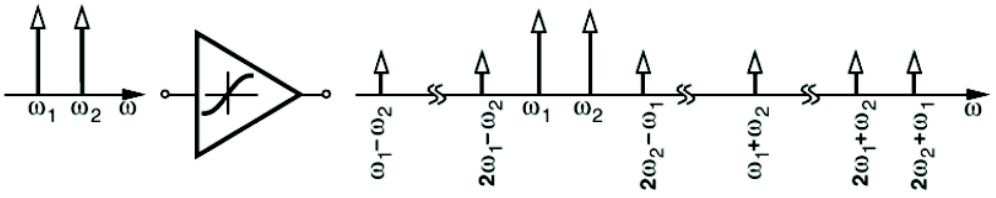
$$\begin{aligned} y(t) = {} & \alpha_1 \cdot (A_1 cos\omega_1 t + A_2 cos\omega_2 t) + \\ & + \alpha_2 \cdot (A_1 cos\omega_1 t + A_2 cos\omega_2 t)^2 + \\ & + \alpha_3 \cdot (A_1 cos\omega_1 t + A_2 cos\omega_2 t)^3 \end{aligned} \tag{4.12}$$

Expanding the right-hand side of equation (4.12) and considering only the components at ω_1, ω_2, and $\omega_1 \pm \omega_2$:

$$\begin{aligned} y(t) = {} & (\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2) cos(\omega_1 t)) + \\ & + (\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2) cos(\omega_2 t) + \\ & + \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 + \omega_2) + \frac{3\alpha_3 A_1^2 A_2}{4} cos(2\omega_1 - \omega_2) + \\ & + \frac{3\alpha_3 A_1 A_2^2}{4} cos(\omega_1 + 2\omega_2) + \frac{3\alpha_3 A_1 A_2^2}{4} cos(\omega_1 - 2\omega_2) \end{aligned} \tag{4.13}$$

The third order intermodulation products $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ are of particular interest because they appear in the vicinity of ω_1 and ω_2 and they might corrupt the information signal.

Figure 4.12: Intermodulation products

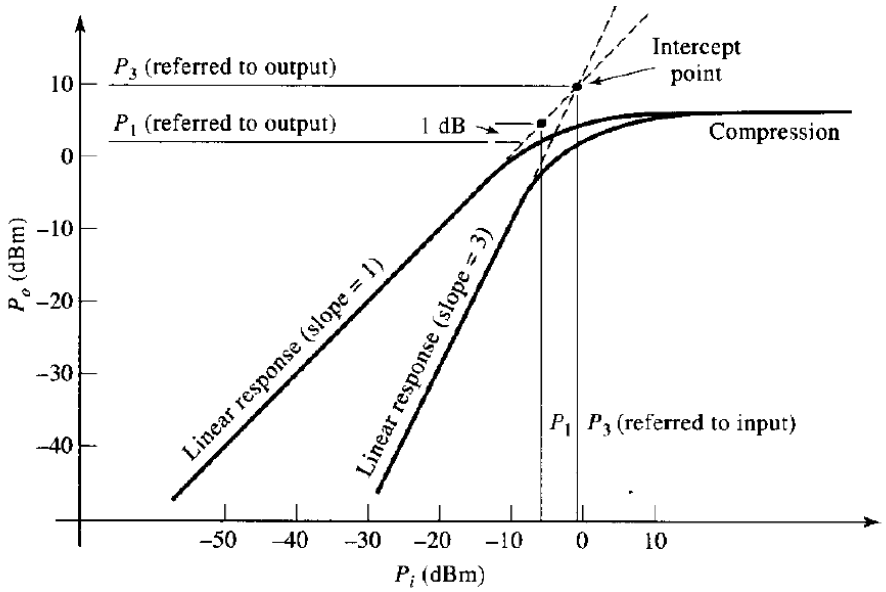


Source: (RAZAVI, 2011)

It is necessary to find the extrapolation point of the 3^{rd} order power curve that is equal to the 1^{st} order curve to calculate the IIP3, as shown in figure 4.13.

An alternative way to calculate the N^{th} intermodulation product is using equation (4.14), where P_{in} is the input power and (ΔP) is the difference between the desired output signal and the undesired N^{th} order output intermodulation product in dB is shown

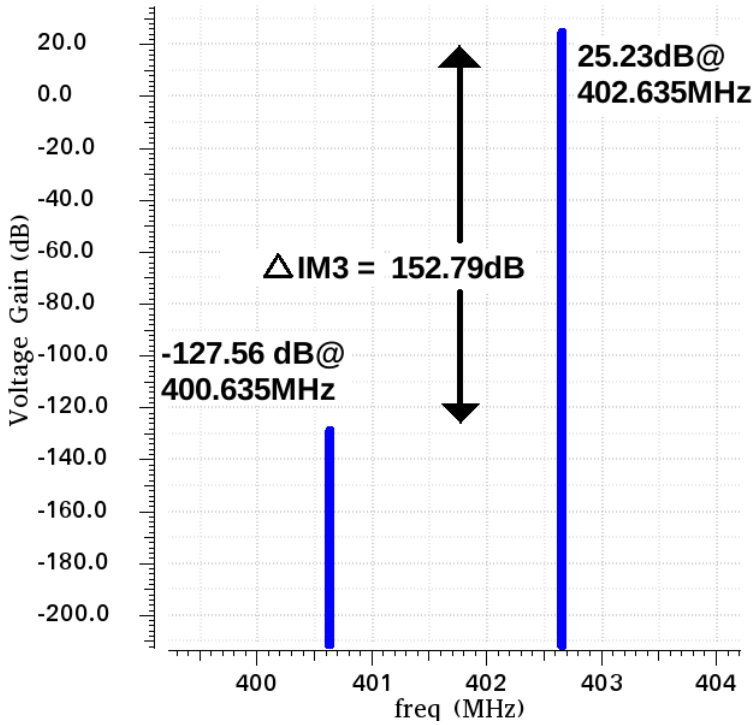
Figure 4.13: Typical IIP3 plot



in figure 4.14. In particular, for N =3, P_{in}= -98 dBm, (ΔP = ΔIM3) the IIP3 can be calculated.

$$IPN = P_{in} + \frac{\Delta P}{N-1} = -98dBm + \frac{152.79}{2} = -21.6dBm \tag{4.14}$$

Figure 4.14: IIP3



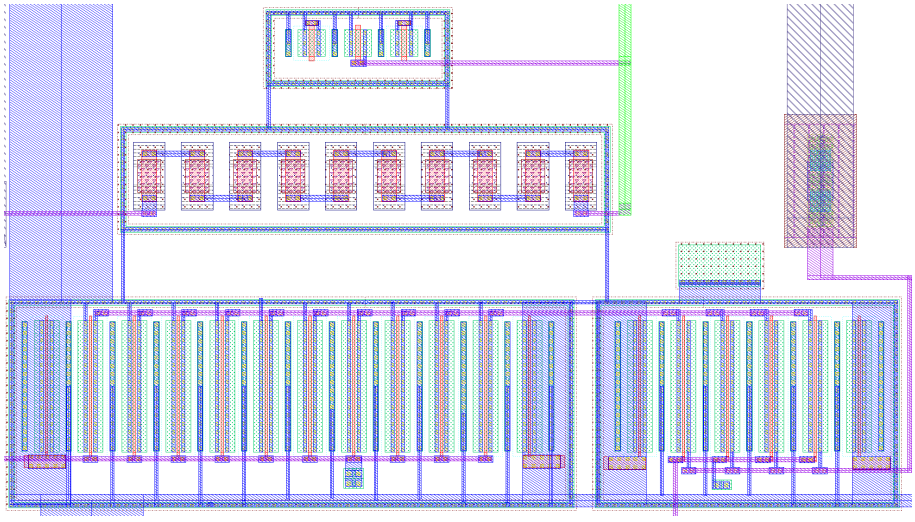
Source: The author

4.2 Layout

The layout of an RF circuit is a crucial step in the design because the parasitic capacitance addiction that appears in the layout might jeopardize the desired specifications. It is essential, therefore, to use some layout techniques to avoid or minimize the effect of the parasitic in the circuit.

A typical layout practice is to decompose a large transistor into parallel transistors of smaller widths with the use of multipliers to limit the noise contribution brought about by increased device widths due to increased gate resistance, R_g. This technique not only reduces R_g but it also reduces junction capacitance. Double contacted gates might also provide further reductions in gate resistance. The disadvantages of this distribution include the increase in the required gate-source and gate-drain vias and the increase in gate-bulk parasitic. Constraints on matching and symmetry and also dummy transistors were used to minimize the mismatch between the components. It was a concern in this project that the transistors should have the same width, differing only by the number of multipliers, to make a proper matching between the devices.

Figure 4.15: Common source cascode structure



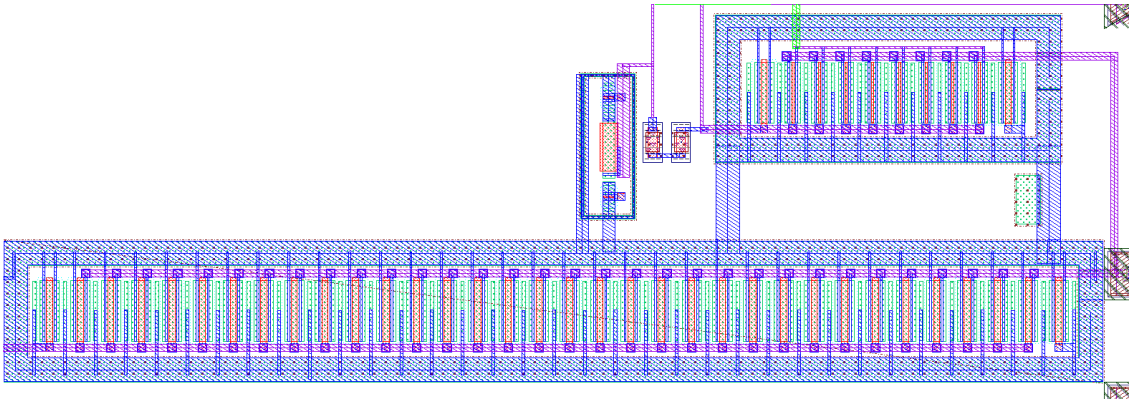
Source: The author

The cascode and the buffer were displaced using these techniques as can be seen in figures 4.15 and 4.16. It was prioritized to use symmetric structures using multipliers instead of fingers to maintain the same current flow in each structure allowing a small parasitic capacitance on each structure. Also, dummy structures were added to each extremity of the transistors to minimize the mismatch effect that might appear due to the manufacturing process.

Some techniques minimize the noise in the circuit. Often the ground and supply voltages of analog and digital blocks are separated, strong contacting to the substrate is essential not only to shunt substrate noise to the ground but also for latch-up prevention. Ground-shields are another way to shunt substrate noise away from devices such as resistors, MIMs, and bond pads. They offer protection against any potential interferer signal that comes to a sensitive net.Critical signal wires were kept away from other nets as far as possible to reduce capacitive coupling.

Some design rules must be followed to avoid electromigration in the circuit. Electromigration is a phenomenon caused by high current densities that pass through a rail that might cause its complete rupture. They define a maximum allowed current per width that might pass through a rail. Depending on the technology, or of which metal used in the manufacturing process, the width value might change. Typical values are 2 $\frac{mA}{\mu m}$ or 1 $\frac{mA}{\mu m}$ (HASTINGS, 2005). Figure 4.16 exemplifies the concern about electromigration. The buffer stage of the LNA consumes around 10 mA, so it was necessary to include a thick guard ring (of $\approx$ 10 μm) to avoid a possible rupture. Since the transistor are split into many devices (by using multipliers), they can support the total current that is divided equally among them. The number of vias depends on the maximum current that a single via supports. The resistance of the wire can cause IR-drops which means that the DC level of that specific lossy wire can change the designed value. The resistance value will depend on the type of metal and the number of vias.

Figure 4.16: Buffer



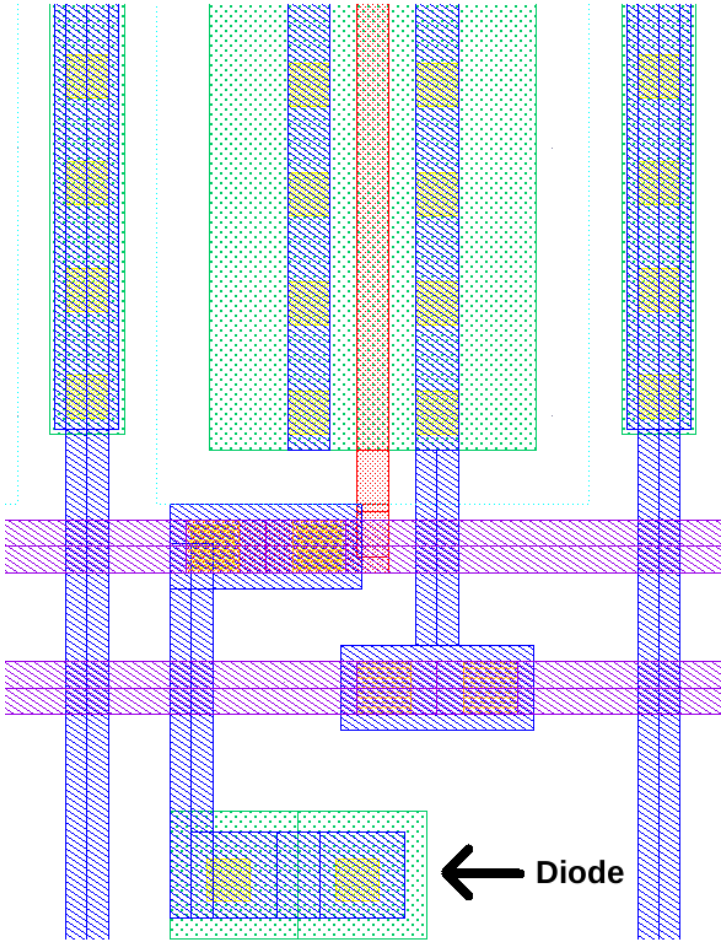
Source: The author

An excessive current might damage the bondwires of the circuit as well. If a large current passes through the amplifier it might cause rupture of the bondwire, so, to solve this problem, multiple bondwires might be required to "split" the excessive current.

Thin gate oxides are subject to charging damage during wafer processing. If the

gate charges to a sufficient potential, the gate oxide will break down. Gate oxide damage in transistors result in a degradation of device reliability, with increased gate current, transconductance and threshold voltage shifts over time. This phenomenon is called antenna effect and providing an alternate discharge path from the gate node to the substrate can avoid it.

Figure 4.17: Diode tie down inserted in the layout



Source: The author

Some design solutions might be adopted to reduce antenna effect in the circuit such as:

- Breaking signal wires into multiples layers, routing to upper metal layers and returning to lower metal layers.
- The addition of extra gates in the circuit (with dummies) will allow making the capacitance ratio between the problematic gate and metal layer smaller, reducing, therefore, the antenna effect.
- The inclusion of reversed biased diodes provides an alternative path to charges flow

instead of going to the gate of the transistor.

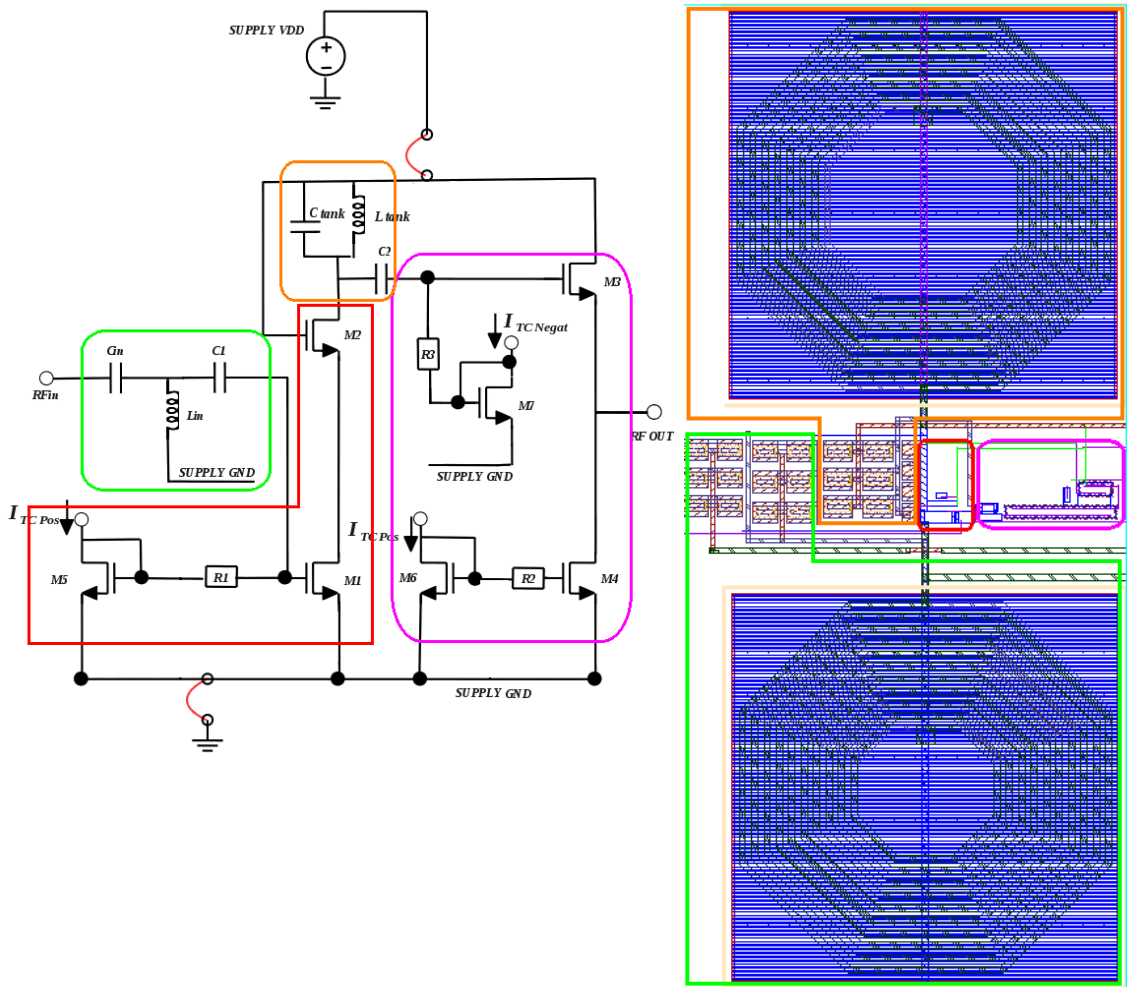
In this project, it was added a nTiedown diode in the final layout to solve the identified antenna problems in the final layout, as shown in figure 4.17.

Figure 4.18 shows the final LNA layout. It was a concern the placement of each structure, as well as the routing techniques to avoid inherent parasitic capacitance and mutual interference between the components.

The total occupied area of this LNA is 794 μm X 357 μm.

Figure 4.18: Final LNA structure

(a) LNA Schematic (b) LNA layout

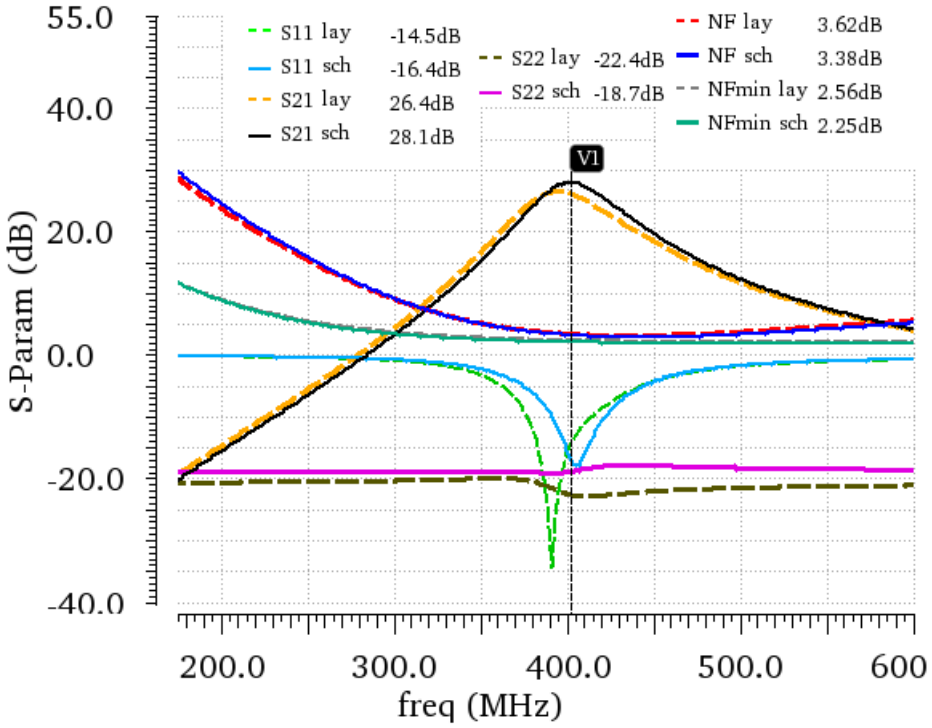


Source: The author

4.3 Post-layout simulations

Upon completion of the layout, it is necessary to extract the parasitic capacitance that might change the schematic results.

Figure 4.19: Comparison between nominal and extracted results



Source: The author

Figure 4.19 shows the S-parameters and NF for schematic and post-layout simulation with the Assura RC typical (RCtyp) extraction. The dashed curves represent the layout extracted results and the solid lines the schematic results. The gain and noise figure results were similar in the schematic and layout. The S_{11} parameter deviates a little from the initial. Figure 4.19 shows that the input matching network tunes the circuit $\approx$ 380 MHz. The effect of the wire bonding might compensate this value because it will add some parasitic inductance and consequently will slightly increase the input matching frequency to a value close to the desired frequency of 401.635 MHz. The wire bonding usually adds about 1nH of inductance per millimeter of wire.

The power consumption of the LNA, including the output buffer, is 6.53 mW.

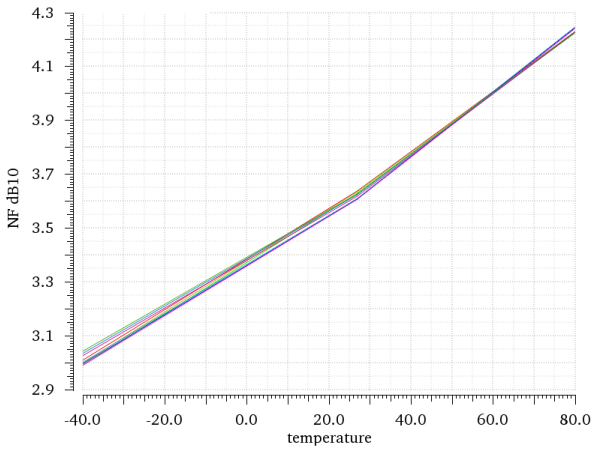
4.4 Corners Analysis

4.4.1 Temperature coefficient

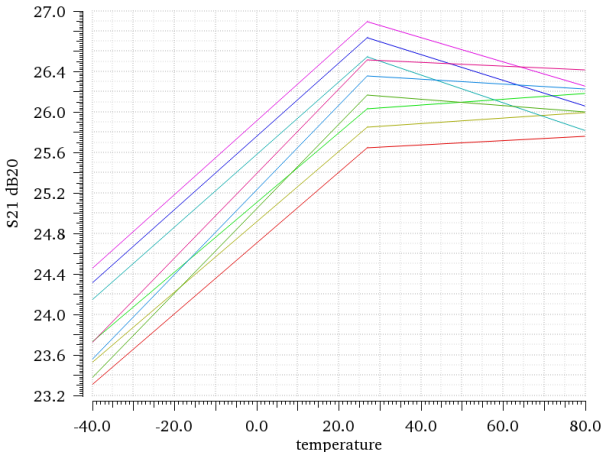
It was simulated a corners analysis to verify the functioning of the circuit under extreme conditions, varying the temperature and supply voltage from its nominal values. The supply voltage varied from 1.08 V to 1.32 V (10%), the temperature varied from -40° C to 80° C ((LANDIECH et al., 2010)) and it also included some transistor variation including fast and slow operation modes for each transistor.

Figure 4.20: Corner analysis

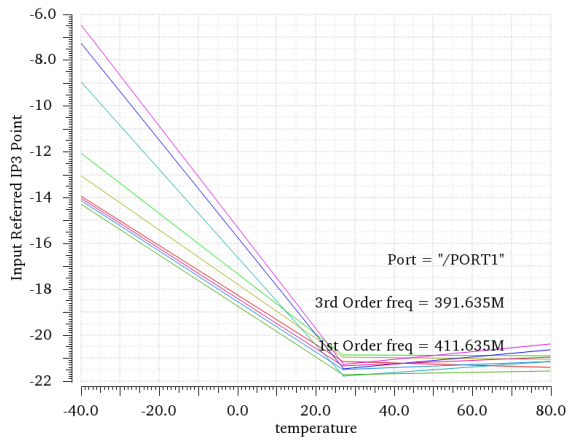
(a) Noise figure corner



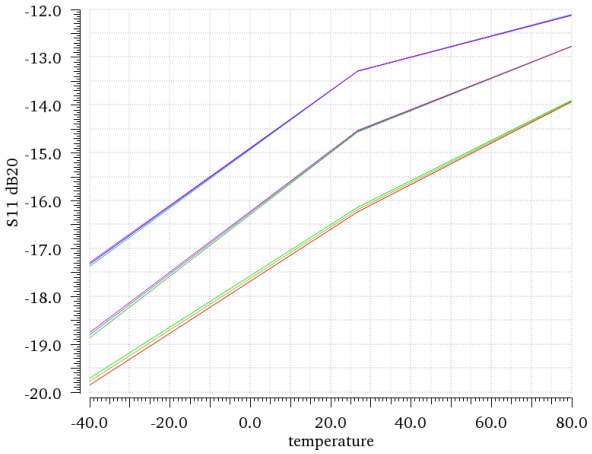
(b) Power gain corner



(c) IIP3 corner



(d) Input return loss corner



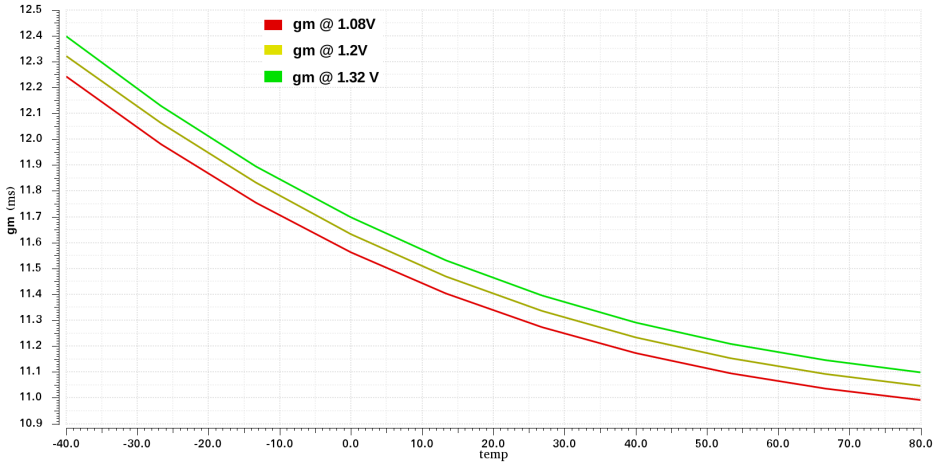
Source: The author

In this project, three current mirrors are used to bias the LNA with 25μA each. To make compensation for this variation in temperature it is important to determine which design variables mainly act degrading the noise behavior at 80 degrees. Sensitivity analysis identifies which parameter is more relevant to control on both stages (transconductance

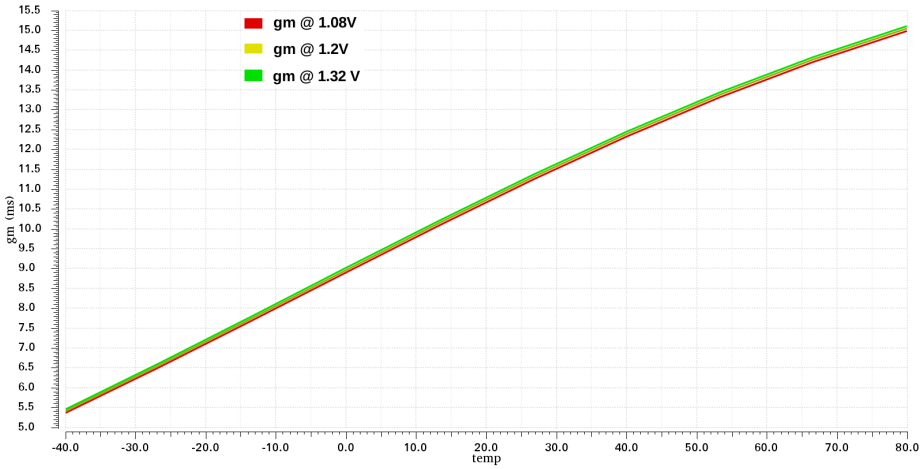
and the buffer stage). The main noise contribution in the transconductance stage comes from the common source transistor that receives the signal at the gate (transistor M1 fig. 4.1). The transconductance parameter (gm) of this transistor plays a primary role in the overall noise contribution. If gm decreases (due to the increase in temperature) the noise figure increases because the current in this branch decreases, which causes a smaller gain and consequently a higher noise figure. So the transconductance from the common source transistor has an inverse relation concerning NF (figure 4.21 (a)). To make compensation for this inverse relation, a current source with a positive temperature coefficient might provide a proportional increase in current with the temperature to modify this different behavior (figure 4.21 (b)).

Figure 4.21: gm behavior with variation of temperature and VDC

(a) Without temperature compensation



(b) With temperature compensation



Source: The author

To identify a reasonable value from temperature compensation a parametric analysis was made to identify which positive temperature coefficient (TC) would present a

proper result for this temperature variation. In this way, it will increase the robustness of the transconductance stage of the LNA.

The signal behavior has to be analyzed to find the design variable that has the most significant influence on the noise contribution in the buffer stage. The buffer stage is responsible for matching the output from the LNA with 50 Ω. As known, the seen output impedance is a parallel equivalent between a drain point of view from the bottom transistor (large impedance) with a source point of view from the top transistor (lower impedance and then, the approximate equivalent value). That means that the transconductance determines the output impedance from the top transistor (1/gm). The transconductance cannot be too different from 20 mS, or the output does not match with the external matching network. The Common Drain transistor allows the voltage gain to be close to 1. The design variable that measures the inversion channel is the relation gm/Id. So the channel inversion must be the lower as possible. To maintain a $\frac{gm}{I_d}$ as constant as possible, a current source that decreases in value with the increase in temperature is needed.The same parametric analysis was made to determine the appropriate value from the temperature coefficient that maintains the channel inversion as constant as possible.

Tables 4.2 and 4.3 show all specifications considering PVT variations.

Table 4.2: LNA Corner results

Metric	*Specification*	*Min*	*Max*
1dBCP	≥ -40	-32.42	-27.56
IIP3	≥ -30	-21.78	-6.47
S11	≤ -10	-19.86	-12.1
S22	≤ -10	-57.73	-14.75
S21	≥ 20	23.31	26.9
NF	≤ 4	2.98	4.24

Table 4.3: LNA Worst corner

Metric	*value*	*VDD*	*Temp.*	*model*
1dBCP	-32.42	1.08 V	80	tt
IIP3	-21.78	1.08 V	27	ss
S11	-12.1	1.08 V	80	ss
S22	-14.75	1.08 V	-40	ff
S21	23.31	1.08 V	-40	ff
NF	4.24	1.08 V	80	ss

4.5 MonteCarlo Analysis

It is necessary to make a variability analysis in the circuits to test possible variations on the manufacturing of integrated circuits because its final performance is affected. The variability divides itself between mismatch and process variability. That means that it is possible to find variations that affect identically designed devices at one die in equal manner (process variations), and in different manner (mismatch variations).

The process variability gives an uncertainty degree around a mean value of the devices, i.e., it affects equally all devices in the same die and does not cause mismatches in the circuit.

There are two main types of mismatch: global or local. The global mismatch presents variation gradient of the devices parameters in a wafer that will cause a mismatch, i.e., the distance of the devices affects the variation of them. The local mismatch is a random mismatch, and it is not possible to predict its exact value, so it is quantified by its standart deviation.

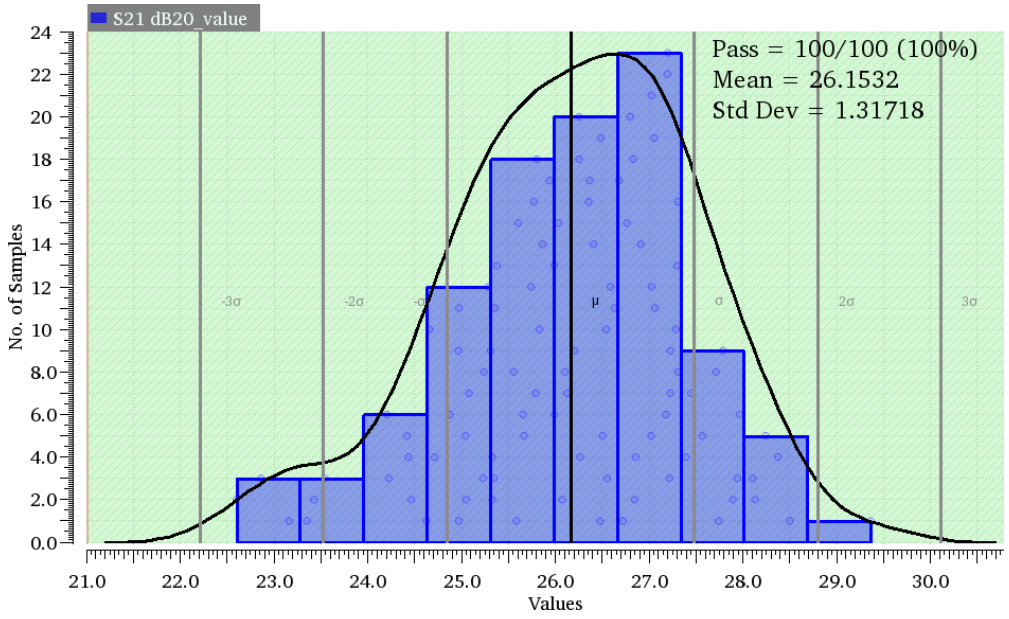
In this project, it was attempted to minimize the variability using some layout techniques described on previous layout section, like matched devices, the proximity between devices, fingers and multipliers, symmetry, current orientation, and dummies.

In this sense, it is necessary to run a Monte Carlo simulation to perform process variations and mismatch contributions in the circuit and also obtain a statistical result that informs the number of samples that will work adequately after the manufacturing process. Figures 4.22, 4.23 and 4.24 show the statistical results of all LNA specifications for a total of 100 samples. Samples located in red areas in the graphs indicate that the circuit fails with the specification limit in those samples.

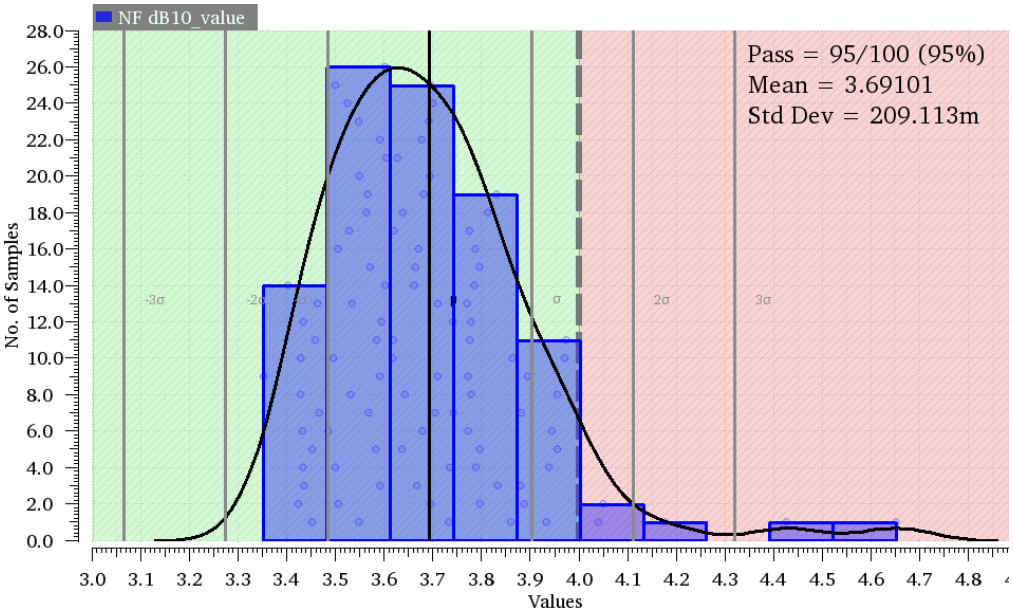
The histograms show that all the metrics are passing the initial specification except for the noise figure specification that fails for 5% of the samples. Although this value of noise figure is above the expected initial specification, it will not compromise the performance of the whole receiver with the inclusion of mixers.

Figure 4.22: LNA gain and NF MonteCarlo analysis

(a) S_{21} Monte Carlo - Specification: S_{21} > 20 dB



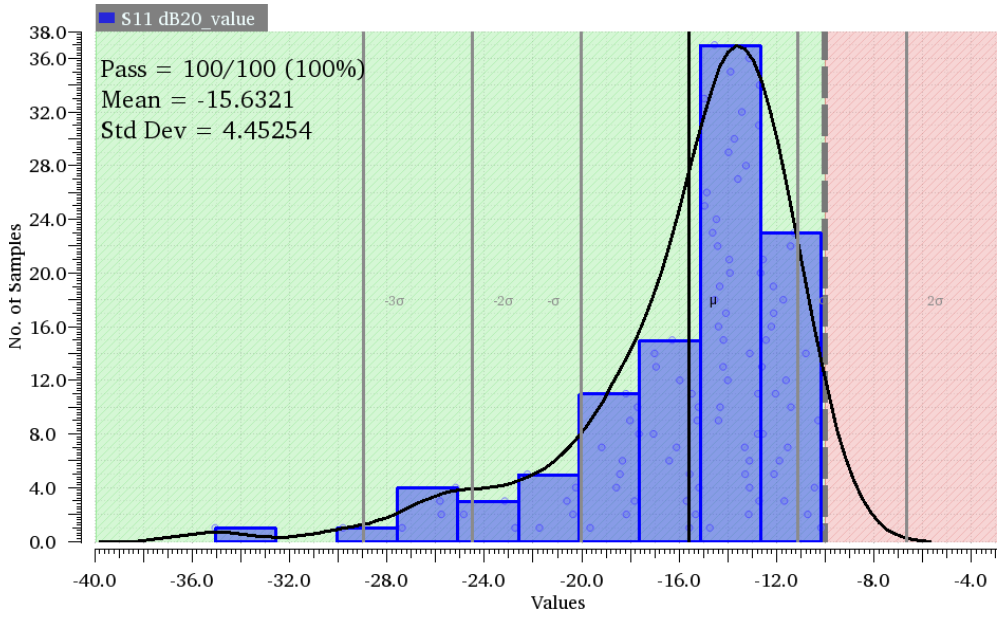
(b) NF Monte Carlo - Specification NF < 4 dB



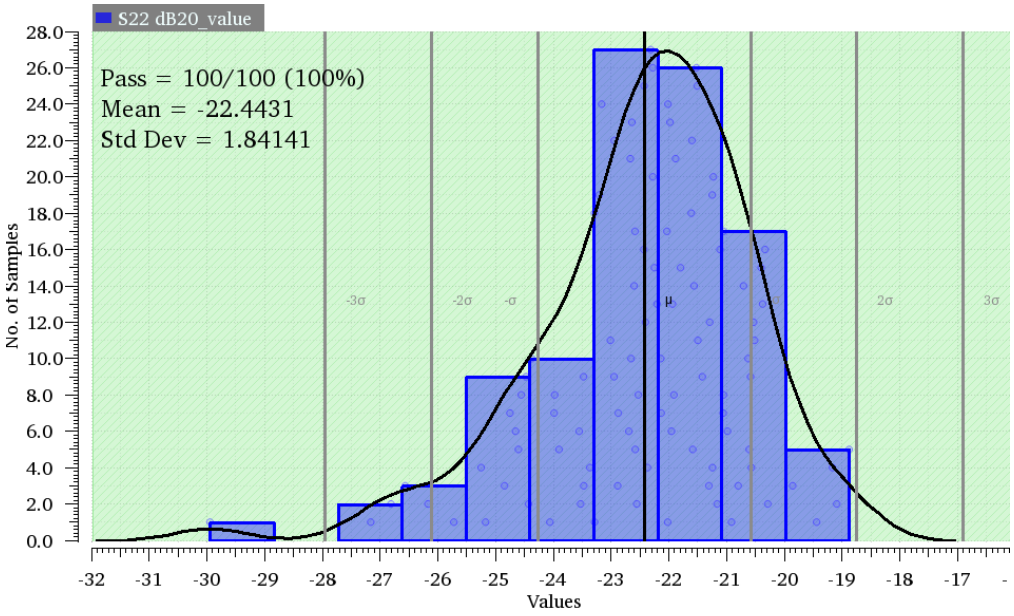
Source: The author

Figure 4.23: LNA S_{11} and S_{22} MonteCarlo analysis

(a) S_{11} Monte Carlo - Specification: S_{11} < -10 dB



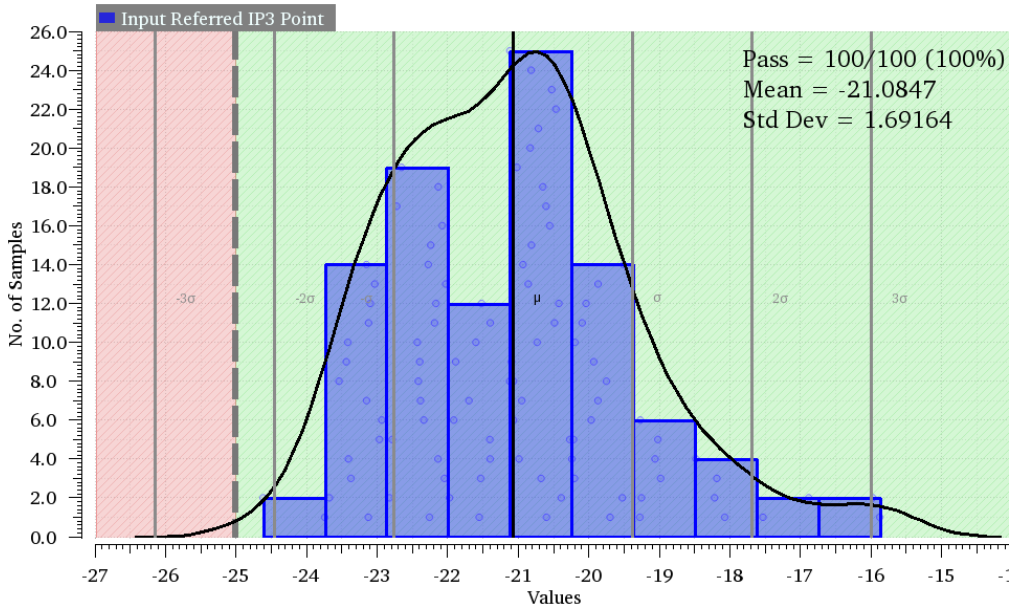
(b) S_{22} Monte Carlo - Specification: S_{22} < -10 dB



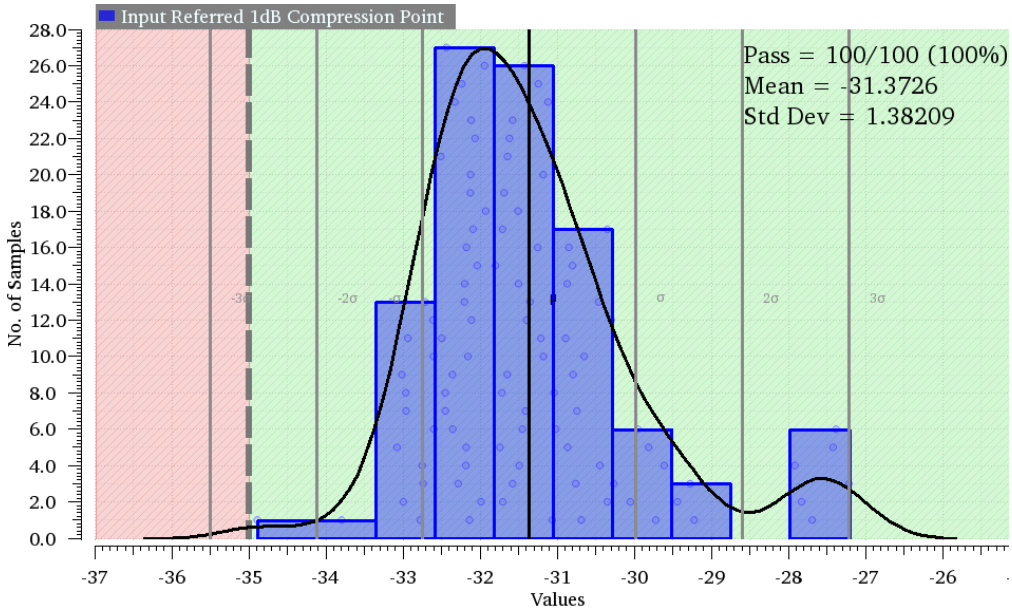
Source: The author

Figure 4.24: LNA IIP_3 and 1dBCP MonteCarlo analysis

(a) IIP_3 MC - Specification: IIP_3 > -25 dBm



(b) 1dBCP MC - Specification: 1dBCP > -35 dBm



Source: The author

4.6 Figure of Merit

The design of low noise amplifiers aims for small noise figures and higher gains with low power consumption and good linearity for a given operational frequency. In this sense, a Figure of Merit (FoM) (SOUZA; MARIANO; TARIS, 2017) that involves all those metrics is defined to compare different LNA topologies. Equation 4.15 details the figure of merit of LNAs.

$$FoM = \frac{Gain \cdot IIP_3 \cdot f(MHz)}{(F-1)P_{dc}(mW)} \tag{4.15}$$

$$NF = 10log(F) \tag{4.16}$$

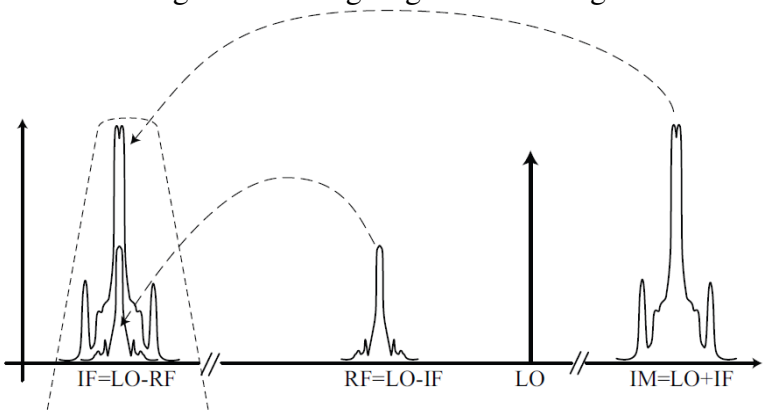
Here f is the frequency (in GHz), F is the noise factor (eq. 4.16), G is the gain of the LNA, IIP_3 is the input referred third-order intercept point and P_{DC} the DC supply power. Note, that gain and IIP3 are taken as absolute values and not on a decibel scale.

This project consumes a total of 6.53 mW, it has 3.62 dB of noise figure, 26.4 dB of gain and -21.6 dBm of IIP_3 for a 401.635 MHz of operational frequency (parasitic extracted results). These values give a total FoM of -142.72.

5 IMAGE REJECTION FILTER

Due to the mixer characteristics, a combination of input (RF) and the local oscillator (LO) signals generates an undesired signal, called image (IM) signal. If this image enters into the mixer, it will also shift this image signal to the intermediary frequency (IF) and it corrupts the information, so it is necessary the inclusion of a filter stage in the architecture to remove the image, called image rejection filter.

Figure 5.1: Image signal and RF signal



Source: (NIKNEJAD, 2016b)

In this project, we have an RF signal at 401.635 MHz, a LO signal at 377.92 MHz and therefore an image signal at 354.205 MHz. A bandpass filter was implemented to solve this image problem aiming the specifications shown in table 5.1.

Table 5.1: Bandpass Filter specifications

Specification	*Limits*	*Unit*
Low 3 dB Frequency	376.635	MHz
High 3 dB Frequency	426.635	MHz
Minimun rejection @ 354.2 MHz	20	dB
Minimun rejection @ 462.5 MHz	20	dB
Bandwidth	50	MHz

The adopted filter design procedure (TAYLOR, 2006), which includes a project of an equivalent lowpass filter for further conversion to a bandpass filter, will be explained

in a sequence of steps as follows:

1. Determination of central frequency (f_o)

$$f_o = \sqrt{f_L \cdot f_H} \tag{5.1}$$
$$f_o = \sqrt{377.635M \cdot 426.856M}$$
$$f_o = 400.856MHz$$

where f_L and f_H are the low and high 3dB frequencies, respectively.

2. Desired rejection

It must be calculated for the frequencies f_1 (Minimum rejection frequency of 354.2 MHz) and f_2 (Minimum rejection frequency of 462.5 MHz) a geometrically related stopband frequency pairs to obtain a proper rejection, according to equations 5.3 and 5.5.

$$f_o^2 = f_1 \cdot f_2 \tag{5.2}$$
$$(400.856M)^2 = 354.2M \cdot f_2$$
$$f_2 = 453.66MHz$$

$$f_2 - f_1 = 453.66M - 354.2M = 99.458MHz \tag{5.3}$$

$$f_o^2 = f_1 \cdot f_2 \tag{5.4}$$
$$(400.856M)^2 = f_1 \cdot 462.5M$$
$$f_1 = 347.428MHz$$

$$f_2 - f_1 = 462.5M - 347.428M = 115.072MHz \tag{5.5}$$

Table 5.2 resume these calculations.

Table 5.2: Bandpass Filter specifications

f_1	f_2	$f_2 - f_1$ *(BW)*
354.2 MHz	*453.66 MHz*	99.458 MHz
347.428 MHz	**462.5 MHz**	115.072 MHz

3. Steepness factor (A_s) We are interested in the most restrictive values, i.e., it will be used the lowest bandwidth value of 99.458 MHz with 20 dB of rejection. With the geometric bandwidth values and the initial specification bandwidth, it is possible to calculate a normalization factor called Steepness Factor (A_S), defined as:

$$A_S = \frac{BW_{20dB}}{BW_{3dB}} \tag{5.6}$$
$$A_S = \frac{99.458M}{50M}$$
$$A_S = 1.99$$

4. Choice of the normalized lowpass filter

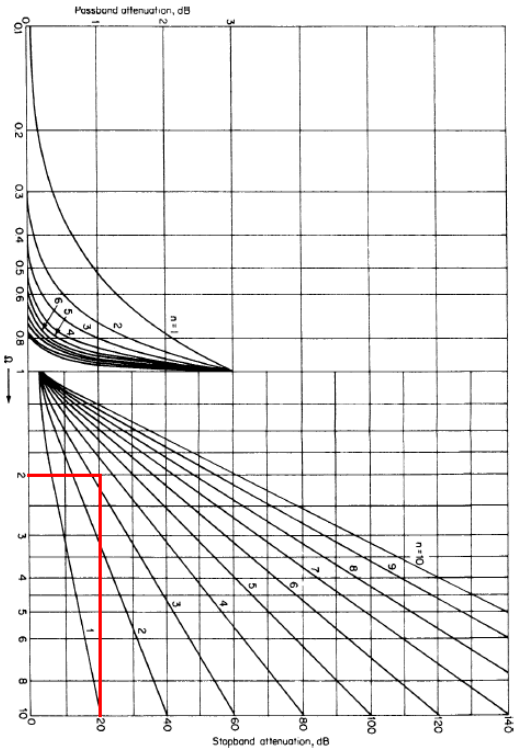
   The choice of normalized lowpass filter was made using as a reference figure 5.2. The normalized filter is required to have over 20 dB of rejection at 1.99 rad/s. According to figure 5.2, it is possible to choose any of the following options:

$$Options = \begin{cases} 3^{rd} order Butterworth Filter; \\ 3^{rd} order 0.01 dB ripple Chebyshev Filter; \\ 3^{rd} order 0.1 dB ripple Chebyshev Filter; \\ 3^{rd} order 0.25 dB ripple Chebyshev Filter; \end{cases}$$

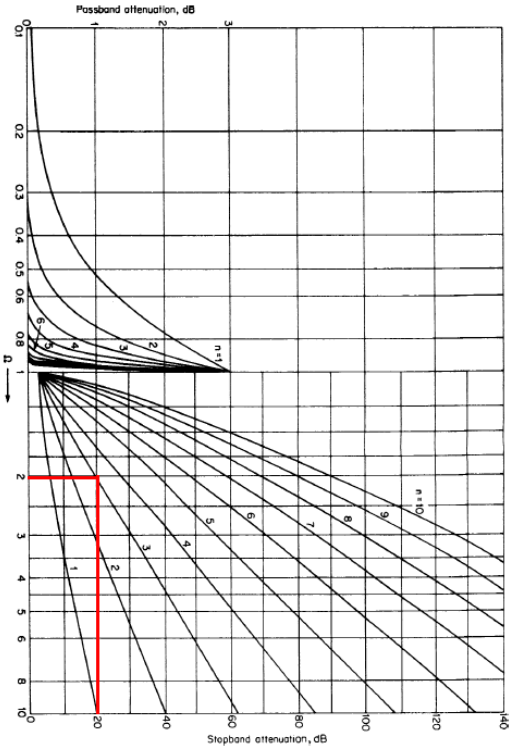
   The 0.1dB and 0.01dB Chebyshev filters could solve the problem, but with no margin for variations. The project specifications would be too tight using these filters. The 0.25dB Chebyshev filter attends the requirements as well as the Butterworth filter, so, it was chosen a 3^{rd} order Butterworth Filter, to guarantee a proper functioning, for presenting a flat band represented by figure 5.3.

Figure 5.2: Lowpass filters order vs attenuation (dB)

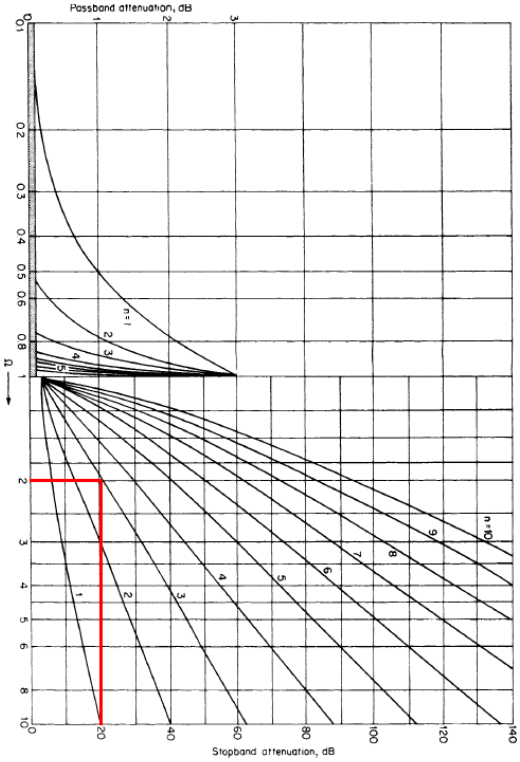
(a) Butterworth Filter



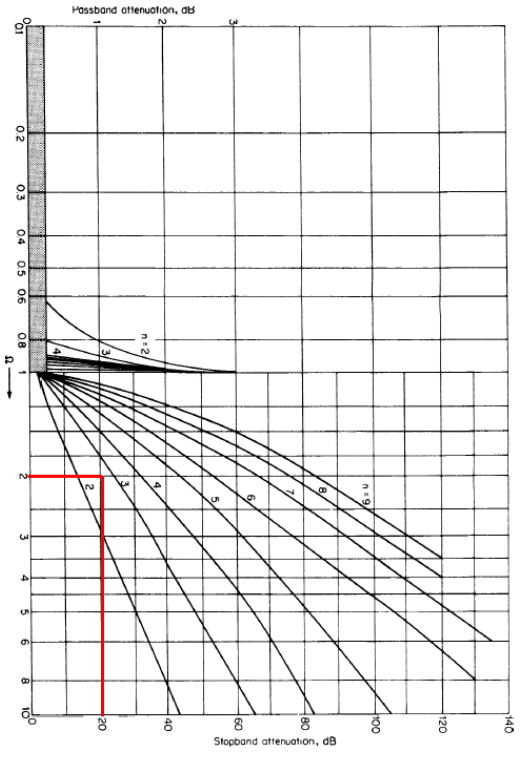
(b) Chebyshev filter with 0.01 dB ripple



(c) Chebyshev filter with 0.1 dB ripple



(d) Chebyshev filter with 0.25 dB ripple

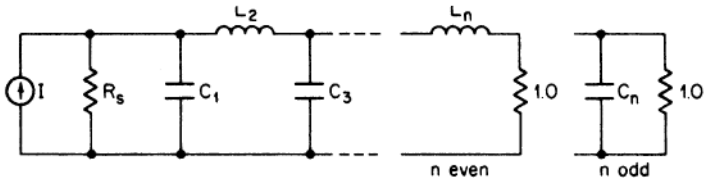


Source: (TAYLOR, 2006)

The value of each component depends on the relation between input and output impedance. In this case, the filter uses the same value of 50 ohms for both input

and output impedance, so the values of capacitors C_1 and C_3 are equal to 1 and L_2 is equal to 2 for a 3^{rd} order Butterworth filter.

Figure 5.3: Butterworth LC element values



n	R_s	C_1	L_2	C_3	L_4
2	1.0000	1.4142	1.4142		
	1.1111	1.0353	1.8352		
	1.2500	0.8485	2.1213		
	1.4286	0.6971	2.4387		
	1.6667	0.5657	2.8284		
	2.0000	0.4483	3.3461		
	2.5000	0.3419	4.0951		
	3.3333	0.2447	5.3126		
	5.0000	0.1557	7.7067		
	10.0000	0.0743	14.8138		
	Inf.	1.4142	0.7071		
3	1.0000	1.0000	2.0000	1.0000	
	0.9000	0.8082	1.6332	1.5994	
	0.8000	0.8442	1.3840	1.9259	
	0.7000	0.9152	1.1652	2.2774	
	0.6000	1.0225	0.9650	2.7024	
	0.5000	1.1811	0.7789	3.2612	
	0.4000	1.4254	0.6042	4.0642	
	0.3000	1.8380	0.4396	5.3634	
	0.2000	2.6687	0.2842	7.9102	
	0.1000	5.1672	0.1377	15.4554	
	Inf.	1.5000	1.3333	0.5000	

Source: (TAYLOR, 2006)

5. Denormalization

Defining the parameter "Frequency Scaling Factor" (FSF) as:

$$FSF = 2 \cdot \pi \cdot BW \tag{5.7}$$

$$FSF = 2 \cdot \pi \cdot 50M$$

$$FSF = 314.16MHz$$

$$C'_1 = C'_3 = \frac{C}{FSF \cdot R_L} \tag{5.8}$$

$$C'_1 = 63.66pF$$

$$L'_2 = \frac{L \cdot R_L}{FSF} \tag{5.9}$$

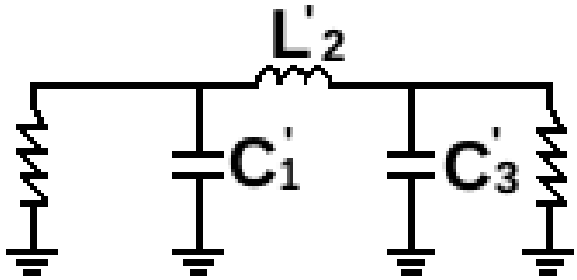
$$L'_2 = 318.31nH$$

(5.10)

where C'_1 , C'_3, and L'_2 are the denormalized filter components C_1, C_3, and L_2,

respectively. Figure 5.4 shows the final low-pass filter.

Figure 5.4: 3^{rd} order Butterworth low-pass filter

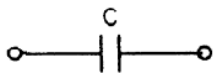
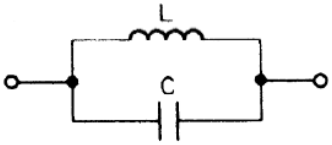
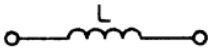
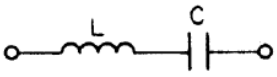
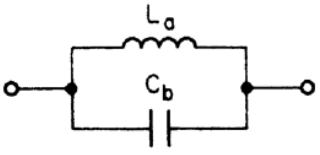
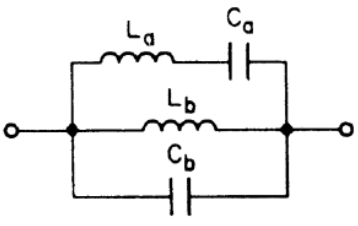
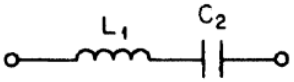
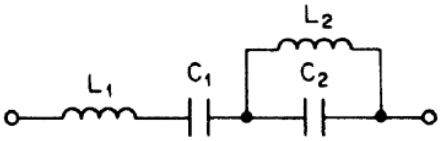


Source: The author

6. Equivalent bandpass filter

   A transformation of each component of the lowpass filter must be done to obtain a bandpass filter. A capacitor in parallel with an inductor must replace each capacitor, and an inductor in series with a capacitor must replace each inductor as shown in figure 5.5.

Figure 5.5: The low-pass to Bandpass transformation

	Low-Pass Branch	Bandpass Configuration	Circuit Values
Type I			$L=\frac{1}{\omega_0^2 C}$ $C=\frac{1}{\omega_0^2 L}$
Type II			$C_a=\frac{1}{\omega_0^2 L_a}$ $L_b=\frac{1}{\omega_0^2 C_b}$
Type III			$C_1=\frac{1}{\omega_0^2 L_1}$ $L_2=\frac{1}{\omega_0^2 C_2}$
Type IV			

Source: (TAYLOR, 2006)

The new components must be in resonance with the respective pair at central frequency f_0 , i.e.:

- C_1 and L_2 must be in resonance @ f_0

$$L_2 = \frac{1}{\omega^2 \cdot C_1} = \frac{1}{(2\pi \cdot 400.856M)^2 \cdot 63.66p} = 2.47nH \tag{5.11}$$

- C_3 and L_1 must be in resonance @ f_0

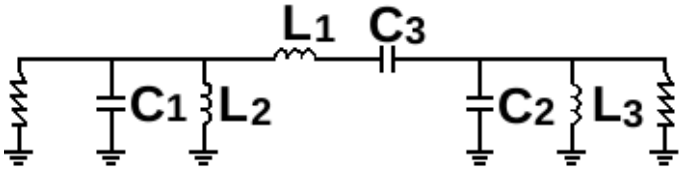
$$C_3 = \frac{1}{\omega^2 \cdot L_1} = \frac{1}{(2\pi \cdot 400.856M)^2 \cdot 318.31n} = 495.24fF \tag{5.12}$$

- C_2 and L_3 must be in resonance @ f_0

$$L_3 = \frac{1}{\omega^2 \cdot C_2} = \frac{1}{(2\pi \cdot 400.856M)^2 \cdot 63.66p} = 2.47nH \tag{5.13}$$

The final passband filter is shown in figure 5.6.

Figure 5.6: Butterworth bandpass filter



Source: The author

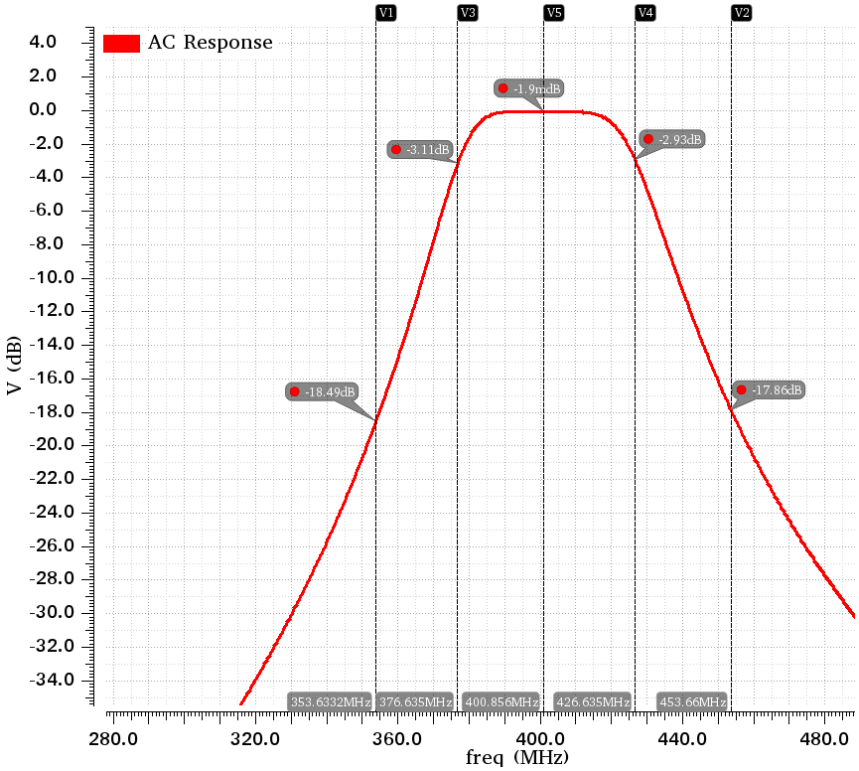
A two-port testbench was made to verify the design, and it was measured the frequency response of the filter. Figure 5.7 presents the result.

The designed filter achieves a voltage gain of approximately 0dB, a bandwidth approximately of 50 MHz, between 3dB frequencies of 376.635 MHz and 426.635 MHz, and provide the rejection near to -20 dB on both lower and higher frequencies (354.2 MHz and 453.66 MHz).

Although in theory, the filter would solve the problem it is hard to make a complete integration with the other circuits due to the high value of one inductor. For this reason, it was decided to use an external filter in the project (BPF−A410+, 2018) and a Verilog-A™ code was implemented to model the frequency response of the filter.

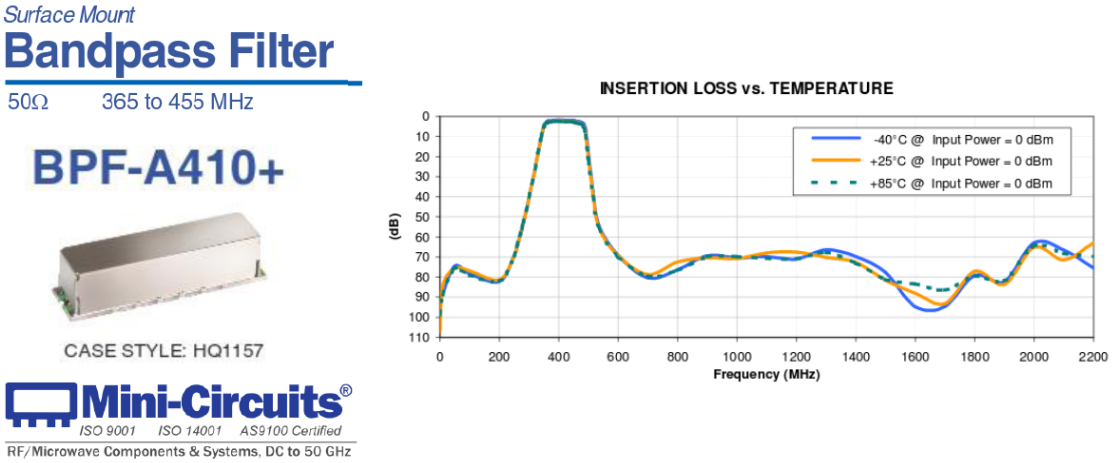
For this project it was used the bandpass filter BPF-A410 provided by Mini-Circuits® that presents a similar frequency response at the desired frequency (figure 5.8. The filter datasheet also offers an S-parameter archive that can be instantiated in a component to obtain a more precise simulation.

Figure 5.7: Filter result



Source: The author

Figure 5.8: Commercial filter



Source: (BPF−A410+, 2018)

6 MIXER

6.1 Introduction

The third block of the receiver is the mixer, which has a function to translate the signal from an RF frequency to an intermediary baseband frequency, providing an amount of gain and noise as well.

The mixer works as a multiplier of RF signal and a reference local oscillator signal, considering time domain (equation 6.3). Similarly, it makes a convolution of RF and LO signals, considering the frequency domain.

So, supposing an input RF signal and LO signal as follows:

$$v_{RF} = A(t)cos(\omega_o t + \Phi(t)) \quad (6.1)$$

$$v_{LO} = A_{LO}cos(\omega_{LO} t) \quad (6.2)$$

$$v_{OUT} = v_{RF} \cdot v_{LO} \quad (6.3)$$

$$v_{OUT} = (\frac{A(t) \cdot A_{LO}}{2}) \cdot [cos\Phi(cos(\omega_{LO} + +\omega_o)t + cos(\omega_{LO} - \omega_o)t) - \quad (6.4)$$
$$-sin\Phi(sin(\omega_{LO} + \omega_o)t + sin(\omega_{LO} - \omega_o)t)]$$

$$v_{OUT} = (\frac{A(t) \cdot A_{LO}}{2}) \cdot [\underbrace{(cos((\omega_{LO} + \omega_o)t + \phi(t))}_{uppersideband} + \underbrace{(cos(\omega_{LO} - \omega_o)t + \phi(t)))}_{lowersideband}] \quad (6.5)$$

Equation 6.5 shows the frequency displacement that is a characteristic of mixer circuits. Only one side of the band is of interest, in this case, the lower frequency $\omega_{LO} - \omega_o$.

In this project, it is necessary to make a downconversion from 401.635 MHz to 23.715 MHz with a local oscillator frequency of 377.92MHz. With this value, a single oscillator generates all frequencies necessary in the transceiver (TUDE et al., 1986). The following figures of merit are usually simulated and measured to characterize a mixer.

- Power consumption
- RF to IF Conversion Gain
- Noise and NF
- Input and output impedance matching
- LO to RF and LO to IF isolation
- Linearity

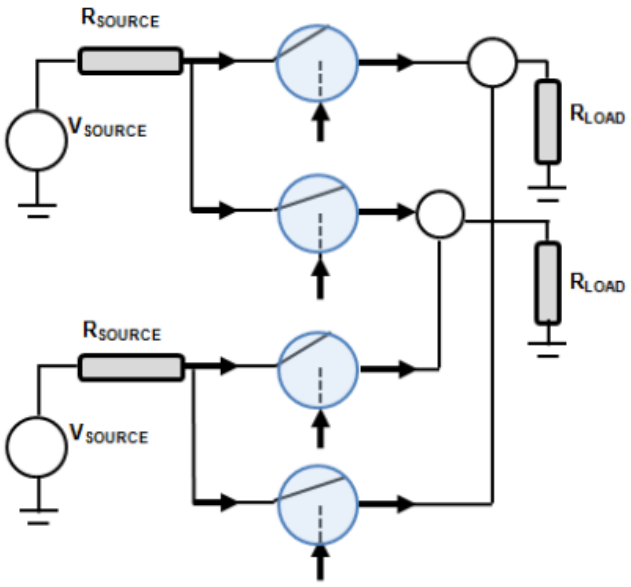
6.2 Mixer topologies

It is possible to classify mixers between two types: active and passive mixers.

Passive mixers are usually more linear than the active mixers, but they have higher noise figure, and they have negative gain (loss), and good linearity since the output signal is a current and voltage swing does not limit the linearity of the mixer. However, a passive mixer needs a large LO drive when compared to the active Gilbert cell mixer (VOLTTI; KOIVISTO; TIILIHARJU, 2007). Also, it requires an operational amplifier, extra power consumption and introduces additional noise.

Active mixers are not much linear, but they provide high gain and a moderate noise figure as well (TERROVITIS; MEYER, 1999). The main types of active mixer topologies are single and double balanced cells. Both topologies use three stages to compose the mixer: a transconductor, a switching pair, and a load.

Figure 6.1: Mixer representation

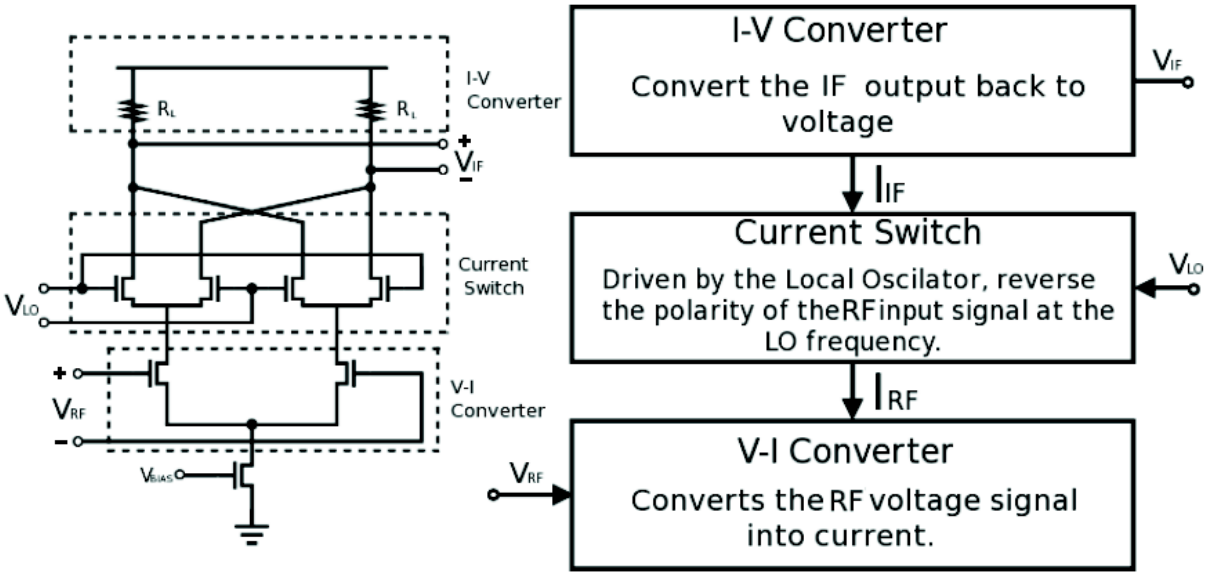


A single balanced mixer provides a strong LO feedthrough component at the output. The feedthrough is present because of DC offset on the RF input which produces a differential LO voltage component at the output. The LO component is highly undesirable because it could desensitize an amplifier stage after mixer and an eventual mismatch in the circuit may generate it.

Double balanced Gilbert cell mixers, consist of a differential RF input stage, two switching pairs and a load for each pair as illustrated in figure 6.2. This topology presents better LO to IF port isolation when compared to single balanced. It also rejects even order

distortion due to its differential operation.

Figure 6.2: Double balanced mixer



Source: (RAZAVI, 2011) - (adapted)

The mixer might comply with a set of specifications according to system level simulations to guarantee that the receiver will provide gain and noise figure that are necessary to the Analog-to-digital converter. Table 6.1 summarizes the goals of this project.

Table 6.1: Mixer specifications

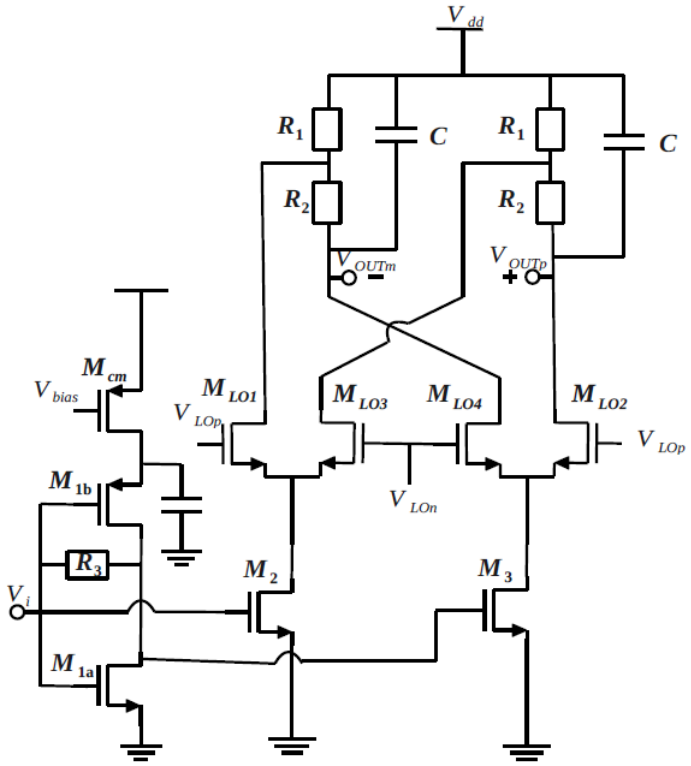
Specification	*Limits*	*Unit*
Input Frequency	401.635	MHz
Output Frequency	23.715	MHz
Input impedance	50	Ω
IIP3	> -15	dBm
Noise Figure	≤ 10	dB
Gain	≥ 15	dB

6.3 Schematic project

The mixer is similar to a Gilbert Cell topology that has a single-to-differential stage to connect the output of the external filter, which is single-ended to the differential input of the mixer. Figure 6.3 shows the schematic of the mixer.

Transistors M_{1a} and M_{1b} compose the single-to-differential converter, transistors M_2 and M_3 are the RF transconductors, and the M_{LOx} represents the LO switches. Resistors (R_1 and R_2) and capacitors represent the load stage.

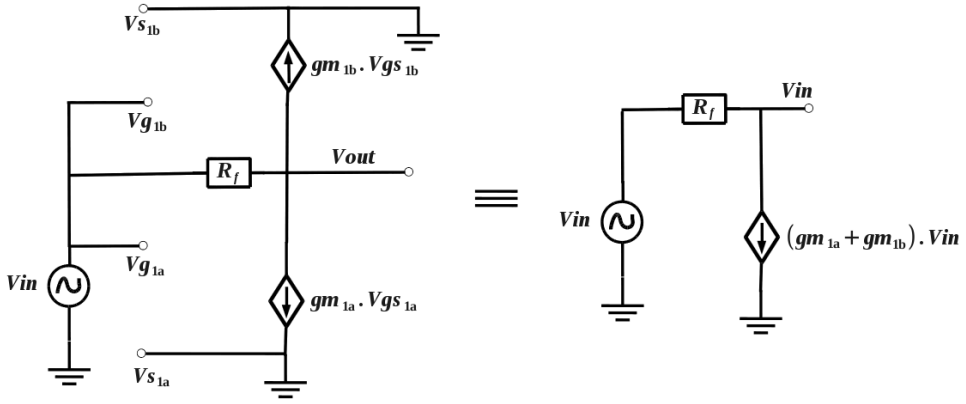
Figure 6.3: Schematic of mixer



Source: The author

A resistor feedback inverter composes the single-to-differential stage. The voltage that appears on both resistor terminals are equal and with a $180°$ phase deviation, so connecting each terminal at the gates of RF transconductors it will generate the current for the positive and negative input terminals of the mixer. Applying the small signal model in the circuit, it reduces to a simplified model that approximates to figure 6.4.

Figure 6.4: Simplified small signal model for single-to-differential stage



Source: The author

Making the impedance matching with the output filter impedance (50 Ω), we have:

$$Z_{in} = \frac{1}{gm_{1a} + gm_{1b}} \tag{6.6}$$

$$50\Omega = \frac{1}{gm_{1a} + gm_{1b}} \tag{6.7}$$

$$gm_{1a} + gm_{1b} = 20mS \tag{6.8}$$

Transistor M_{CM} adjusts the DC level of PMOS transistor M_{1b}. It was necessary to have a DC voltage of approximately 600mV in the resistor terminals, so the source of M_{1b} has 1.1V that comes from V_{CM} with a V_{bias} of 600 mV. A total current of 1.4 mA defines the width of each transistor using the quadratic model shown in equations 6.9 and 6.10.

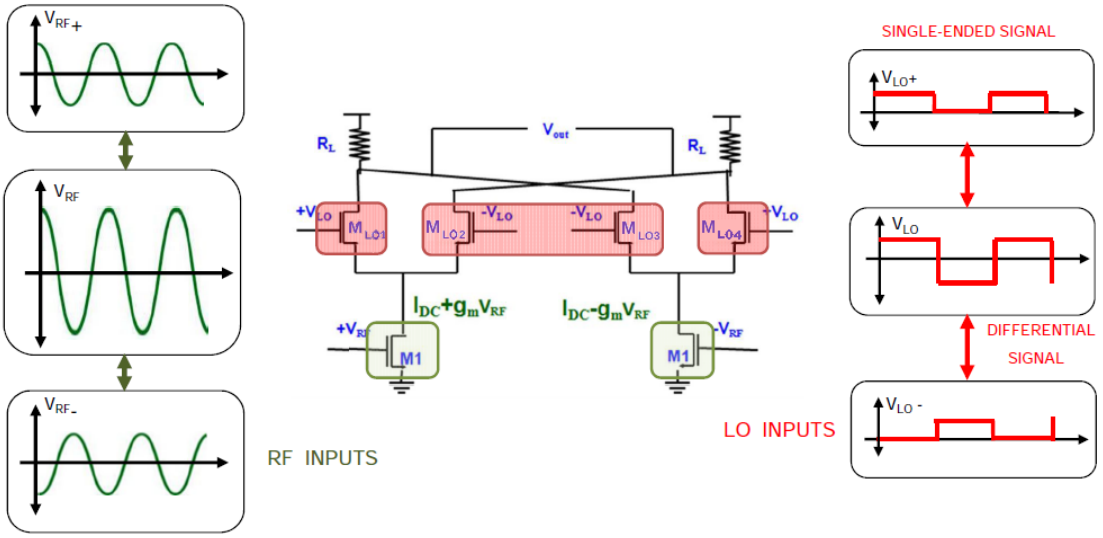
$$\begin{aligned} I_d &= \frac{1}{2} \cdot \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \\ 1.4m &= \frac{1}{2} \cdot 384\mu \cdot \frac{W}{240n} \cdot (594.2m - 301.3m)^2 \\ W_{M1a} &= 20.4\mu m \end{aligned} \tag{6.9}$$

$$\begin{aligned} I_d &= \frac{1}{2} \cdot \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \\ 1.4m &= \frac{1}{2} \cdot 330\mu \cdot \frac{W}{240n} \cdot (594.2m - 301.3m)^2 \\ W_{M1b} &= 23\mu m \end{aligned} \tag{6.10}$$

To calculate the conversion gain, we will follow a strategy used in a typical double

balanced mixer. The RF and LO signals are equal with a phase deviation of 180 degrees (figure 6.5), so the differential signal will have a doubled amplitude.

Figure 6.5: Basic Gilbert Cell



Source: The author

Considering I_{LO1}, I_{LO2}, I_{LO3}, and I_{LO4} as the currents that pass through the LO transistors M_{LO1}, M_{LO2}, M_{LO3}, and M_{LO4}, respectively, the currents of each branch are defined by equations 6.11, 6.12, 6.13, and 6.14.

$$I_{LO1} = \frac{I_{RF1}}{2} - gm_1 \cdot \frac{V_{LO}}{2} \tag{6.11}$$

$$I_{LO2} = \frac{I_{RF1}}{2} + gm_2 \cdot \frac{V_{LO}}{2} \tag{6.12}$$

$$I_{LO3} = \frac{I_{RF2}}{2} - gm_3 \cdot \frac{V_{LO}}{2} \tag{6.13}$$

$$I_{LO4} = \frac{I_{RF2}}{2} + gm_4 \cdot \frac{V_{LO}}{2} \tag{6.14}$$

The current that passes through each load is the difference between two branches (eq. 6.15 and 6.16):

$$I_{OUT1} = I_{LO1} - I_{LO3} = (gm_3 - gm_1) \cdot \frac{V_{LO}}{2} \tag{6.15}$$

$$I_{OUT2} = I_{LO4} - I_{LO2} = (gm_4 - gm_2) \cdot \frac{V_{LO}}{2} \tag{6.16}$$

$$V_{OUT1} = I_{OUT1} \cdot R_{OUT} = \frac{V_{LO}}{Vd_{sat}}(gm_{RF}) \cdot V_{RF} \cdot R_{out} \tag{6.17}$$

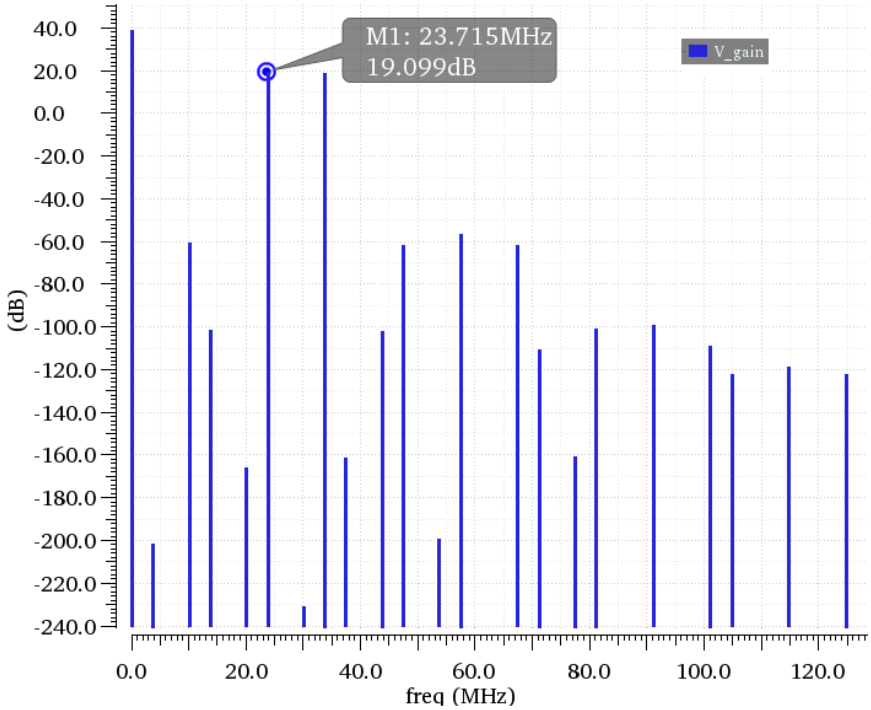
$$C_G = \frac{V_{OUT}}{V_{RF}} = \frac{V_{LO}}{Vd_{sat}} \cdot gm_{RF} \cdot R_{out} \tag{6.18}$$

To calculate the conversion gain it is necessary to obtain the output voltage (eq. 6.17) and divide by input RF voltage (eq. 6.18).

As the differential circuit depends only on the difference of two branches, this methodology can be extended to the proposed circuit if the circuit maintains equal the values of $I_{LO1} - ILO_3$ and $I_{LO4} - I_{LO2}$.In this project it is being used the following values: $V_{LO} = 600mV$, $Vd_{sat} = 65mV$, $gm_{RF} = 10mS$, and $R_{out} = 100\Omega$, which gives a total conversion gain of 19.3 dB.

Figure 6.6 shows the voltage gain result using a QPSS analysis.

Figure 6.6: Conversion Gain



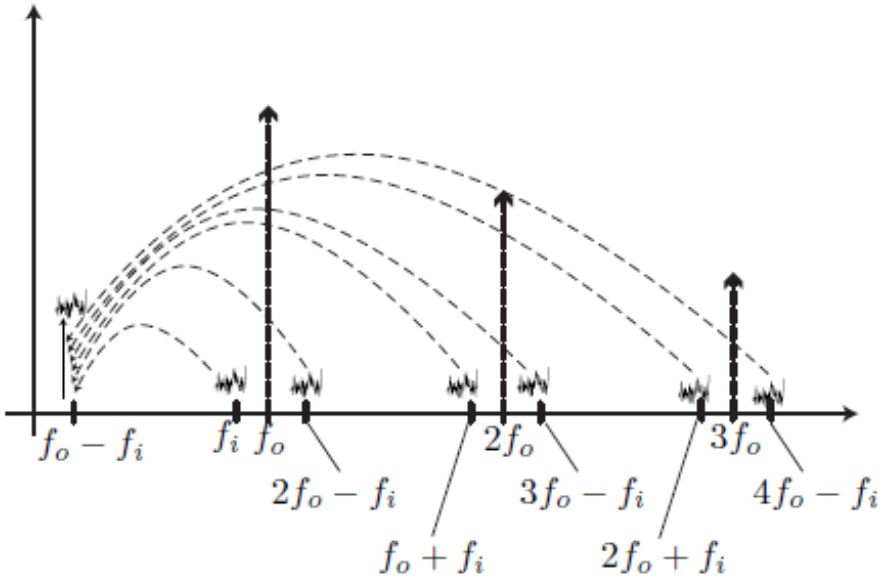
Source: The author

This mixer is inside a superheterodyne architecture that suffers from an image signal generation due to the mixing process. It is necessary to filter the image signal before the mixer. Otherwise, it will fold to the same intermediary frequency, and it will act as a frequency interferer, losing the signal. Beside this, noise sources that come from other harmonics that mixer generates will also corrupt the desired IF signal as shown in figure 6.7. These other images are easy to reject because they are distant from the desired signal and an image reject filter will be able to attenuate them significantly.

Downconverter mixers are inherently noisy circuits because the noise of both image and the desired band will combine in the desired channel at the IF frequency. Mixers are commonly affected by thermal and flicker noise.

Thermal agitation of electrons causes the thermal noise, and it is present on transistors and resistors in the circuit. For transistors, equation 6.19 models thermal noise,

Figure 6.7: Noise displacement



Source: (NIKNEJAD, 2016a)

where K is the Boltzmann constant, T is the temperature, γ is an empirical factor that depends on the technology and g_{do} is the channel resistance with V_{ds}=0. Ideally, g_{do} is equal to g_m, but effects such velocity saturation can cause a difference between these parameters (PERROTT, 2012).

$$\frac{\overline{v_{thermal}}^2}{\Delta f} = \frac{4 \cdot K \cdot T \cdot \gamma}{g_{do}} \tag{6.19}$$

Flicker noise is associated with surface charge trapping in semiconductors. It is presented in transistors and diodes, but not in resistors. A current source, with power spectral density that depends on the frequency of operation, models the Flicker noise (equation 6.20), where K_f is an empirical constant that depends on the manufacturing process.

$$S_i(f) = K_f \cdot \frac{I^a}{f^b} \tag{6.20}$$

Flicker noise is more significant in circuits that operate at lower frequencies, or in this case, mixers that translate the signal to lower frequencies. Equation 6.20 can be extended to a noise current over a frequency bandwidth (equation 6.21).

$$S_i(f) = K_f \cdot I^a \cdot ln(\frac{f_2}{f_1}) \tag{6.21}$$

In the MOSFET the surface recombination of flicker noise might modulate the

channel current and can be minimized by careful treatment during the manufacturing process. Equation 6.22 shows an electrical equivalent model for transistors.

$$\frac{\overline{v_n}^2}{\Delta f} = \frac{K_f}{C_{ox}WL} \cdot \frac{1}{f} \tag{6.22}$$

Therefore, the noise of a transistor is the superposition of thermal and flicker noises (equation 6.23)

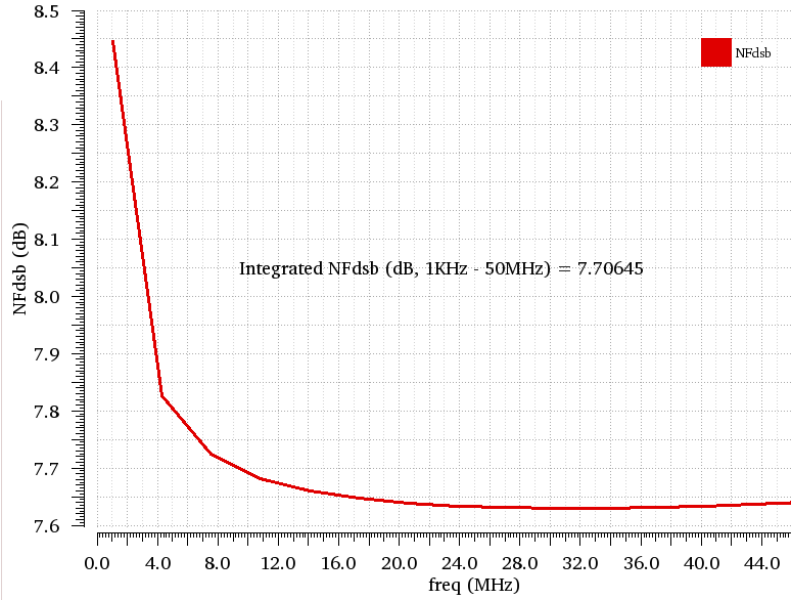
$$\frac{\overline{v_n}^2}{\Delta f} = \underbrace{\frac{8KT}{3g_m}}_{Channel} + \underbrace{\frac{4R_{gate}KT}{3}}_{R_{sat}} + \underbrace{\frac{K_f}{C_{ox}WL} \cdot \frac{1}{f}}_{Flicker} \tag{6.23}$$

The switching pairs (M_{LO}) contribute mostly for the flicker noise output of the Gilbert mixer (CHENG et al., 2011) while the transconductors contribute to thermal noise.

Equation 6.23 infers that higher transistor widths will reduce the total flicker noise, but it also contributes to thermal noise. Due to compromises between gain and noise figure, it was necessary to find an intermediary value that provides adequate value for the noise specification. In this project, each LO transistor has a total width of $72\mu m$ using minimum length. This value was obtained using a parametric analysis.

The total noise contribution is a superposition of thermal noise of resistors, transconductors and the flicker noise of LO transistors. Combining QPSS and QPNOISE simulations give information of DSB NF. The integrated double-sideband noise figure over a band varying from 1MHz to 25 MHz has a value of 7.7 dB (figure 6.8).

Figure 6.8: DSB Noise Figure

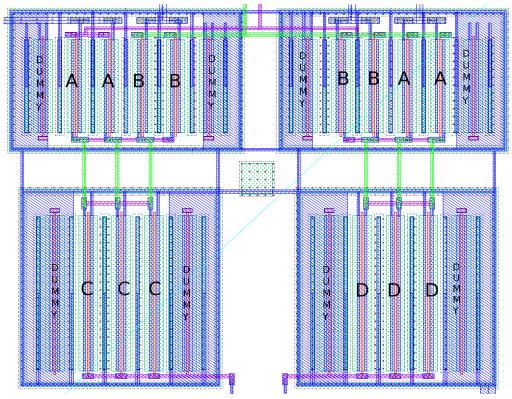


Source: The author

6.4 Layout

The Gilbert cell topology is by nature a symmetrical structure, so the layout of the mixer was designed as symmetrical as possible to guarantee that the simulation results of the schematic remain close to the results obtained from the layout parasitic.

Figure 6.9: Symmetric placement of LO switches(above) and transconductor(below)



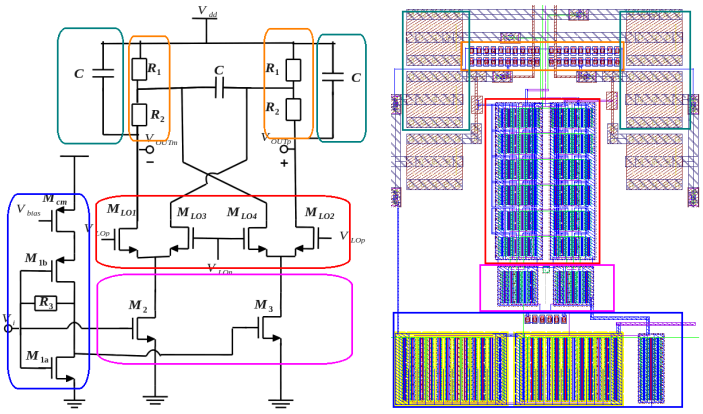
Source: The author

Figure 6.9 exemplifies the symmetry in the LO switches and the transconductor. In this case, not only the transistors were displaced symmetrically, but it was a concern to draw the LO nets to have approximately the same length to avoid any mismatch effect in the switches. The schematic provides a small difference in the switches.

The complete layout of the mixer follows the same strategies listed in chapter 4. Figure 6.10 (b) shows the complete layout and figure 6.10 (a) shows where each correspondent component of the layout in the schematic.

Figure 6.10: Final Mixer structure

(a) Mixer Schematic (b) Mixer layout



Source: The author

The complete layout occupies a total area of 130μm x 100 μm.

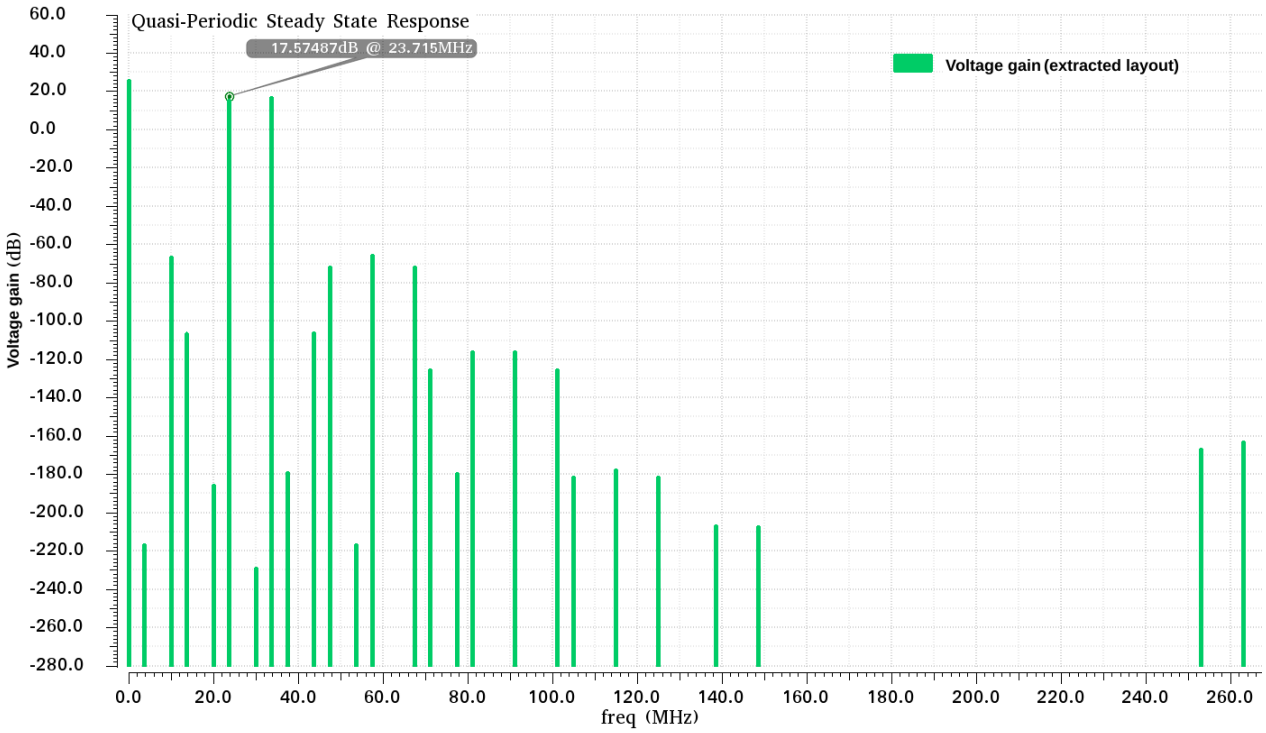
6.4.1 Post-layout results

A QPSS and QPnoise simulation with the inclusion of parasitic provides a more precise result of the circuit.

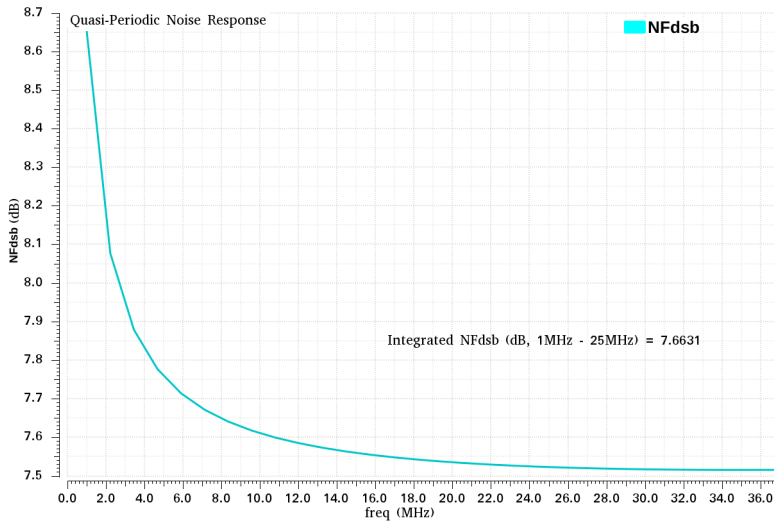
The graphs of figures 6.11 (a) and 6.11 (b) show the simulation results.

Figure 6.11: Mixer Post-layout results

(a) Conversion gain

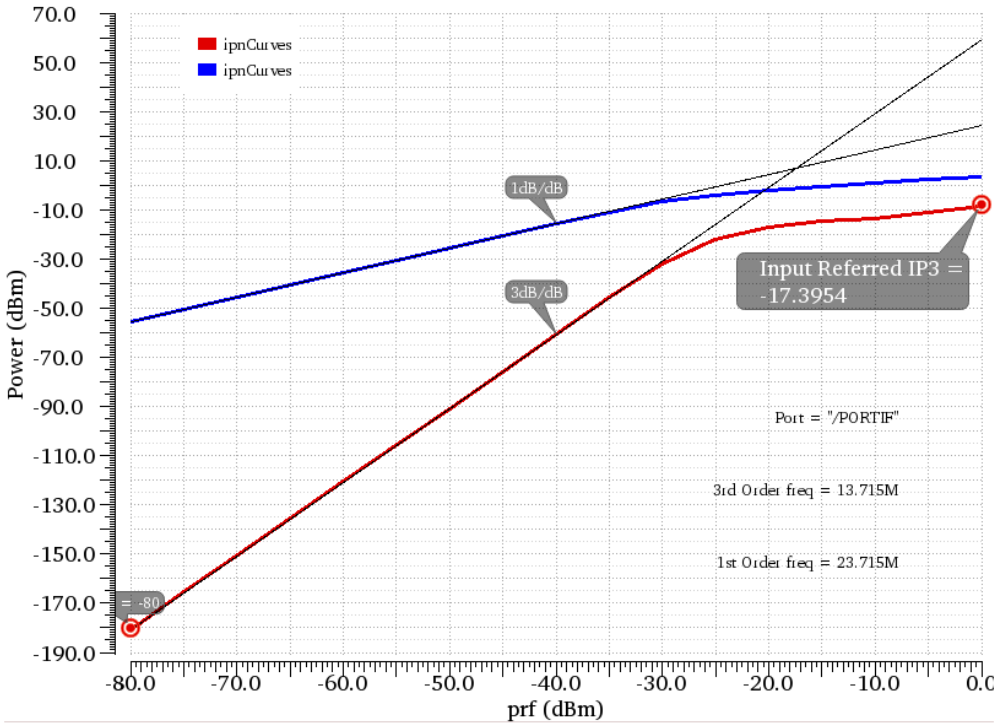


(b) DSB NF



Source: The author

Figure 6.12: Final mixer IIP3



Source: The author

6.5 Robustness Analysis

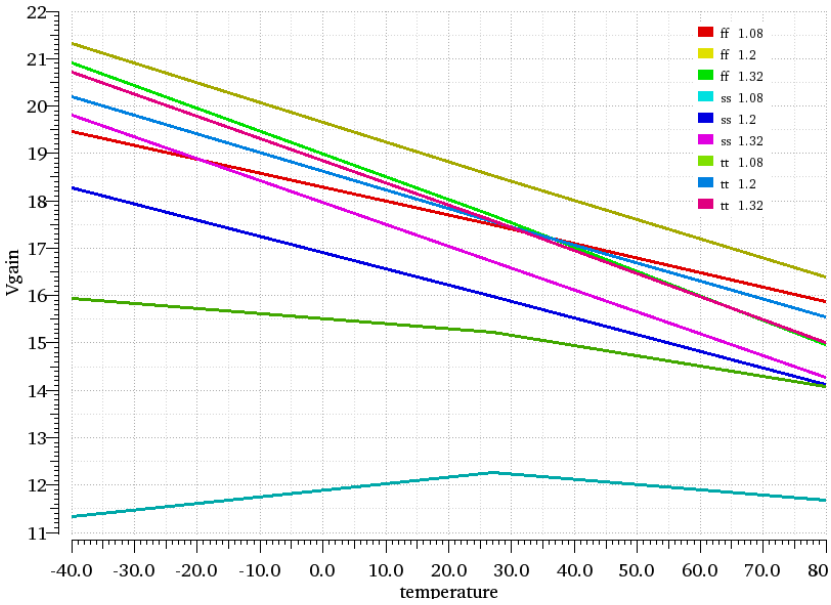
The simulation of the worst case scenario of operation is done performing a robustness analysis under PVT variations in the mixer. Using the same temperature range of previous circuits (-40°C to 80°C), a variation of 10% of VDD and the transistor operating at slow and fast modes we get the following results:

The gain corner decreases with the increase of temperature 6.13 (a). The total gain varies about 5 dB for each corner. The lowest gain corner occurs when the transistors are operating at slow mode. If the transistor is not on slow mode, higher temperatures are dominant to reduce the total gain.

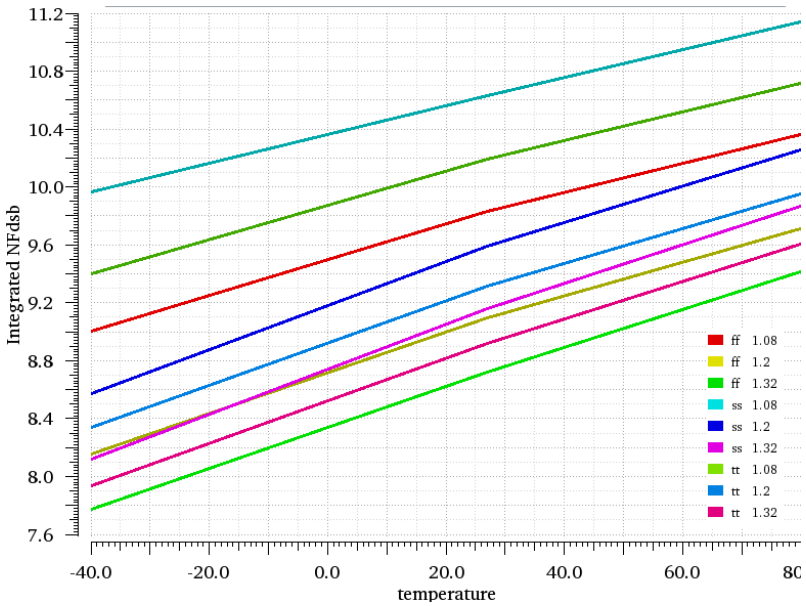
The noise figure corners follow the thermal noise behavior. That means they will increase almost linearly with the increase of the temperature. Figure 6.13 (b) shows the behavior of each corner. The noise figure value varies approximately 1.5 dB in the whole range of temperature for any specific corner. This range is not significant to compromise the receiver, due to the high gain of the LNA in the first stage of the receiver. For the worst NF corner value of 11.2 dB and considering the worst LNA gain corner the total noise figure of the maintains close to the LNA noise figure according to Friis equation.

Figure 6.13: Mixer corners results

(a) Conversion gain corner



(b) Noise figure corner



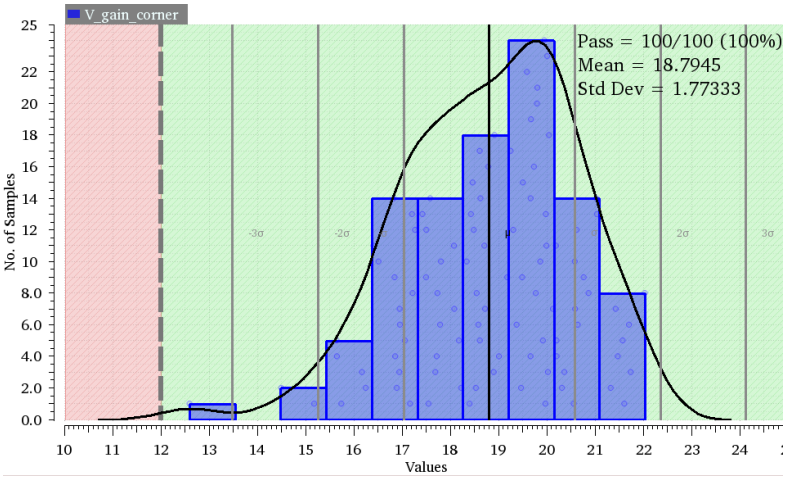
Source: The author

6.5.1 Monte carlo

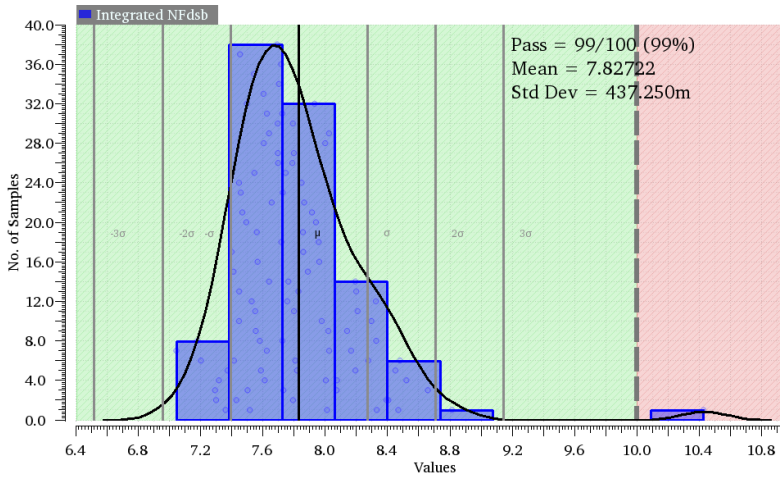
For statistical results, a Monte Carlo simulation with mismatch and process contributions was performed with a total of 100 samples. The results tends to a Gaussian distribution and are shown on figures 6.14 (a), 6.14 (b), and 6.14 (c). The red area limits the specifications that the mixer must attend.

Figure 6.14: Mixer Monte Carlo results

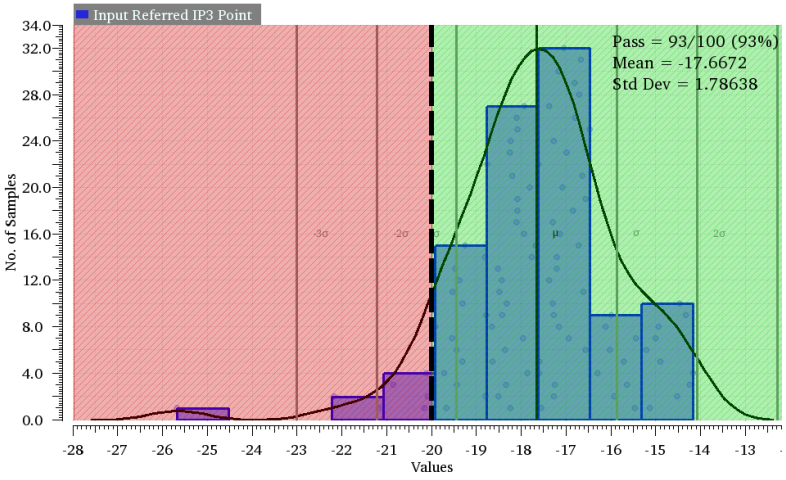
(a) Conversion Gain Histogram - Specification: CG > 12 dB



(b) Noise Figure Histogram - Specification: NF < 10 dB



(c) IIP3 Histogram - Specification: IIP3 > -20 dBm



Source: The author

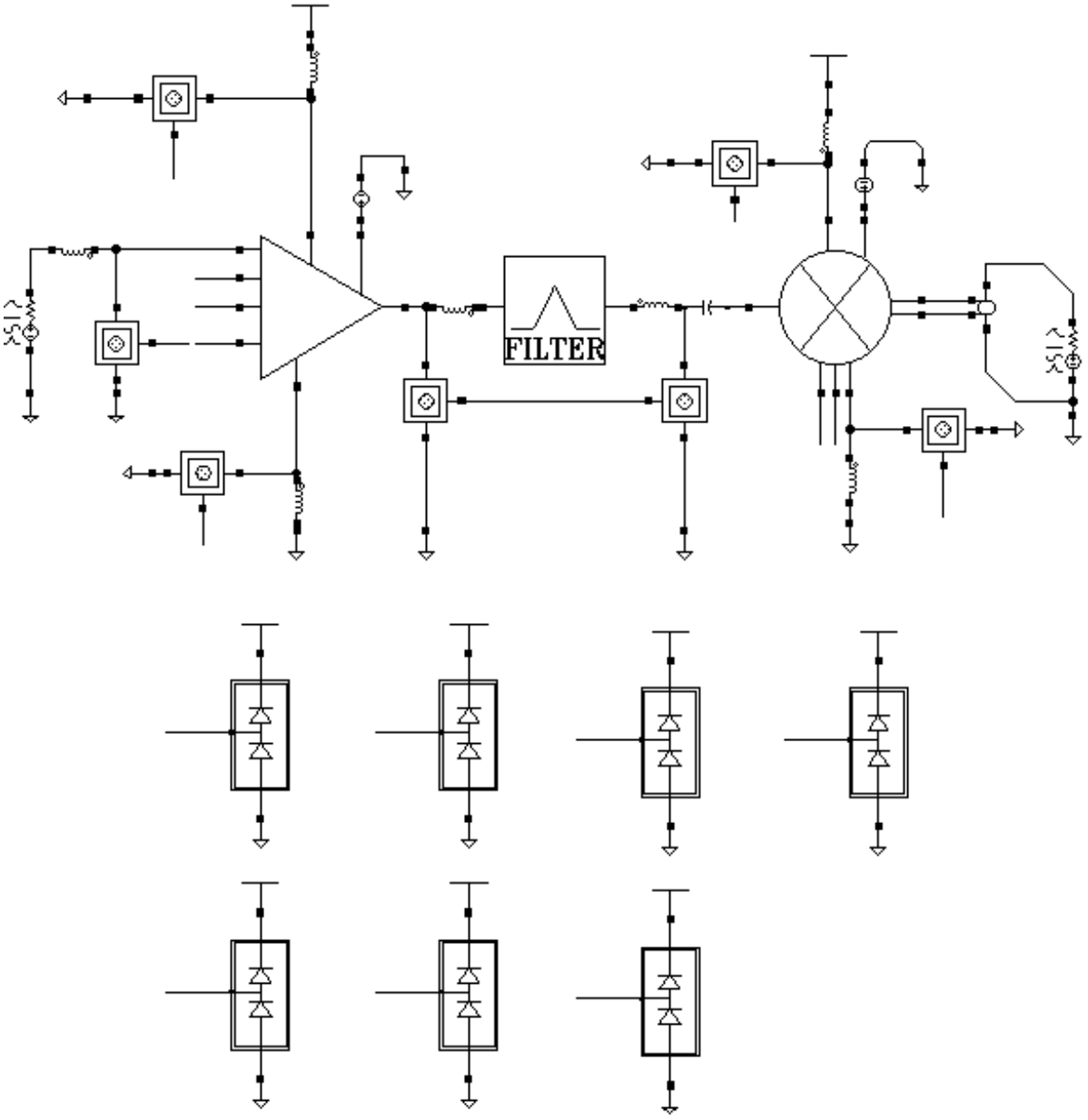
The conversion gain specification remains close to the nominal value with a mean value of 18.79 dB with a standard deviation of 1.77dB for 100 samples. The same occurs with the IIP3 specification that presented a mean value of -17.67 dBm with 1.78 dBm of standard deviation.

Only one sample of Gain and NF histograms differs from the majority. The circuit might run out of operation in this specific scenario, and it would be necessary to include in the circuitry a calibration structure that compensates this specific situation.

7 TOP-LEVEL SIMULATIONS

After the design of the first three blocks, it was created a testbench that includes the blocks and some pads and simple bondwires models in order to simulate the behavior of each specification due to the cascade effect of the blocks and also with the inclusion of parasitic that comes from pads, bondwires, and ESD protection that might corrupt the signal.

Figure 7.1: Schematic of RF front end testbench with pads, bondwires and ESD protection

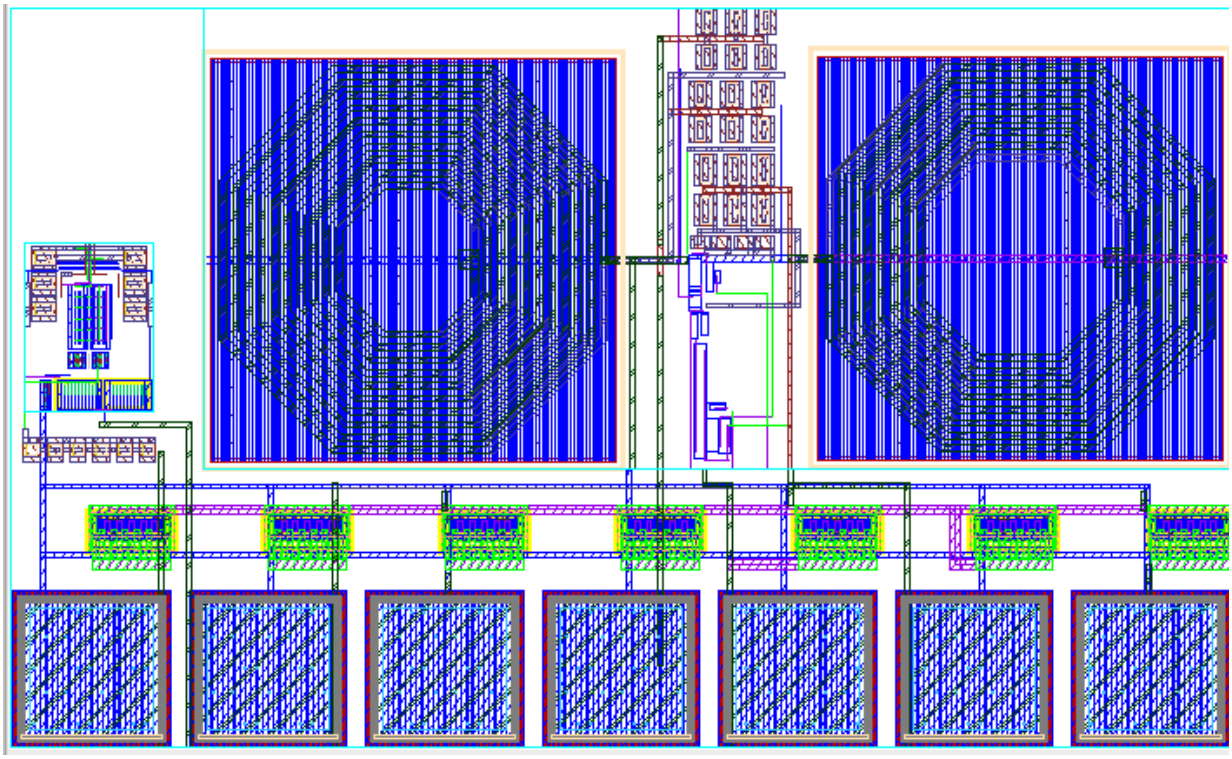


Source: The author

Figure 7.2 presents the layout of the final structure including the pads, and the

ESD structure occupying a total area of $573.1\mu m$ X $948\mu m$.

Figure 7.2: Final layout with pads and ESD protection



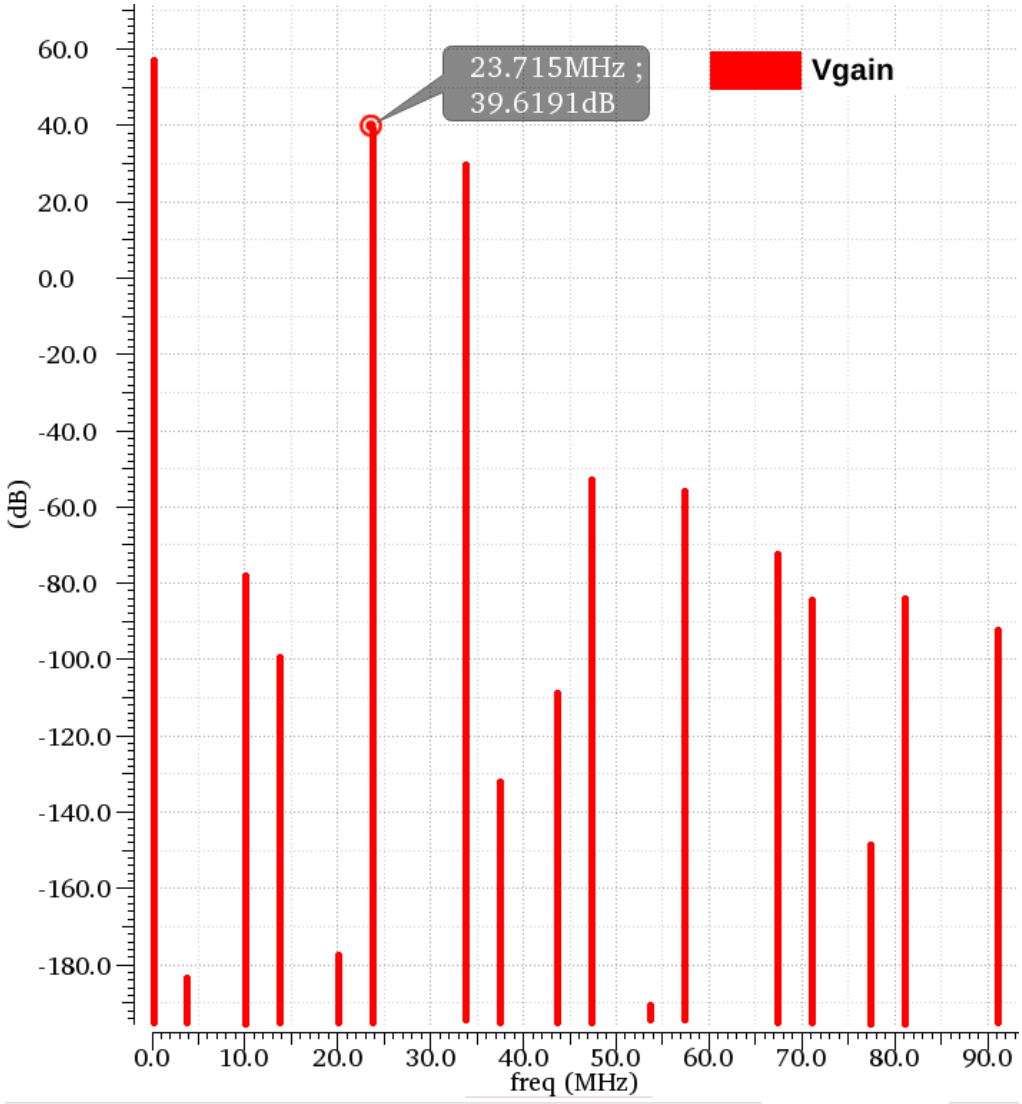
Source: The author

7.1 Nominal simulation

It is possible to simulate the total gain and the integrated noise figure with a combination of QPSS and QPNoise simulations. The layout parasitics of the LNA, mixer, and the pads were included in this simulation. The filter remains in a Verilog-A model and the bondwire model remains with ideal components.

The initial estimation of the gain was about 35 dB for the RF front-end. A total of 39dB of gain was obtained (figure 7.3). This result will simplify the project of the baseband amplifier since it requires a lesser amount of gain.

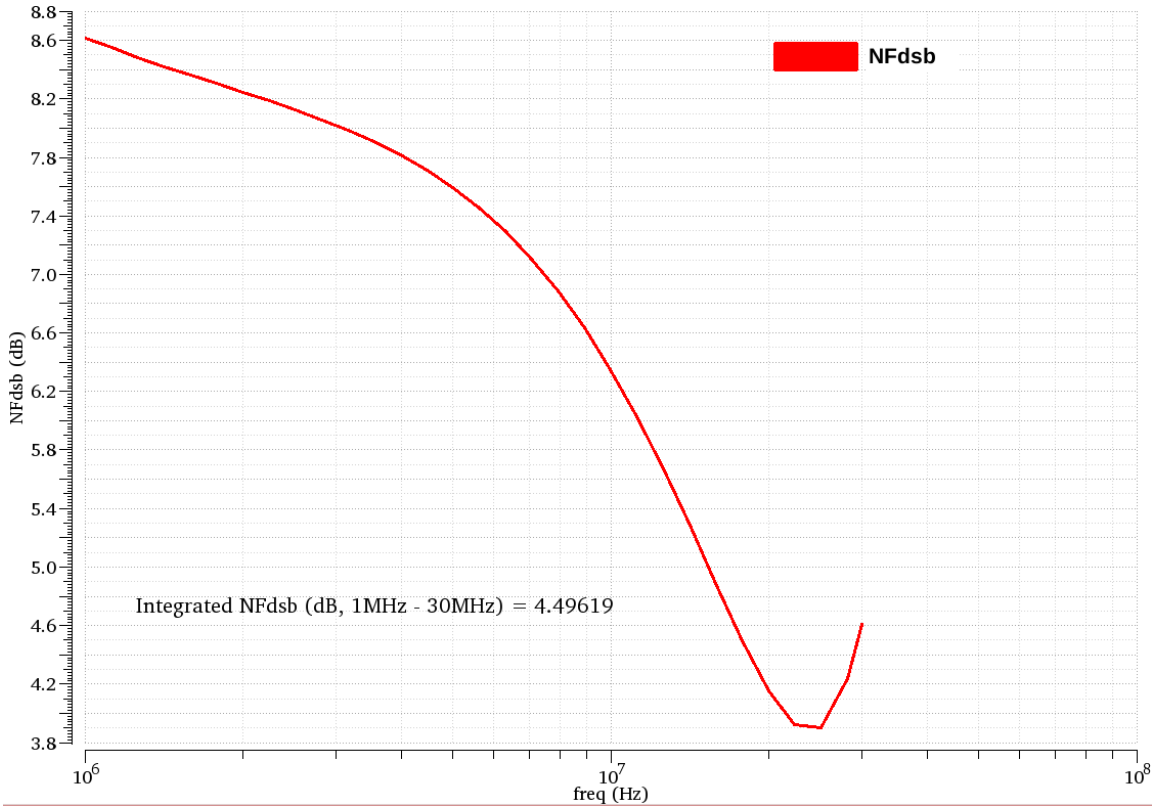
Figure 7.3: Receiver voltage gain



Source: The author

The noise figure specification is 3dB lower than the initial specification (figure 7.4), so the project will not have problems regarding noise.

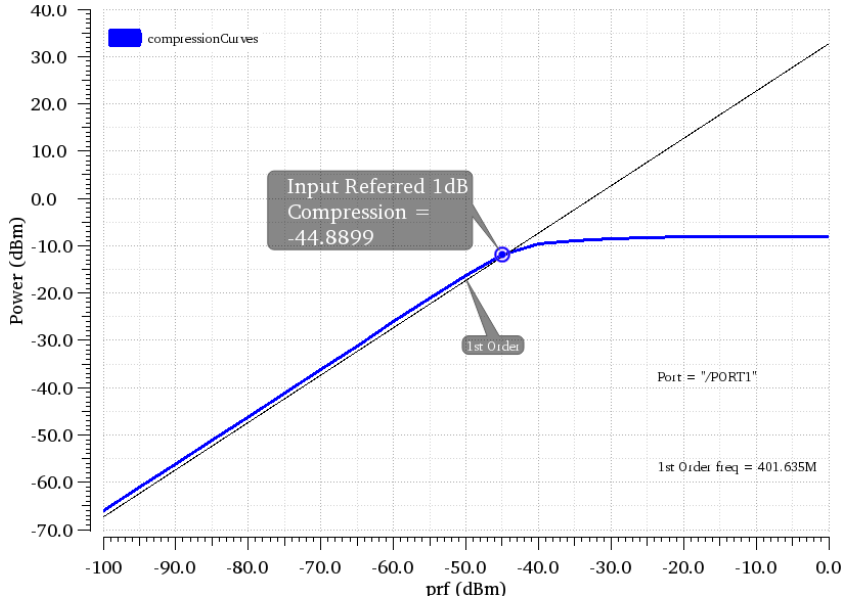
Figure 7.4: Receiver noise figure



Source: The author

A two-tone test with a QPSS simulation is necessary to measure the linearity of the receiver. The final nominal results of linearity are shown in figures 7.5 and 7.6.

Figure 7.5: Receiver 1dBCP

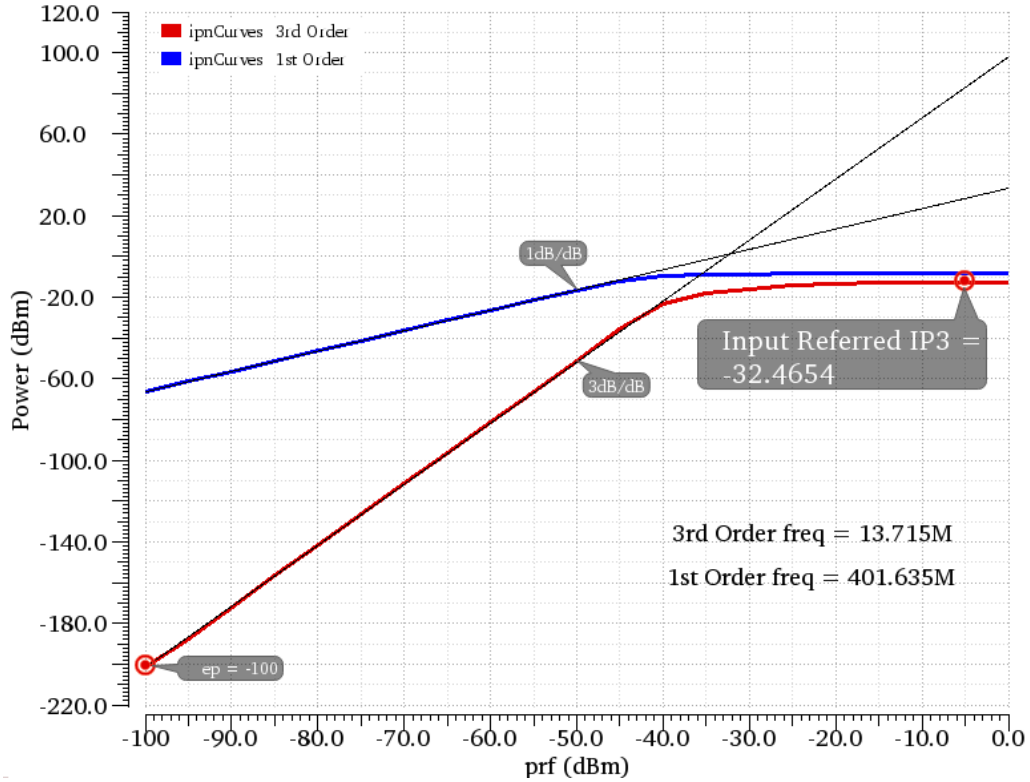


Source: The author

The IIP3 performance attends roughly the initial specification of -35 dBm, al-

though the communication protocol permits a lower IIP3 value. The 1dBCP remains close to the ideal value that differs approximately 10dB from the IIP3.

Figure 7.6: Receiver IIP3



Source: The author

7.2 Corner simulation

Table 7.1 presents the corner simulation of the post-layout circuit. The table presents the worst obtained values for each specification, considering the process, supply voltage, and temperature variations.

Table 7.1: Top-level corner results

Block	corner (temp,VDD)	NF	Gain	IIP3
RF Front-End	Nominal	4.63	39.6	-32.46
	-40° , 1.08 V	3.83	38.05	-29.32
	27° , 1.08 V	4.256	43.68	-33.32
	80° , 1.08 V	4.81	38.6	-31.79

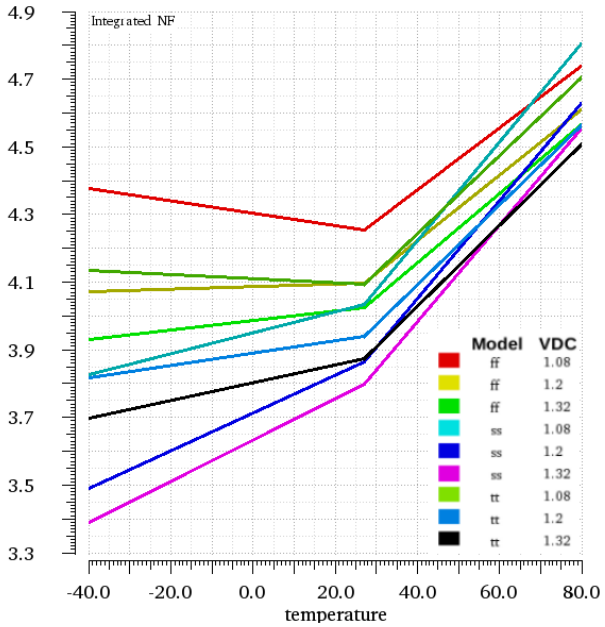
The worst NF value had the value of 4.81 dB and occurred at higher temperatures with transistors operating at slow modes with low Vdd. This NF value is more than 2 dB lesser than the initial specification of 7dB. The worst gain corner had the value of 38dB (3dB higher than the initial specification) and occurred in the same conditions as the NF corner. With this result of gain, the project of the baseband amplifier can be simplified to provide the necessary amplitude of the signal that goes to the ADC. The worst linearity corner remains close to the specification of -35 dBm with lower temperatures, and it will not compromise the final result.

Figure 7.7 shows the behavior of NF specification with PVT variations. The graph shows that the NF has a PTAT characteristic. Current sources with CTAT behavior were included in the simulations with the objective to reduce the total noise figure at higher temperatures to make the noise figure curves flatter. There was a small reduction of total noise figure at higher temperatures using this strategy.

The voltage gain corner has a maximum variation of 10 dB depending on the corner (figure 7.8). This variation can jeopardize the ADC at the end of the receiver. One possibility to solve this problem is to include in the architecture a calibration structure that can compensate a specific corner or minimize the spread of gain in the circuit obtaining a better voltage level for the AD converter.

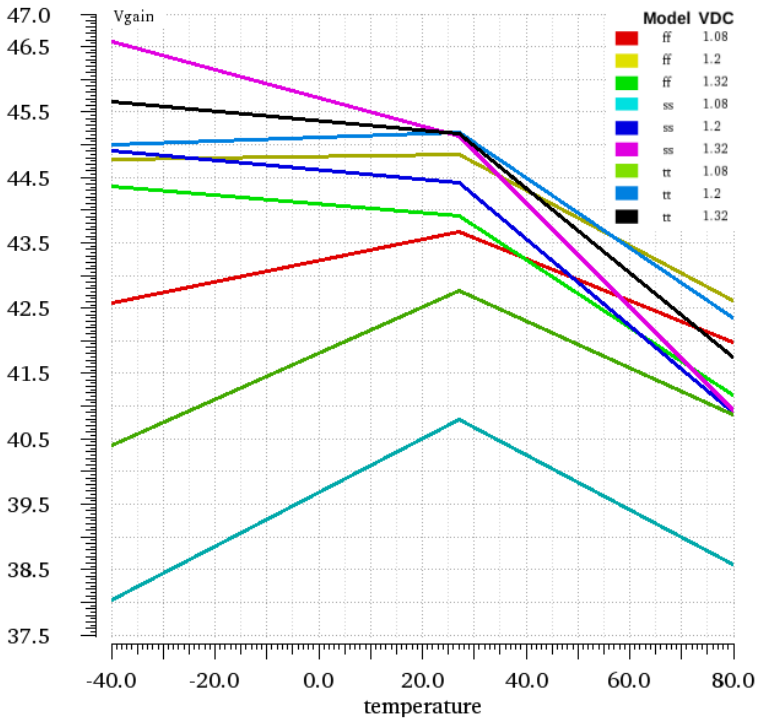
The IIP3 corner variations do not seem to be a problem since the specification requires that the IIP3 have to be higher than -35 dBm which occurs on all curves in the graph of figure 7.9. Only the typical corner tends to fail if the temperature drops below -40° C, but the worst interferer, that appears with -45 dBm of power at the frequency of

Figure 7.7: NF corner behavior



Source: The author

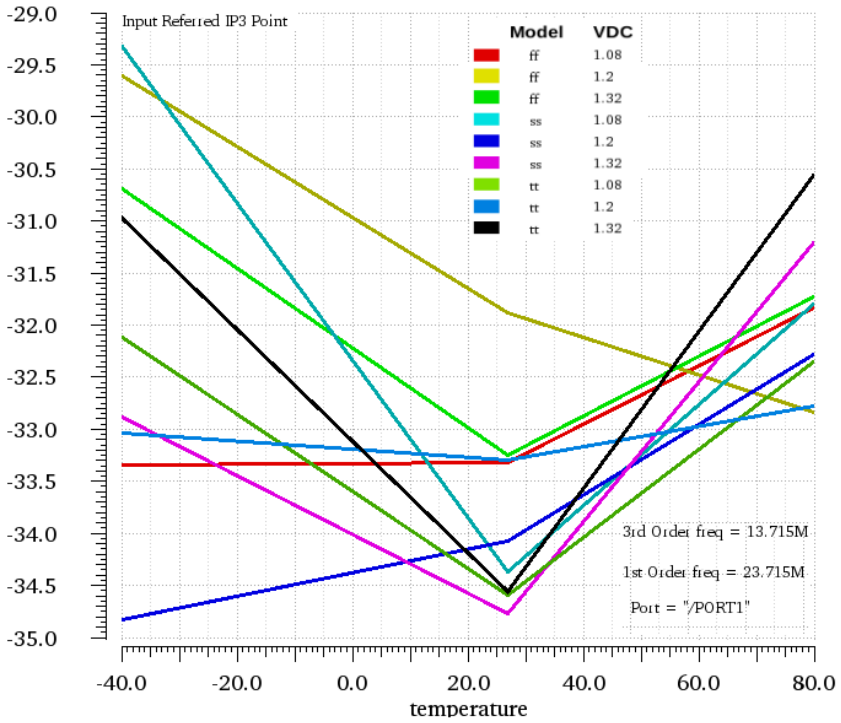
Figure 7.8: Voltage gain corner behavior



Source: The author

462.5 MHz, still will not have a significant influence on receiver performance.

Figure 7.9: IIP3 corner behavior



Source: The author

7.3 Monte Carlo simulation

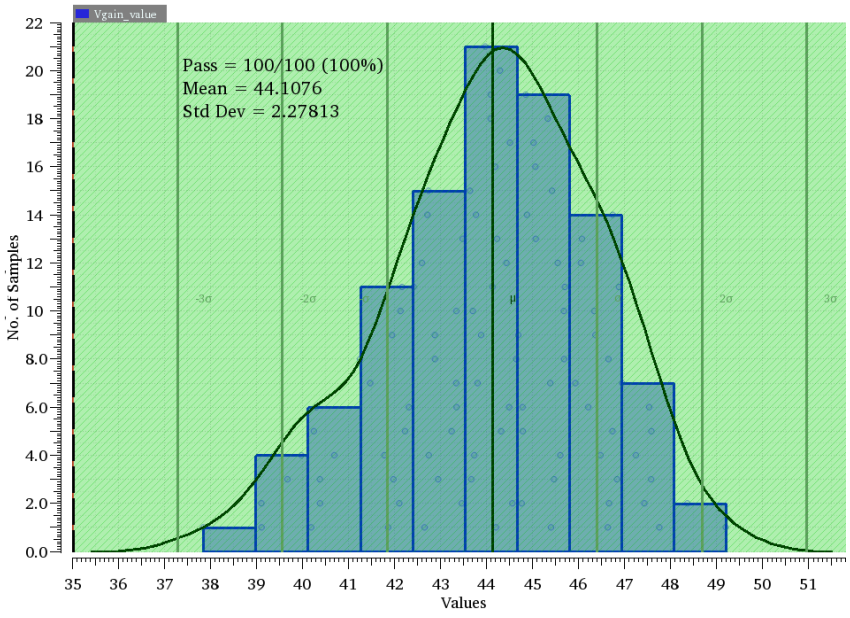
A Monte Carlo simulation was performed using mismatch and process variations with a total of 100 samples with all three blocks. The histograms are shown in figures 7.10,7.11, 7.12 and table 7.2 summarize the simulation results.

Table 7.2: Top-Level MonteCarlo results

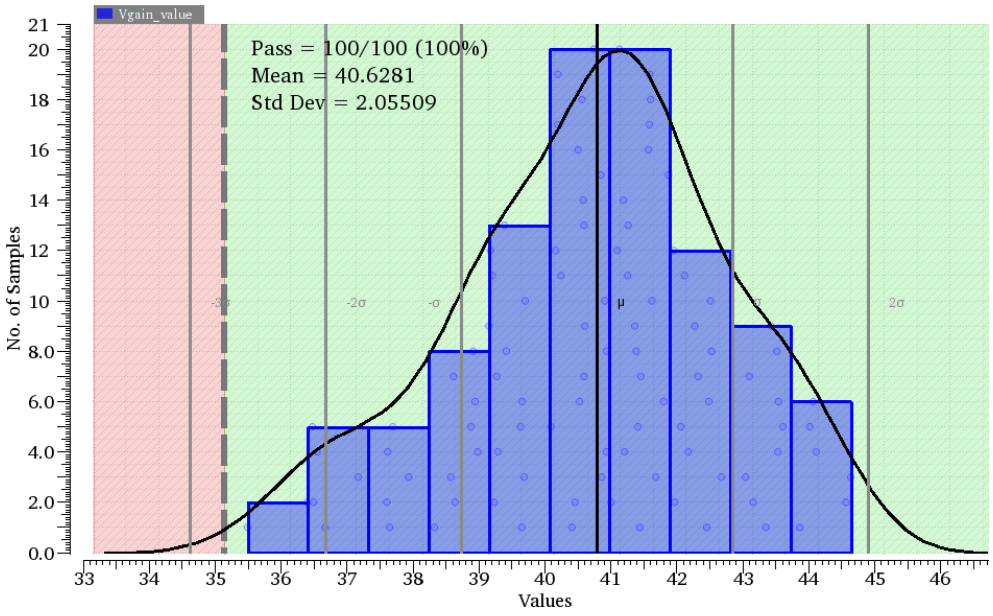
Block	Target	# Samples	Yield	Mean	Std Dev	Median
RF front-end	NF $\leq$ 7 dB	100	100%	5.415	479.6m	5.36
	Gain >35 dB	100	100%	40.63	2.055	40.83
	IIP3 >-35 dBm	100	100%	-30.34	1.342	-30.39

Figure 7.10: Top-level gain MonteCarlo analysis

(a) Schematic S_{21} Monte Carlo - Specification : S_{21} > 35 dB



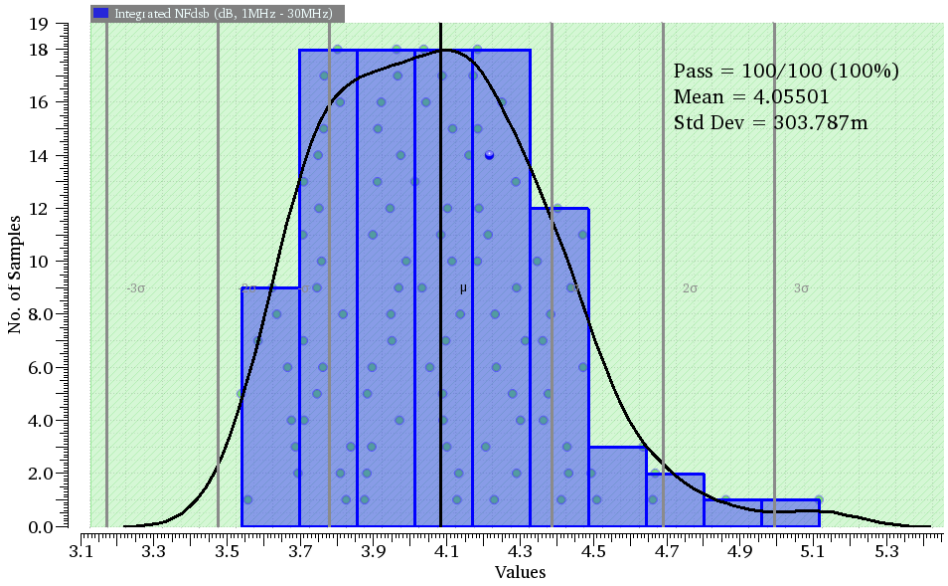
(b) Post-Layout S_{21} Monte Carlo - Specification : S_{21} > 35 dB



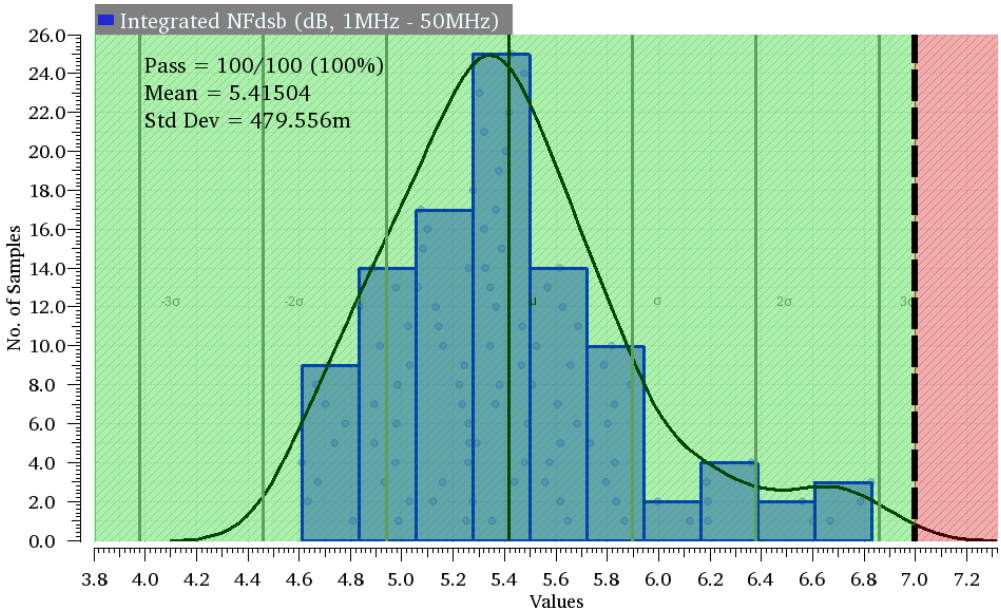
Source: The author

Figure 7.11: Top-level NF MonteCarlo analysis

(a) Schematic NF Monte Carlo - Specification: NF < 7dB



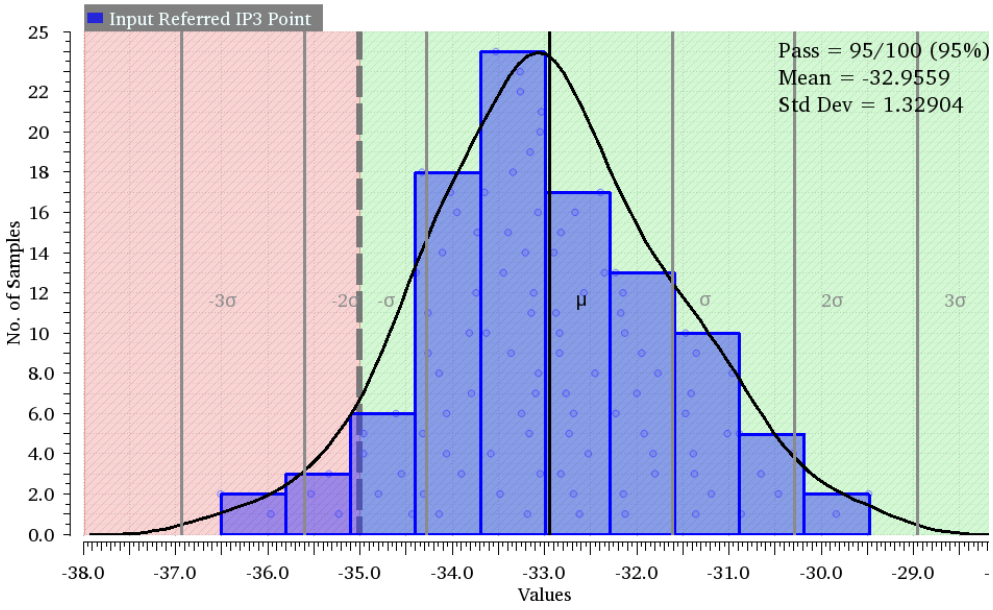
(b) Post-Layout NF Monte Carlo - Specification: NF < 7dB



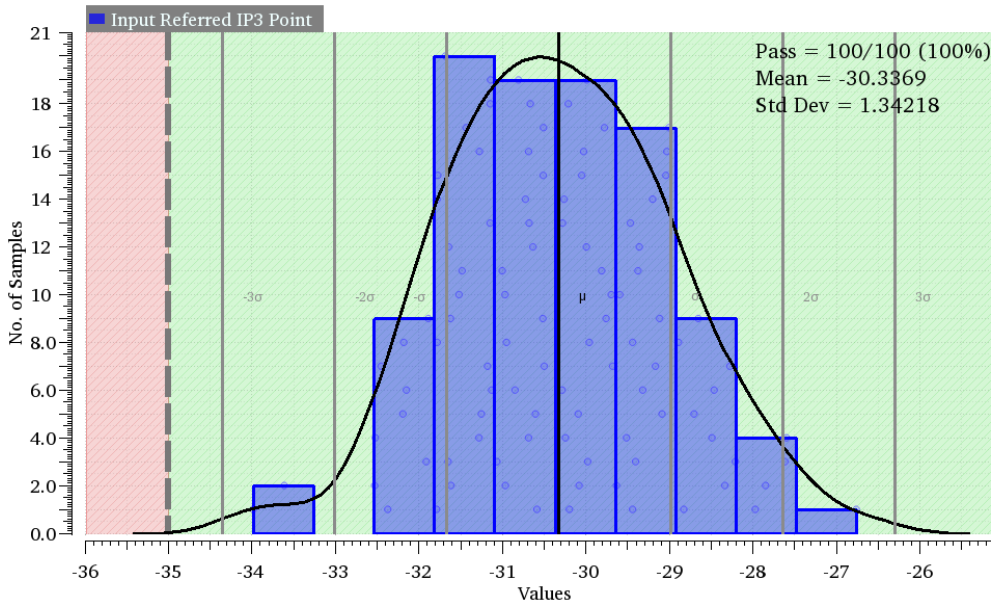
Source: The author

Figure 7.12: Top-level IIP_3 MonteCarlo analysis

(a) Schematic IIP_3 Monte Carlo - Specification : IIP_3 > -35 dBm



(b) Post-Layout IIP_3 Monte Carlo - Specification : IIP_3 > -35 dBm



Source: The author

7.4 Receivers comparison

This project is a specific demand of the industry, so it was not possible to find a large amount of published receivers that could operate in the same conditions this project requires.

Among all receivers, this project obtained the best results on power consumption and occupied area.

The proposed receiver presents larger NF when comparing with (JUNIOR et al., 2016), but with better power consumption, area and IIP3. This difference in the NF comes from the strategies adopted in the project. The conjugate noise matching technique can provide a low value for NF paying the price of linearity and gain. (JUNIOR et al., 2016) uses four LNA stages to reduce the total NF and increase the gain by loosing total area, linearity and power consumption.

Comparing with (KULKARNI et al., 2012), it provides better NF, Area and power consumption but with lower gain and IIP3. The results of (KULKARNI et al., 2012) receiver serve to evidence the trade-off between specifications for a particular application. In this case, to obtain high gain and linearity, power consumption and NF were lost.

The circuit offers similar performance when compared with (ZENCIR N. S. DOGAN, 2002), and occupies a significant smaller area and power consumption. All the results in this work came from parasitic analysis while the circuits of the other published receivers are measured results.

Finally, table 7.3 summarizes a comparison of all receivers performances. In bold are the best results for each parameter.

Table 7.3: Comparison of Published Receivers

	This Work*	*(JUNIOR et al., 2016)***	*(ZENCIR N. S. DOGAN, 2002)***	*(KULKARNI et al., 2012)***
Gain (dB)	39	70.4	54	**80**
NF (dB)	4.5	**2.3**	3.8	7.9
P_{dc} (mW)	**10.4**	47	15	120
IIP3 (dBm)	-32.5	-63	-34	**+2**
Area (mm^2)	**0.54**	2.9	2.47	2.14
Freq (MHz)	401	401	435	470
Tech	130nm	130nm	500nm	180nm

* Parasitic extracted results ** Measured results

8 CONCLUSION

This thesis presented RF front-end using a superheterodyne receiver architecture with the 130nm CMOS technology that IBM provides. The work details the design of a low noise amplifier, an image rejection filter, and a downconverter mixer.

In the LNA chapter demonstrates how to implement a Common Source Cascode topology with a conjugate noise match technique. This technique permits to use a simple matching network minimizing the use of inductors obtaining a desired noise figure (that might achieve the minimum noise figure available for the circuit), but it has a poor impedance matching (in this work, the input resistance was around 36 ohms instead of the desired 50 ohms). Also, each current source of the LNA has a different temperature coefficient (TC). This strategy attempts to reduce the total noise figure dependence with temperature. With a proper TC, the noise figure at higher temperatures would decrease, and the noise figure at lower temperatures would increase, so the noise figure range of variation with temperature would decrease.

It was not possible to achieve the total integration of the image rejection filter due to the high value of its components. A Butterworth bandpass filter could attend the initial specifications but unrealistic values of inductors forced to use an external component in this architecture.

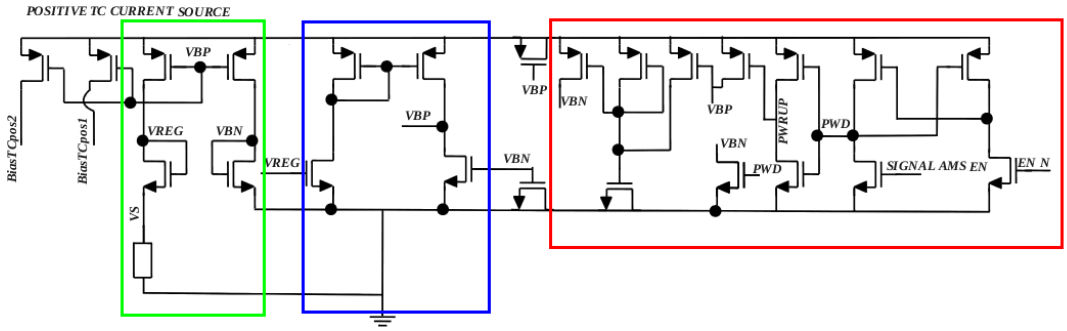
The mixer used a Gilbert Cell topology with a modification in the load stage. With a slight variation of voltage levels on each LO switch, it was possible to increase the conversion gain about 5 dB higher than the traditional Gilbert Cell load with acceptable noise figure performance. Also, a single-to-differential stage was implemented to make a proper connection between the single outputs of the LNA and filter to the differential input of the mixer.

Taking a performance comparison of the RF front-end of different receiver topologies, the proposed architecture obtained better results on linearity, power consumption, and total area. Although the noise figure and gain values were adequate for this application, other receiver topologies obtained better results.

8.1 Future Work

For future work, it is necessary to design the other receiver structures that operate at intermediary and baseband frequencies (IF mixer, VGA and AD converter). Also, the bias structures (current and voltage references) were not implemented in this work. One possibility of implementation of the current sources is a self-biased current source shown in figure 8.1. This structure uses a self-cascode MOSFET (green), a self-biased current source (blue) and a start-up/enable circuit (red) to generate a PTAT reference.

Figure 8.1: Current Source with positive TC



Source: The author

A similar idea can be employed to generate a CTAT reference. However, in this case, it must use a bandgap reference using bipolar to create a negative TC.

The LO input of the mixer is also ideal (although it was simulated with the signal that would cause the most distortion in the circuit). It is possible to implement the synthesizer using an N-integer topology to generate all LO frequencies with a cross-coupled voltage controlled oscillator topology.

It was not possible to send this work for manufacture because MOSIS has ended its operations. It is also possible to make a vertical porting to another technology node to make feasible manufacturing for further measurements.

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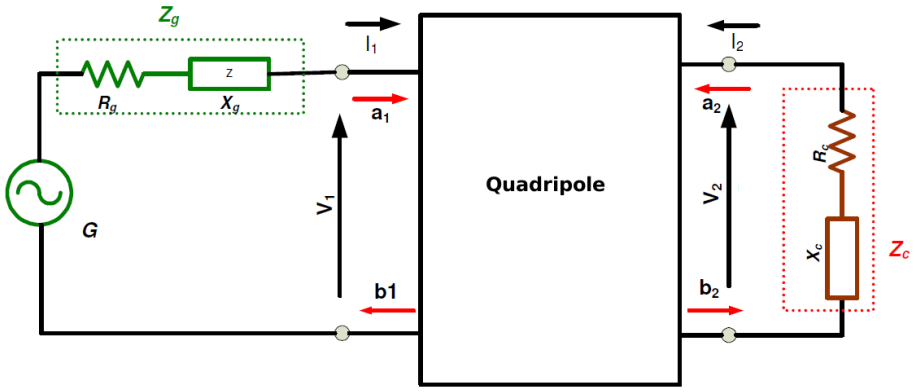
APPENDIX A — SCATTERING PARAMETERS

Generalized Scattering Parameters (S-Parameter) were defined by (KUROKAWA, 1965) and they are described as a relationship between a set of variables a_i e b_i, which are normalized complex voltages and are defined in terms of a voltage V_i, a current I_i and an arbitrary impedance Z_i at i^{th} circuit port to be analyzed as shown in figure A.1.

Figure A.1: Quadripole



Source: The author

The independent variable a_1 and a_2 are normalized as a function of incident voltages and the reference impedance Z_i:

$$a_1 = \frac{V_1 + Z_1 I_1}{2\sqrt{Z_1}} \tag{A.1}$$

$$a_2 = \frac{V_2 + Z_2 I_2}{2\sqrt{Z_2}} \tag{A.2}$$

The dependent variables b_1 and b_2 are normalized with the same incident voltages and impedance as follows:

$$b_1 = \frac{V_1 - Z_1 I_1}{2\sqrt{Z_1}} \tag{A.3}$$

$$b_2 = \frac{V_2 - Z_2 I_2}{2\sqrt{Z_2}} \tag{A.4}$$

The S-Parameters can be characterized as shown in equation A.5

$$S_{ij} = \frac{b_i}{a_j}\bigg|_{a_k=0, k\neq j} \tag{A.5}$$

Particularly for a two-port network, the S-parameter can be written in the matrix

form as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{A.6}$$

where:

S_{11} - Input return loss or input reflection coefficient;

S_{22} - Output return loss or output reflection coefficient;

S_{21} - Power gain;

S_{12} - Reverse gain or isolation;

S-parameters are also used to characterize the stability of circuits using a parameter called “Stern stability factor (K)” which is given by

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}| \cdot |S_{12}|} \tag{A.7}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$.

If $K > 1$ and $\Delta < 1$, then the circuit is unconditionally stable, i.e. it does not oscillate with any combination of source and load impedance(RAZAVI, 2011). LNAs might become unstable due to ground and supply parasitic inductance resulting from the packaging.