UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM MICROELETRÔNICA - PGMICRO

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Study of the Hysteretic Behavior in ZnO Nanoparticle Thin-Film Transistors

Thesis presented in partial fulfillment of requirements for the degree of Master in Microelectronics

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Porto Alegre, August, 2012.

CIP – CATALOGAÇÃO NA PUBLICAÇÃO

Vidor, Fábio Fedrizzi

Study of the Hysteretic Behavior in ZnO Nanoparticle Thin-Film / Fábio Fedrizzi Vidor – Porto Alegre: Programa de Pós-Graduação em Microeletrônica, 2012.

121 f.:il.

Thesis (Master) – Universidade Federal do Rio Grande do Sul. Programa de Pós-Graduação em Microeletrônica. Porto Alegre, BR – RS, 2012. Advisor: Gilson I. With.

1. Nanoparticles. 2. ZnO. 3. Thin-film transistors. 4. Low-cost electronics. I. Wirth, Gilson I.

ACKNOWLEDGMENT

I extend my sincere thanks to Prof. Dr.-Ing. Gilson I. Wirth, Prof. Dr.-Ing. Ulrich Hilleringmann and M.Sc Fabian Assion for their directions and support throughout my work. Their guidance and continuous flow of ideas and critical suggestions made the elaboration of this work possible. I also thank Thiago Hanna Both for his careful reading of this work and suggestions during the research. The excellent working environment and support of LaProt from UFRGS - Federal University of Rio Grande do Sul and Group Sensorik from University Paderborn are deeply appreciated.

I would like to express my gratitude to my friends from Brazil and Germany for their friendship over the years. Furthermore, I would like to thank the Federal University of Rio Grande do Sul for the free and high quality education.

This work is dedicated to my family and my wife, Jéssica, whose love and support have been a continual inspiration.

At the end, I would like to thank CAPES for the financial support that makes this work possible.

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LIST OF SYMBOLS

C_{ins}	Gate capacitance
E	Energy
$\vec{E}$	Electric Field
E_C	Minimum conduction band energy
E_F	Fermi level
E_{FM}	Metal Fermi level
E_{FS}	Semiconductor Fermi level
E_V	Maximum valence band energy
E_{VAC}	Vacuum level
g_m	Transistor transconductance
I_D	Drain current
I_G	Gate current
I_{loc}	Local current
L	Transistor length
K_B	Boltzmann's constant
q	Electron charge
S	Sub-threshold slope voltage
T	Absolute temperature
t_{ins}	Gate dielectric thickness
t_{ox}	Gate oxide thickness
V_{DS} , V_D	Drain-source voltage
V_F	Forward voltage
V_{GS} , V_G	Gate-source voltage
V_R	Reverse voltage
V_T	Threshold voltage
x	Position

W	Transistor width
$W_{\varphi B}$	Metal-semiconductor barrier width
W_F	Metal-semiconductor barrier width under forward bias
W_o	Metal-semiconductor barrier width at thermal equilibrium
W_R	Metal-semiconductor barrier width under reverse bias
$\Delta\varphi_{BF}$	Variation of barrier height under forward bias
$\Delta\varphi_{BR}$	Variation of barrier height under reverse bias
ε_o	Vacuum permittivity
ε_r	Relative permittivity
μ	Carrier mobility
μ_{FE}	Field-effect mobility
χ	Electron affinity
φ	Work function
φ_B	Barrier height from the metal to the semiconductor
φ_{Bo}	Intrinsic barrier height at thermal equilibrium
φ_{Bn}	Barrier height considering the Schottky effect
φ_i	Barrier height from the semiconductor to the metal
φ_M	Metal work function
φ_S	Semiconductor work function

LIST OF ABREVIATIONS AND ACRONYMS

ALD	Atomic layer deposition
ATO	Antimony tin oxide
FET	Field effect transistor
GZO	Gallium doped zinc oxide
ITO	Indium tin oxide
HDMS	Bis(trimethylsilyl)amine – an adhesion promoter
MISFET	Metal insulator semiconductor field effect transistor
MOSFET	Metal oxide semiconductor field effect transistor
MS	Metal-semiconductor junction
NBTI	Negative bias temperature instability
NMP	N-Methyl-2-pyrrolidone
PECVD	Plasma enhanced chemical vapor deposition
PEN	Polyethylene Naphthalate – a polymer
PES	Polyethersulfone – a polymer
PGMEA	Propylene glycol monomethyl ether acetate – a solvent
PI	Polyimide – a polymer
PMCF-m	Poly(melamine-co-formaldehyde)-methylated – cross-linker agent
PVP	Poly(4-vinylphenol) – a polymer
RF	Radio Frequency
RIE	Reactive ion etching
RDF	Random dopant fluctuations
RTS	Random telegraph signal
SEM	Scanning electron microscope
TFT	Thin-film transistor
UFRGS	Universidade Federal do Rio Grande do Sul

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ABSTRACT

During the last decades, the interest in flexible electronics has arisen. Systems that present benefits such as low cost, improved performance, transparency, reliability and better environmental credential are being extensively researched by several groups. Thin-film transistors (TFT) have good potential concerning these technologies. Therefore, zinc oxide (ZnO) based devices have been attracting researchers for its electrical, sensory and optical properties.

In this work, ZnO nanoparticles were used to integrate thin-film transistors, in which cross-linked PVP (Poly(4-vinylphenol)) and PECVD-SiO_2 (plasma enhanced chemical vapor deposition silicon dioxide) were used as gate dielectric layer. The complete integration process targets low cost and low temperature requirements (< 200°C). For this reason, simple process techniques as spin-coating or sidewall-etchback were used. Unfortunately, there are different reliability concerns in ZnO devices, among them aging or hysteresis. An experimental investigation of the hysteresis in the transfer characteristic is performed, and a qualitative model for the observed behavior is proposed. It was observed that the hysteresis direction is affected by temperature variation when the polymeric dielectric is used. The PVP bulk polarization, the traps in nanoparticles and at the polymeric dielectric interface, as well as the desorption of oxygen molecules in the surface of the nanoparticles, were attributed as the main cause of the hysteretic behavior.

Moreover, capture and release of charge carriers by traps at determined current paths in the transistor lead to discrete current fluctuations in stress tests, similar to random telegraph signal (RTS) reported in nanoscale MOSFET. This result supports the hypothesis of charge transport mechanism (percolation paths) in nanoparticulate ZnO.

Keywords: Nanoparticles, ZnO, thin-film transistors, low-cost electronics.

Estudo da Histerese em Transistores de Filmes Finos de Nanopartículas de Óxido de Zinco

RESUMO

Nas últimas décadas, o interesse na eletrônica flexível tem aumentado. Sistemas que apresentam benefícios, tais como: baixo custo, melhor desempenho, transparência, confiabilidade e melhores credenciais ecológicas, estão sendo extensivamente pesquisados por vários grupos. Os transistores de filmes-finos possuem potencial para alcançarem essas características. Dispositivos baseados em óxido de zinco (ZnO) tem atraído pesquisadores devido as suas propriedades elétricas, sensoriais e ópticas.

Neste trabalho, nanopartículas de ZnO foram utilizadas como semicondutor ativo e *cross-linked* PVP (polivinilfenol) e PECVD-SiO_2 (*plasma enhanced chemical vapor deposition silicon dioxide*) como dielétricos de porta para integrar transistores de filmes-finos. Este processo de integração tem por objetivo os pré-requisitos de baixo custo e baixa temperatura (<200°C). Por esta razão, a utilização de técnicas de integração simples, como o *spin-coating* ou a técnica de *sidewall-etchback*, foram utilizadas. Infelizmente, existem problemas relacionados à confiabilidade em dispositivos baseados em ZnO, entre eles a degradação no tempo ou a histerese. Após uma investigação experimental da histerese na característica de transferência, um modelo qualitativo para o comportamento observado é proposto. Observou-se que a direção da histerese é afetada pela variação da temperatura quando o dielétrico polimérico é usado. Baseando-se na caracterização dos transistores, a polarização do PVP, as armadilhas na superfície das nanopartículas e na interface com o dielétrico, bem como a liberação de moléculas de oxigênio da superfície das nanopartículas foram atribuídas como as principais causas da histerese.

Além disso, uma flutuação discreta da corrente é observada em testes de estresse devido à captura e liberação de portadores em determinados caminhos de corrente no transistor, semelhante a *random telegraph signal* (RTS), relatado em MOSFET nanométricos. Este resultado suporta o hipotético mecanismo de transporte de elétrons (caminhos de percolação) em filmes compostos por ZnO nanoparticulado.

Palavras-Chave: Nanopartículas, ZnO, Transistor de filmes finos, eletrônica de baixo custo.

1 INTRODUCTION

Thousands of organizations have been pursuing printed, organic and flexible electronics. While some of these technologies are already mature, with substantial growth in thin-film photovoltaics market, for instance, others such as thin-film transistors, developed by hundreds of organizations, are becoming only now commercially available. The benefits of these new electronics are numerous - ranging from lower cost, improved performance, flexibility, transparency, reliability and better environmental credentials. Existing electronics and electrical products will be impacted by many newly created applications, as sensory electronic skins and transparent screens, and their extent is countless (SUN et al., 2007), (WONG et al., 2009) and (AXISA et al., 2005). Figure 1.1 presents some potential application of these new technologies, such as transparent screens and flexible electronic circuits.

http://vitsnspeceendeavours.blogspot.com http://news.bbc.co.uk/2/hi/technology/

Figure 1.1: Application of transparent and flexible electronics.

To integrate thin-film transistors the use of polycrystalline silicon as an active material requires expensive and complex integration processes. This is the main reason for the growing interest in solution-processed semiconducting alternatives, which are low-cost and low temperature processes. Transistors based on organic materials, particularly pentacene, are an alternative for polycrystalline silicon. However, organic semiconductors present limited channel mobility, air instability and electrical reliability issues, which generally requires further integration steps in order to overcome these issues, compromising the cost of the integration process (LEE et al., 2008) and (WONG et al., 2009).

Solutions based on inorganic materials have gained focus among researchers as a possible substitute for active semiconductors. Zinc oxide has attracted attention as a key material because of its electrical, sensory and optical properties. This material is already widely spread in society, for example, in the manufacturing of paintings, cosmetics,

pharmaceutical, plastics, batteries, electrical equipments and textiles (JAGADISH et al., 2005).

Nowadays, there are some very promising electronic devices employing ZnO as semiconductor under research. However, the techniques used require high vacuum or high temperatures (LEE et al., 2008), which are not suitable for low-cost production on flexible polymeric substrates (BUBEL et al., 2009) and (WONG et al., 2009).

Focusing on low-cost applications, a high throughput manufacturing process is needed. This is normally achieved by simple techniques such as spin coating, inkjet-printing or roll-to-roll processes. Nanoparticulate ZnO presents potential characteristics, and with recent improvements in the growth technology of ZnO nanostructures, new opportunities and applications for ZnO are emerging, i.e., flat screen and active matrix liquid crystal displays, gas, chemical and biological sensors, and UV light emitters (WONG et al., 2009), (FAN et al., 2005), (WANG et al., 2004), (MORKOÇ et al., 2009) and (JIN et al., 2008). By using nanoparticulate ZnO, it is possible to directly process the semiconductor from a liquid dispersion without the necessity of a costly or high temperature process (BUBEL et al., 2009).

Although the ZnO nanoparticles present good prospective and can be produced at low cost and high quality, some problems are observed when using nanoparticles to integrate thin-film transistors (TFT). The main concerns about the ZnO nanoparticle transistors are the hysteresis when using poly(4-vinylphenol) (PVP) (WOLFF et al., 2011-b,c), (FABER et al., 2009), (LEE et al., 2006) or SiO_2 (SUN et al., 2005), (ASSION et al., 2010) as gate dielectric; the low field effect mobility due to the nanoparticle interconnections (LEE et al., 2007); the roughness of the nanoparticles at the interface with the gate dielectric (OKAMURA et al., 2008), (WALTHER et al., 2010); characteristics variation depending on the bending state when integrated on flexible substrates; and the high temperature process (above 200ºC), which is not adequate for some kinds of flexible substrates (LEE et al., 2007), (LEE et al., 2008), (WALTHER et al., 2010).

In this work, ZnO nanoparticles were used to integrate thin-film transistors, in which cross-linked PVP and PECVD-SiO_2 were used as gate dielectric layer. A comprehensive electrical characterization is carried out, focusing on the experimental investigation of the hysteresis in the transfer characteristic, and a qualitative model for the observed behavior is proposed.

This text is structured as follow. The second section discusses metal-semiconductor contacts. In the third section, zinc oxide and polymeric gate dielectric are reviewed. The ZnO TFT properties and the integration process are presented in the fourth section. In the fifth section, the results of the characterization of the transistors are reported together with a discussion of the origin of the hysteretic behavior in ZnO nanoparticle TFT. The conclusion is presented in the sixth section. The Appendix A and B present the wafer cleaning and measurement procedures, respectively. In the Appendix C, graph and tables are exposed, while in Appendix D the summary of this Master thesis in Portuguese.

2 METAL-SEMICONDUCTOR CONTACTS (SCHOTTKY JUNCTIONS)

Because of metal-semiconductor contacts are partly responsible for the operation of the TFT integrated in this work, they are reviewed in this section. The most relevant behavior is concisely presented. First, the metal and semiconductor energy scales are reviewed, as well as their contact under thermal equilibrium, forward and reverse bias. Second, a brief explanation on the current transport process and on Ohmic contact is presented.

2.2 Energy Scales

One of the first steps to understand the contact between metals and semiconductors is regarding their representation in the energy scale and band diagram, separately. The vacuum level (E_{VAC}) is defined as the minimum energy an electron requires in order to completely free itself from a metal or semiconductor (PIERRET, 1996). In metals, almost all states are filled in up to the Fermi level (E_F) and empty at energies above that. In intrinsic semiconductors, however, almost all states are filled in the valence band, while the conduction band is almost empty. This is in accordance to the Fermi-Dirac distribution function (Eq. 2.1), which specifies the probability of an available state with energy E to be occupied by an electron under equilibrium conditions.

$$f_n(E) = \frac{1}{1 + e^{\frac{E - E_F}{K_B T}}} \tag{2.1}$$

in which, E_F is the Fermi level, K_B is the Boltzmann constant and T is the absolute temperature.

Figure 2.1 depicts the Fermi-Dirac distribution for the temperatures $T = 0\,K$ and $T > 0\,K$. Since there are no states in the semiconductor within the forbidden gap, only energies below the valence band maximum or above the conduction band minimum are occupied (PIERRET, 1996), (COLEMAN, 2008).

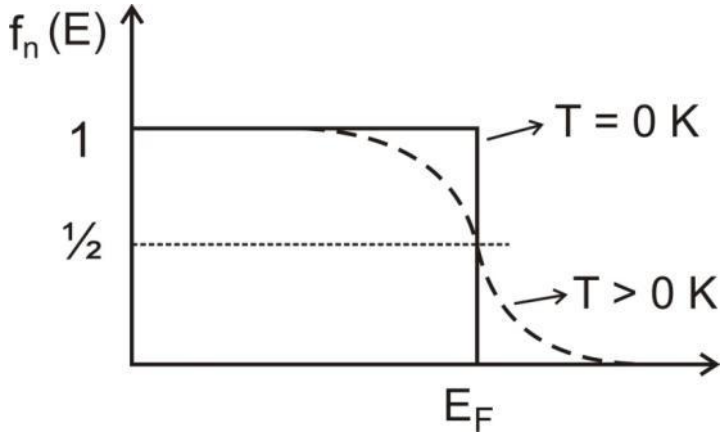


Figure 2.1: Fermi-Dirac distribution for T = 0 K and T > 0 K.

Figure 2.2 shows the energy state diagram of a metal and an n-type semiconductor; the vacuum level and work function (φ), which is the energy required to free an electron at the Fermi level from the metal or semiconductor. In metals, the work function is an invariant property of a specific metal. In semiconductors, the Fermi level varies depending on the doping level. This is the main reason for the electron affinity (χ) to be introduced, which is the difference between the vacuum level and the conduction band edge (PIERRET, 1996).

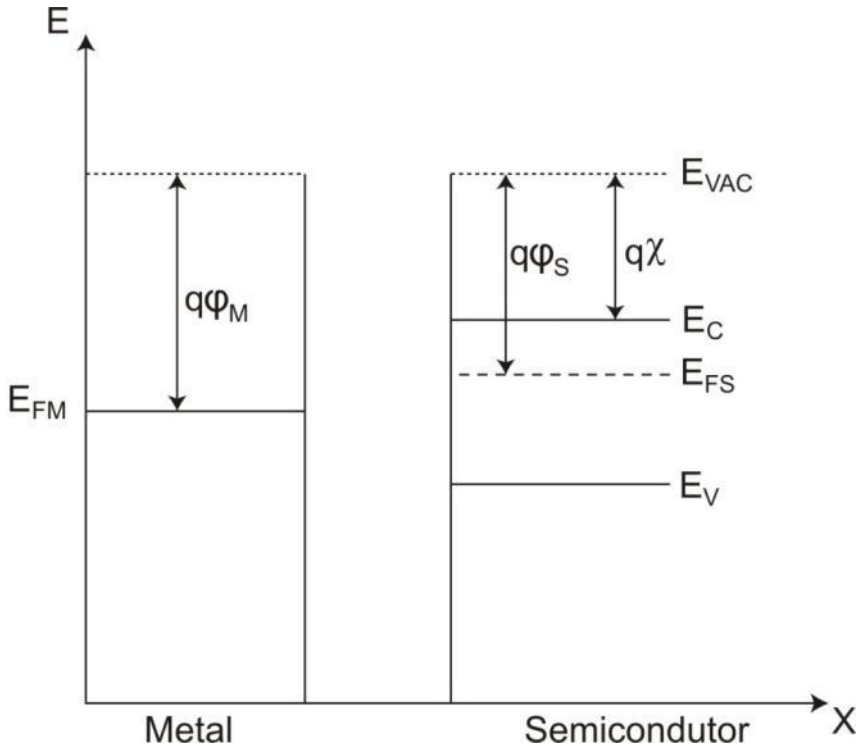


Figure 2.2: Energy plotted as function of position, before the contact between metal and semiconductor. The work function of the metal is higher than that of the n-type semiconductor.

2.3 Metal-Semiconductor Contact

If the Fermi level in the semiconductor is higher than in the metal, for a short time after the conceptual contact formation, electrons from the semiconductor create a surface depletion region (represented in gray in Figure 2.3) and a growing barrier against the electron transfer from the semiconductor into the metal. This will continue until the transfer rate across the interface is the same in both directions, and the Fermi level is the same through the structure (PIERRET, 1996). Figure 2.3 presents the equilibrium energy for an ideal metal to n-type semiconductor contact, Figure 2.4a represents it under forward bias, and Figure 2.4b under reverse bias. A variation in the depletion region width can be observed. The barrier height ($q\varphi_B$) from the metal to the semiconductor is not altered under different bias operation; on the other hand, the barrier from the semiconductor to the metal is sensitive to the applied bias. As explained by Sze et al. (2006), interface states also play a role on metal-semiconductor junctions, pinning the Fermi level at the interface. Therefore the barrier heights determination is not uniquely defined by metal work function and semiconductor electron affinity. Further explanation on this effect is detailed in (SZE et al., 2006).

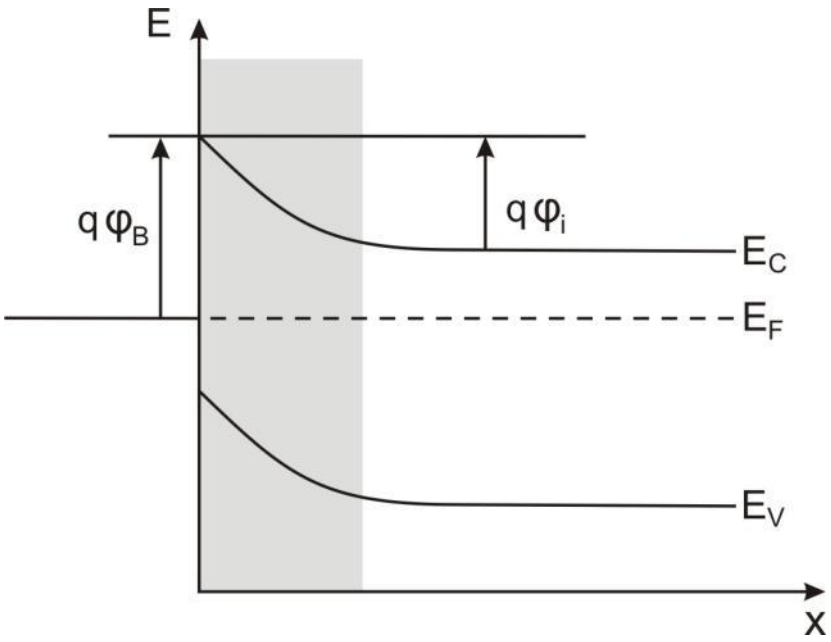
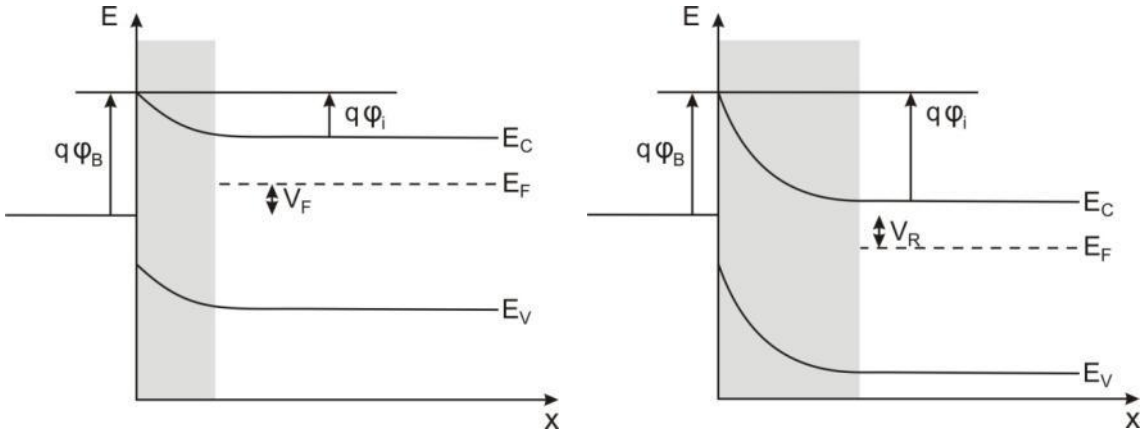


Figure 2.3: Energy-band diagram in metal on n-type semiconductor in thermal equilibrium. $q\varphi_B$ denotes the barrier height from the metal to the semiconductor and $q\varphi_i$ the barrier height from the semiconductor to the metal.



(a) (b)

Figure 2.4: Energy-band diagram in metal on n-type semiconductor under (a) forward bias and (b) reverse bias.

In the presence of an electric field, the barrier energy for charge carrier emission is image-force-induced lowered (SZE et al., 2006). This is called image-force lowering or Schottky effect. The barrier reduction is smaller than the barrier itself; on the other hand the barrier depends on the applied voltage as depicted in Figure 2.5. The intrinsic barrier height at thermal equilibrium is represented by $q\varphi_{Bo}$; when considering the Schottky effect it is reduced to $q\varphi_{Bn}$; $\Delta q\varphi_F$ and $\Delta q\varphi_R$ are the variation in the barrier height under forward and reverse bias operation respectively. Again, a more detailed explanation can be found in (RHODERICK et al., 1988), (SZE et al., 2006), (RIDEOUT, 1978).

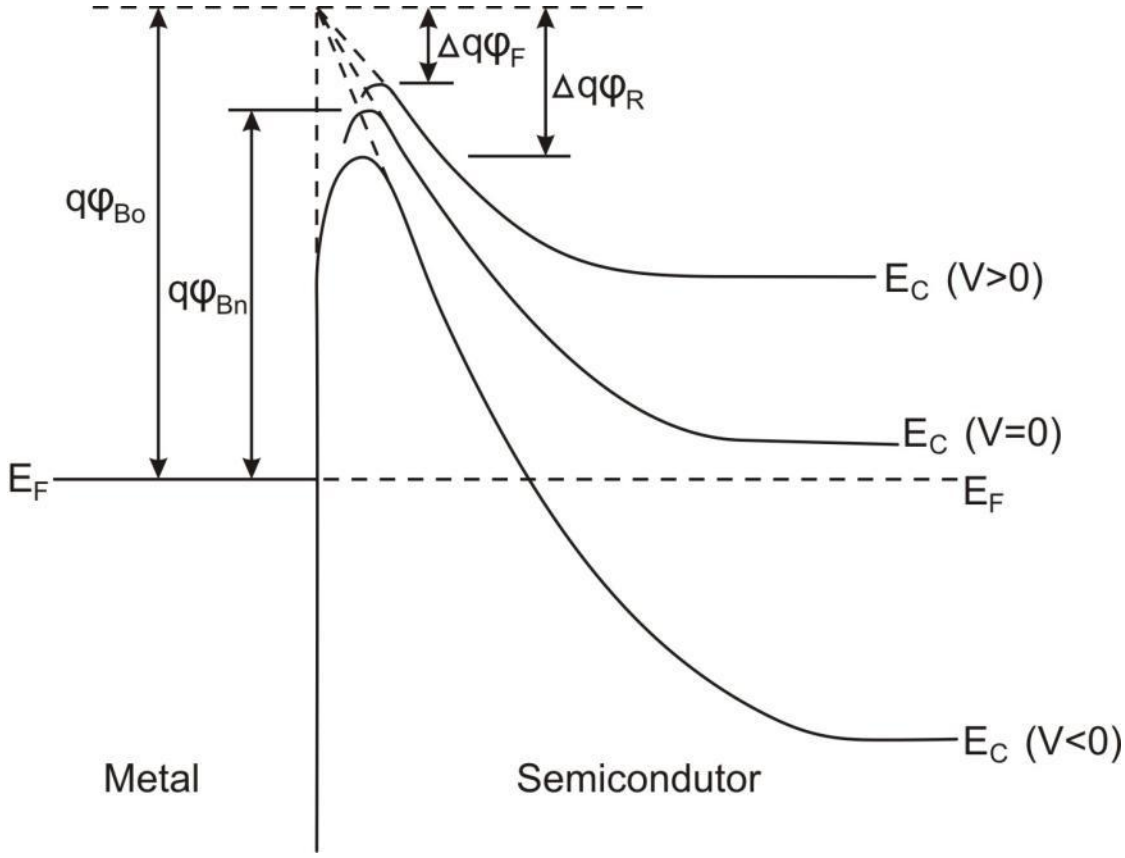


Figure 2.5: Metal-Semiconductor barrier including the Schottky effect under different bias conditions. Adapted from (RIDEOUT, 1978).

Rhoderik et al. (1988) explains that there are different transport mechanisms through the Schottky barriers. Figure 2.6 shows the carrier transport across metal-semiconductor in an n-type semiconductor under forward bias. The mechanisms are:

a) Emission of electron from the semiconductor over the top of the barrier into the metal;

b) Quantum-mechanical tunneling through the barrier;

c) Recombination in the space-charge depletion region;

d) Recombination in the neutral region ("hole injection").

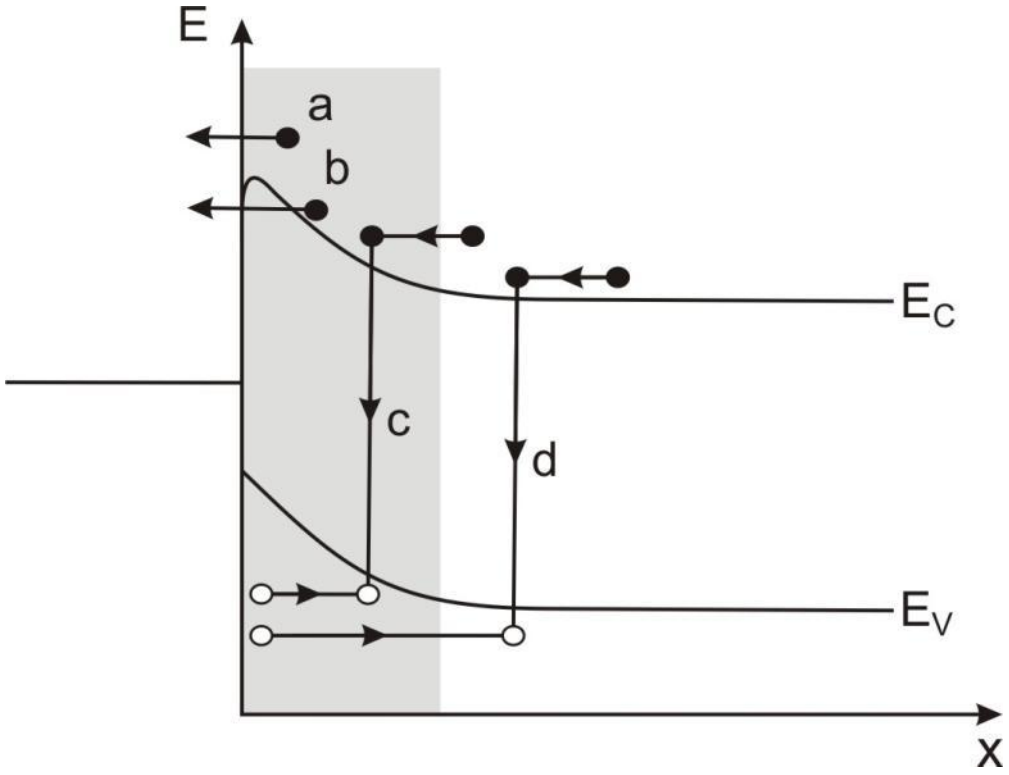


Figure 2.6: Transport process in a forward-biased Schottky barrier.

Process (a) is the most important in most of the Schottky diodes and the other processes are regarded as deviations on this ideal behavior. For a p-type semiconductor, the inverse process is observed, which means that instead of holes there are electrons and instead of electrons there are holes (RHODERICK et al., 1988).

All the previous considerations about the metal-semiconductor contacts consider a rectifying behavior. However, Ohmic contacts present low impedance regardless of their biasing polarity. In other words, the barrier is present, although it is transparent to carrier transport (due to tunneling, process (b) from Figure 2.6). They are normally achieved with heavily doped semiconductors (PIERRET, 1996). Another approach to achieve Ohmic contact is applying bias to the contacts in order to shrink the barrier width, allowing the electron tunneling through the barrier (RHODERICK et al., 1988). This effect can be observed in Figure 2.7, in which the barrier width shrinks when reverse bias is applied to the junction. Additionally, this effect is partly responsible for the functioning of ZnO nanoparticle TFT (HILLERINGMANN et al., 2011).

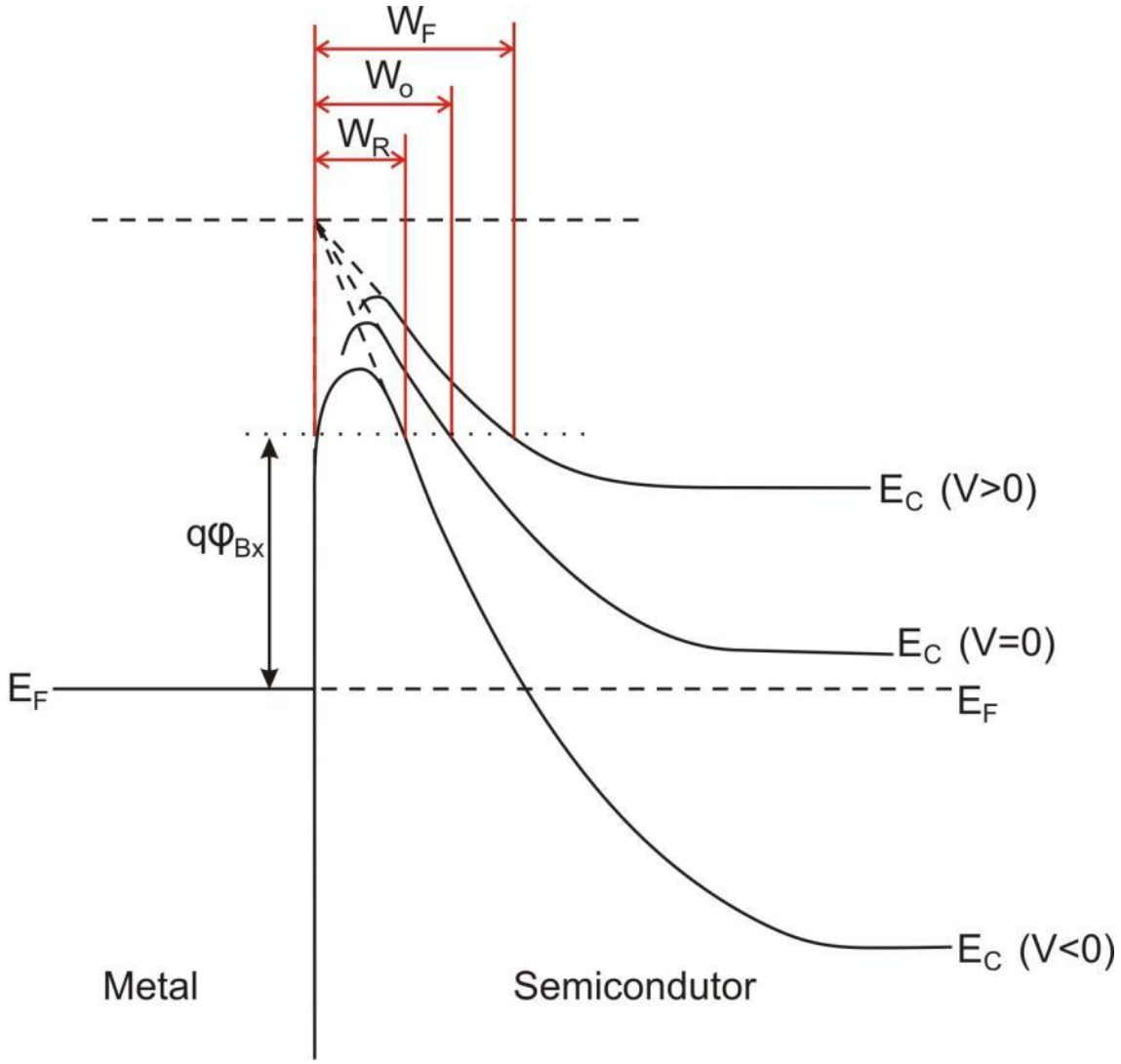


Figure 2.7: Detail of the barrier width variation under different electrical bias.

3 ZINC OXIDE AND GATE DIELECTRIC POLYMER

In this section, characteristics of the ZnO are presented, focusing mainly on its electronic and optic properties. Furthermore, the characteristics of the ZnO nanoparticles used to integrate the thin-film transistors will be presented. Also, some properties of the poly(4-vinylphenol) (PVP) used as a gate dielectric polymer are exposed.

3.1 Zinc Oxide Properties

Zinc oxide is a direct, wide bandgap semiconductor material (3.37 eV), meaning it is transparent to visible light (FAN et al., 2005) and (WANG et al., 2004). This characteristic, combined to the low temperature processes required and its non-toxicity, is one of the reasons why ZnO has been gaining considerable interest for integrating transparent thin-film transistor (FAN et al., 2005) and (WANG et al., 2004). Another reason is its air-stability which can be achieved by proper fabrication or annealing. As most of the II-VI binary compound semiconductors, ZnO usually presents a hexagonal wurtzite crystal structure, as shown in Figure 3.1.

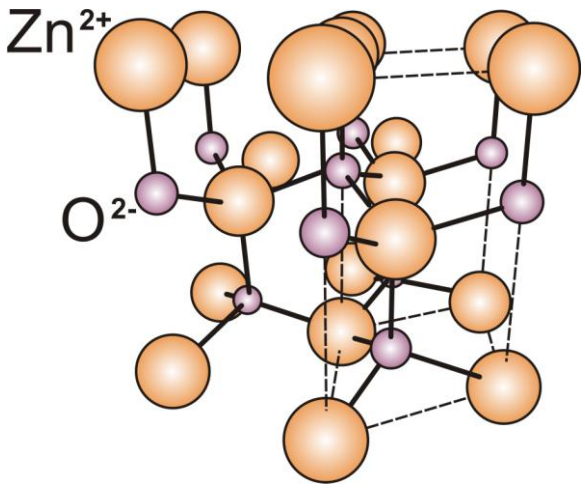


Figure 3.1: ZnO's chemical structure. One unit cell is outlined for clarity. Adapted from (JAGADISH et al., 2004)

One of the issues regarding ZnO is doping. ZnO is predicted to be an intrinsic semiconductor. On the other hand, it is found predominantly as n-type semiconductor due to the presence of a high concentration of native defects in the form of oxygen

vacancies and zinc interstitials that contribute to deep and shallow energy states, respectively (JAGADISH et al., 2004). Other authors, attribute the unintentional n-type conductivity in ZnO to hydrogen, which occurs exclusively in the positive state in ZnO; i.e., it always acts as a donor (VAN DE WALLE, 2000) and (JANOTTI et al., 2007). The obtainment of p-type ZnO has been quite difficult because of the carrier compensation by the native defects of ZnO, as explain Jagadish et al. (2004).

The Table 3.1 shows some properties of ZnO:

Table 3.1: Physical properties of ZnO.

Property	Value
Relative dielectric constant	8.66
Gap Energy	3.37 eV, direct
Intrinsic carrier concentration	$< 10^6$ cm^{-3}
Electron mobility (T = 300 K)	200 $cm^2/(Vs)$
Hole mobility (T = 300 K)	5 - 50 $cm^2/(Vs)$

Source: (FAN et al., 2005)

Metal oxide semiconductor thin films are the most promising devices among solid state chemical sensors (JAGADISH et al., 2004) and ZnO based sensors are widely researched (FAN et al., 2005), (WANG et al., 2004), (QIN et al., 2011), (LIU et al., 2009) and (XU et al., 2000). Due to its excellent piezoelectric properties, it is possible to integrate sensory devices based on SAW (surface-acoustic wave) (FAN et al., 2005), (WANG et al., 2004), (JAGADISH et al., 2004), (QIN et al., 2011). In addition, ZnO is already used as an effective gas, chemical and biological sensor material, since absorbed species interact with surface complexes such as O^-, O^{-2} ,H^+ and OH^- modifying the charge distribution (WANG et al., 2004), (JAGADISH et al., 2004) (MORKOÇ et al., 2009), (LIU et al., 2009) and (XU et al., 2000).

3.2 Zinc Oxide Nanoparticles

ZnO nanostructures are presented in several forms: nanobelt, aligned nanowire arrays, nanotubes, array of propellers, mesoporous, nanowires, cage and shell structures, nanosprings and spheres (JAGADISH et al., 2004), (FAN et al., 2005) and (WANG et al., 2004). Several of these nanostructures can be observed in Figure 3.2.

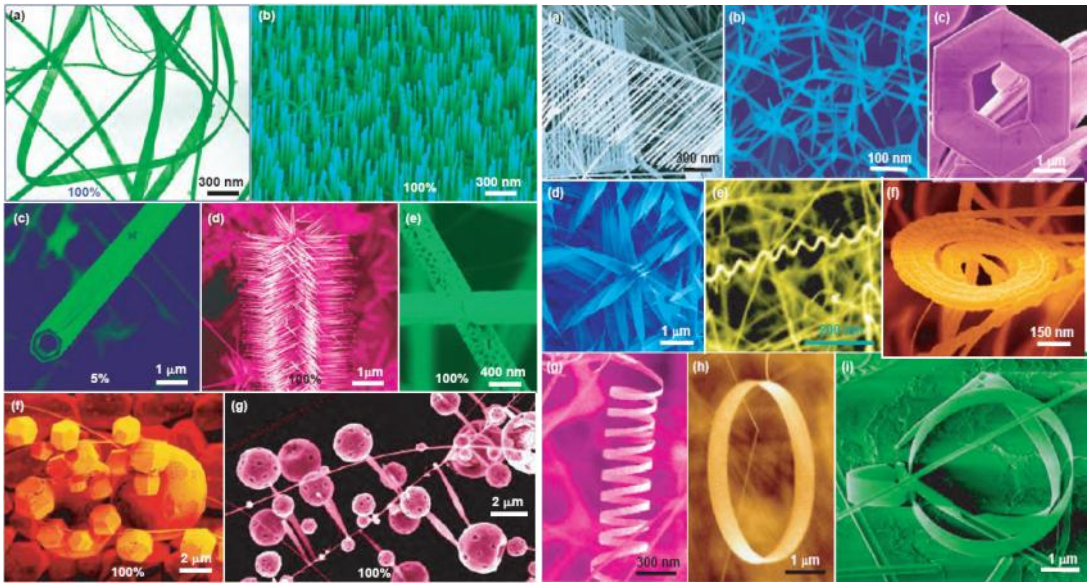


Figure 3.2: Various ZnO nanostructures (JAGADISH et al., 2004).

The ZnO nanoparticles used to integrate the thin-film transistors were the VP AdNano ZnO 20 DW (dispersion of VP AdNano ZnO 20 in water) distributed by Degussa AG (2006). Pure feed stocks and non-contaminating ZnO are used in the synthesis process, so the product is obtained in high purity (zinc oxide content > 99.5%). AdNano zinc oxide is a crystalline solid exhibiting the hexagonal wurtzite lattice. The smallest units of the compound, only visible using an electron microscope, are the primary particles in the range of about 15-30 nm of diameter. Based on this high degree of particle fineness, 1 gram of VP AdNano ZnO 20 can provide an active surface of 20-25 m^2. The primary particles are usually not isolated. They are typically bounded to each other to form aggregates. The effective particle size, which is present in dispersion, for example, is about 100 nm (DEGUSSA, 2006).

Okamura et al. (2008) states that nanoparticulate zinc oxide is regarded as one of the most promising inorganic materials for printable n-type thin-film transistor, due to the compatibility with solution, low-temperature, and high throughput processes.

3.3 PVP Properties

Poly(4-vinylphenol) is a weak acid polymer. Due to its variety of applications and simple fabrication process, many research groups have investigated its properties (VICCA et al., 2010), (BENSON et al., 2008), (JUNG et al., 2005) and (HWANG et al., 2006). Applications of the polymer include the use as gate dielectric insulator in the microelectronic field and responsive surface coating (UPPALAPATI et al., 2010).

The interesting fact about PVP for this work is the fabrication of thin films for potential application as dielectric applied via spin-coating process. However, when the dielectric is a polymer, a cross-linker agent should be applied to support the impact of solvents and bases from further process steps. The cross-linking reaction should not leave any mobile ions in the film and the cross-linker agent used in the photoresist should be avoided (VICCA et al., 2010). Moreover, the cross-linked polymer should have a very smooth surface, high electrical field strength, preferably a high dielectric

constant, high purity, and be hydrophobic while still allowing sufficient adhesion to adjacent layers, as in ZnO nanoparticles dispersion.

The cross-linked PVP is normally dissolved in propylene glycol methyl ether acetate (PGMEA) and poly(melamine-co-formaldehyde)-methylated is used as a cross-linker agent (VICCA et al., 2010), (CHOI et al., 2008) and (LIM et al., 2007). Figure 3.3 presents the chemical structures of such polymeric dielectrics, where (a) is the pure PVP, (b) is the cross-linker agent and (c) is the cross-linked PVP.

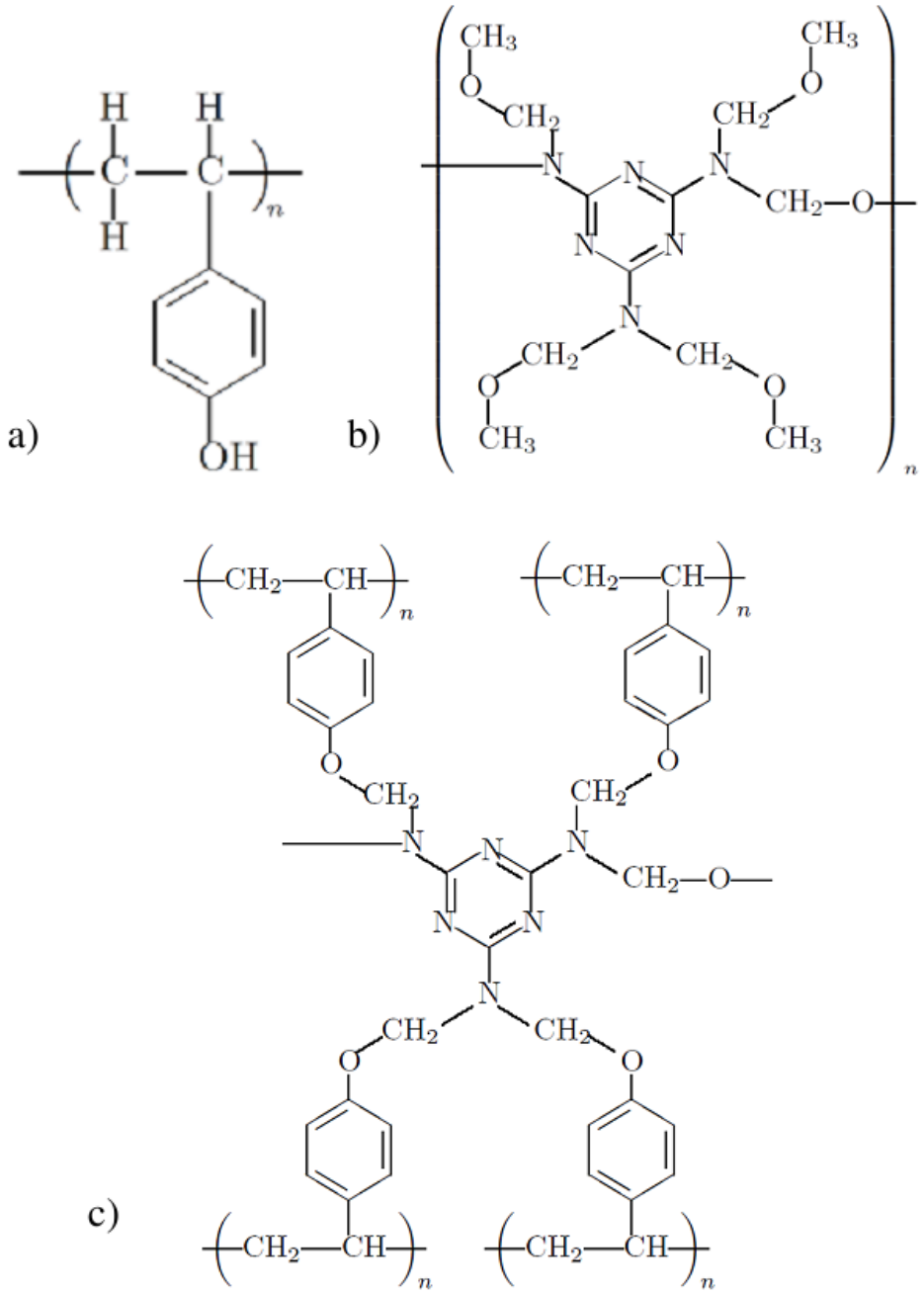


Figure 3.3: Chemical structures of polymeric dielectrics used in this work. (a) Pure PVP, (b) cross linker agent and (c) a cross-linked PVP chemical structure.

Lim et al. (2007) and Faber et al. (2009) report the use of PVP, especially the effect of hydroxyl (OH-) groups in the polymeric gate dielectrics, which may lead to a shift in the threshold voltage depending on the direction of the gate-source voltage sweep, corresponding to a hysteretic behavior in the transfer characteristics. The relative permittivity and the insulator thickness were obtained from (LEHDE, 2010) and their values are $\varepsilon_r = 5.9$ and $t_{ins} = 0.18\,\mu m$ respectively, under the conditions used in the transistor's integration.

4 ZINC OXIDE THIN-FILM TRANSISTOR

In this section, characteristics of ZnO nanoparticle based thin-film transistors (TFT) are presented, as well as the electron transport mechanism in nanoparticulate ZnO film and the transistor integration process. Furthermore, the transistor evolution in our group, a cooperation between University of Paderborn, Germany and UFRGS (Universidade Federal do Rio Grande do Sul), Brazil, and among other research groups is exposed.

4.1 Thin-Film Transistor Properties

In order to understand how the TFT operates, a basic schematic representation of its structure will be used, as shown in Figure 4.1.The channel layer - a semiconductor such as amorphous/poly silicon or an organic/inorganic semiconductor - is used to transport the carriers from source to drain, normally made of metal, which creates a Schottky barriers with the semiconductor. The gate dielectric layer separates the gate electrode from the semiconductor channel. The channel width (W) and length (L) and the gate dielectric thickness (t_{ins}) are the main TFT dimensional characteristics. As depicted in Figure 4.1, the active channel region comprises the rectangular area between source and drain contacts.

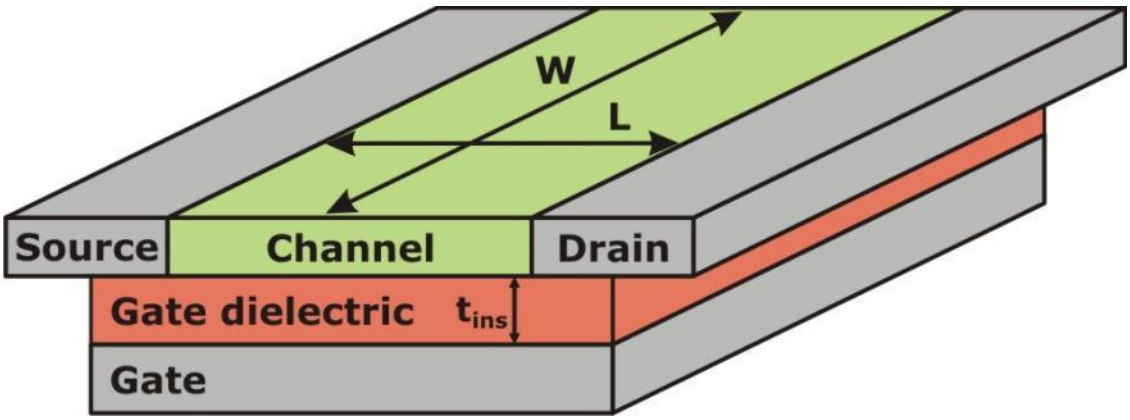


Figure 4.1: Simplified schematic of a TFT structure.

Figure 4.2 presents the key elements of the TFT operation, with electric bias and charge polarities for an n-channel device (channel current flow is mainly by electrons). The voltage applied to the gate electrode (V_{GS}) modulates the charge density in the channel through the gate capacitance. The magnitude of the induced charge density is proportional to the applied gate voltage, which produces a corresponding variation in source-to-drain conductance. For an n-channel device, for instance, when a positive gate

voltage is applied, the electron concentration in the channel increases, while a negative voltage reduces the channel electron density.

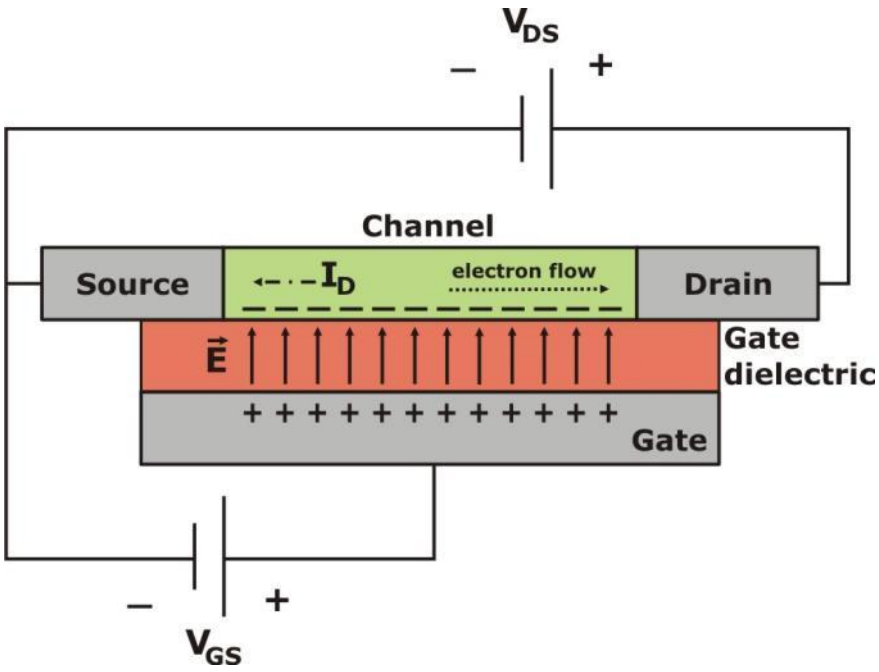


Figure 4.2: Schematic illustration of the central elements of TFT operation.

Another way to explain the formation of the channel is shown in Figure 4.3, in which ideal energy band diagram are shown, depicting the view through the gate of an n-channel accumulation-mode TFT. The device at equilibrium, i.e., with no applied electric bias, is depicted in Figure 4.3a. Negative bias repels the mobile electrons from the interface, creating a depletion region (Figure 4.3b). Comparing this bias condition to the equilibrium one, a conductance reduction is expected due to the reduced density of mobile electrons in the channel. Conversely, positive bias attracts mobile electrons forming an accumulation region near the insulator/channel interface, increasing its conductance (Figure 4.3c) (HONG et al., 2008).

A distinguishing feature of a TFT compared to a conventional MOSFET (metal-oxide-semiconductor field-effect transistor) is that the carrier transport in the channel typically occurs in an accumulation layer in a TFT, whereas, in a MOSFET, it occurs in an inversion layer (HONG et al., 2008).

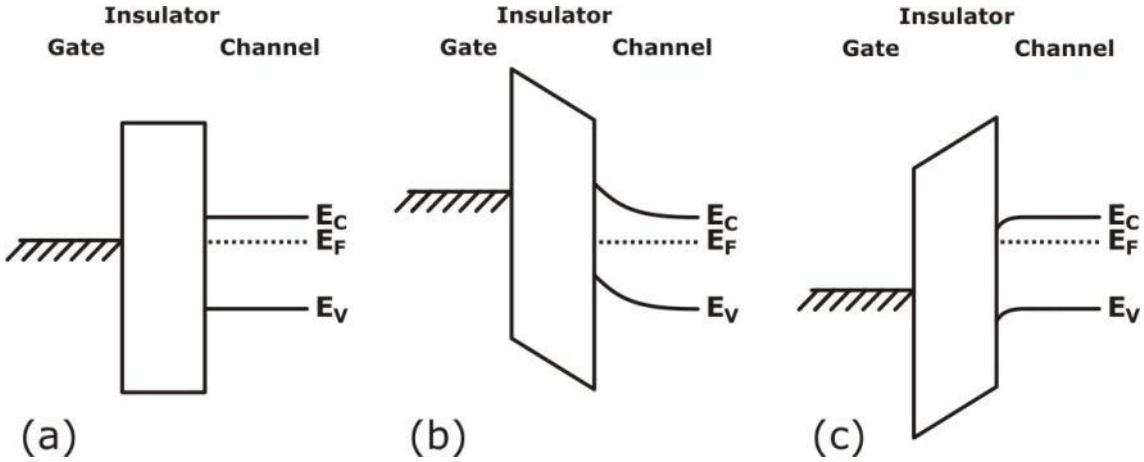


Figure 4.3: Energy band diagram as views through the gate for (a) equilibrium, (b) depletion ($V_{GS} < 0\ V$), and (c) accumulation ($V_{GS} > 0\ V$).

Another important element to understand TFT operation, especially for ZnO TFT integrated in this work, is the behavior of the Schottky barriers under different bias condition. In Figure 4.4a, the unbiased ZnO TFT band diagram is presented, and the presence of Schottky barriers in both metal contacts (drain and source) are observed. ZnO is an intrinsic n-type semiconductor (Section 3); however, the Fermi level exact position, represented by a dash line, is uncertain. By applying a drain voltage in the transistor, as in Figure 4.4b, the drain potential lowering is expected. However, the barrier's width is almost the same, and the electrons cannot tunnel through the barrier.

When the gate is above the threshold voltage (Figure 4.4c), the barrier width shrinks (Ohmic contacts), and the electrons tunnel through the drain and source barriers (WOLFF et al., 2010). In the bulk, the electrons "flow" due to gate voltage effect in the region near the interface of the semiconductor and the gate dielectric (channel).

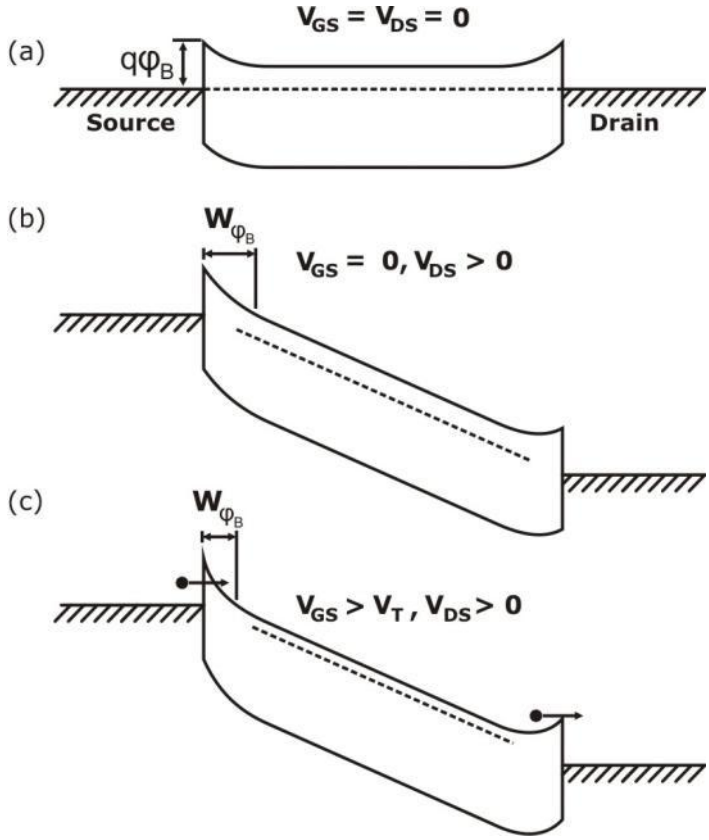


Figure 4.4: Band diagrams along semiconductor surface under various biases.

Even with the above cited differences, the TFT operation is normally expressed in terms of the drain current (I_D) as a function of the gate-to-source (V_{GS}) and the drain-to-source (V_{DS}) voltages. Eq. 4.1 represents the TFT operation; it is the same used to model the metal-insulator-semiconductor field-effect transistor (MISFET). Although, it may not provide quantitative agreement with the device, it represents the transistor's basic operation, as explained by Jagadish et al. (2004).

$$I_D = \begin{cases} 0 & ; V_{GS} \leq V_T \\ \dfrac{\mu C_{ins} W}{L}\left[(V_{GS} - V_T)V_{DS} - \dfrac{V_{DS}^2}{2}\right] & ; V_{DS} \leq V_{GS} - V_T \\ \dfrac{\mu C_{ins} W}{2L}[V_{GS} - V_T]^2 & ; V_{DS} > V_{GS} - V_T \end{cases} \quad (4.1)$$

where, μ is the carrier mobility, C_{ins} is the gate capacitance, W is the transistor width, L is the transistor length and V_T is the threshold voltage.

A more precise model for the TFT operation adds to the above model series resistance to the drain/source contact. Also, there is another model (3-layer model) which takes into account that, in TFT devices, the active semiconductor is a thin layer, and therefore it considers three vertical current paths (channel, bulk and interface) to represent the transistor operation. More sophisticate models such as the comprehensive depletion-mode model or the discrete trap model also describe the TFT as explained by Hong et al. (2008).

On the other hand, for the analysis in this work, the model presented through Eq. 4.1 will be used, since it represents the basic operation of the ZnO TFT and several research groups used the model for characterizing their devices or as base for other models.

In practical terms, there are four general thin-film transistors configuration as depicted in Figure 4.5. Devices can be structured either in staggered or in coplanar configuration (HONG et al., 2008). The position of drain/source electrodes and gate dielectric in relation to the channel defines the configuration. In coplanar structures (Figure 4.5b and Figure 4.5d), the drain/source electrodes and the insulator are located in the same side of the channel, and in staggered structures (Figure 4.5a and Figure 4.5c) the drain/source electrodes and the insulator are located in opposites sides.

Other consideration when comparing the coplanar and staggered configuration is regarding the current flow in the transistor as shown in Figure 4.5 (HONG et al., 2008). In the coplanar configuration, the drain/source electrodes are in direct contact with the induced channel, enabling a direct current flow; in staggered devices, the current must flow vertically to the induced channel before flowing horizontally towards the drain. In the last configuration, due to the large contact area between drain/source and the semiconductor, a minimal contact resistance is achieved.

Additionally, the devices can be classified as either bottom-gate (Figure 4.5a and Figure 4.5b) or top-gate devices (Figure 4.5c and Figure 4.5d). A bottom-gate TFT, which has the gate electrode and dielectric underneath the channel, is normally referred as an inverted TFT.

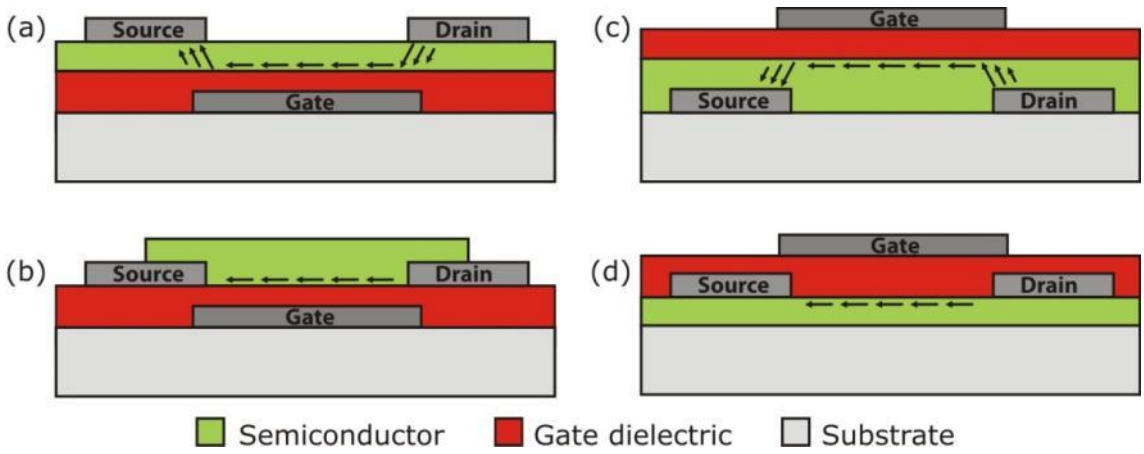


Figure 4.5: Four general thin-film transistor configurations, including: (a) staggered bottom-gate, (b) coplanar bottom-gate, (c) staggered top-gate and (d) coplanar top-gate.

Additionally, the channel in the TFT can be either patterned or unpatterned, as shown in Figure 4.6. When the channel is patterned (Figure 4.6a) the width-to-length ratio is well defined. On the other hand when an unpatterned channel is used, peripheral current flows due to fringing electric fields outside the drawn channel. This effect can be observed in Figure 4.6b. For unpatterned channel devices, in addition to the current limited into the drain/source area, the fringing current also contributes to the total current, increasing the current when compared to the patterned channel device (JAGADISH et al., 2006).

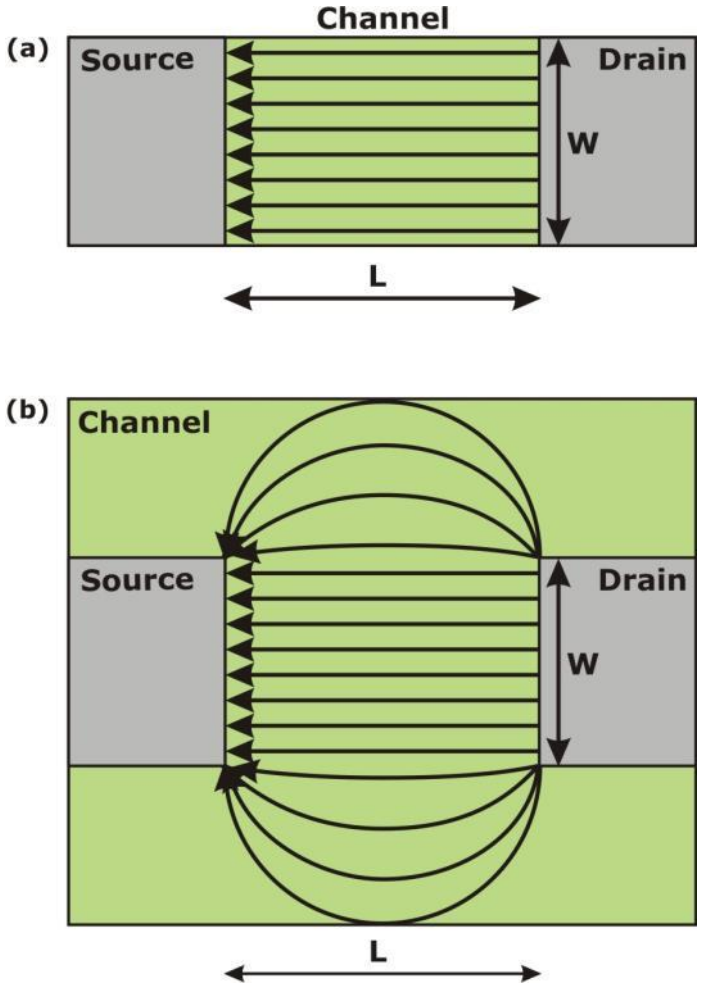


Figure 4.6: Schematic layout of a TFT structure (gate electrode and gate dielectric layers are not shown explicitly here), in which (a) the channel layer is patterned, and (b) the channel layer is unpatterned. The current is represented by arrows.

4.2 ZnO Thin-Film Transistor

In this subsection, it will be presented the evolution of the TFT in our group (a cooperation between University of Paderborn, Germany and UFRGS, Brazil), first using silicon nanoparticles and afterwards using ZnO nanoparticles. ZnO based TFT from other research groups will also be presented.

4.2.1 TFT in our group

The Sensor Technology Department from Paderborn, Germany has been working since 2005 with TFT, as part of an intensive cooperation with the industrial segments for both thin-film transistors as well as so-called single-particle transistors. The aim of the research is to develop a suitable manufacturing process for electronic logic circuits on foil substrates, where transistors with proper switching behavior should be suitable for low-cost/low-performance (low power) applications (SENSORIK, 2012). In 2010 the University of Paderborn and UFRGS started a collaborative work aiming to improve

the devices and exchange knowledge in their expertise areas. The following transistor evolution with a more detailed integration process and explanation is reported in (HILLERINGMANN et al., 2011).

The group started the research using silicon nanoparticles as active semiconductor. For simplicity, thermally oxidized doped silicon wafers were used as gate structure for the first tests of the transistors, as shown in Figure 4.7, although this technique is not suitable for circuit integration.

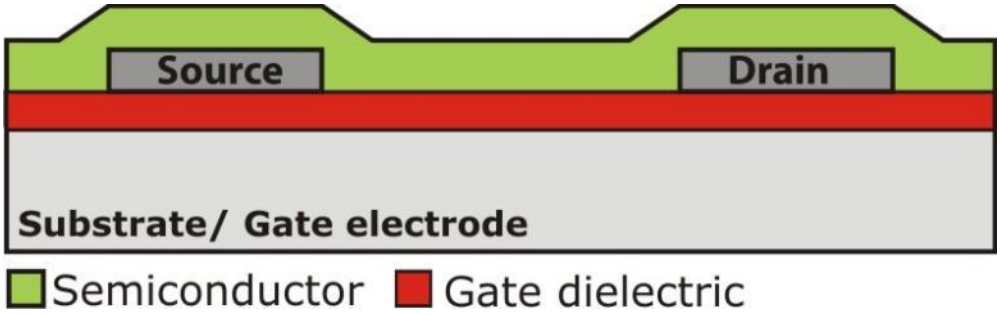


Figure 4.7: Integrated TFT using oxidized doped silicon as gate structure. Adapted from (HILLERINGMANN et al., 2011)

The transfer characteristic of the device with $L = 8\,\mu m$ and $W = 16.000\,\mu m$ is shown in Figure 4.8. Even at very high gate and drain voltages the drain current is in the nanoampere range only.

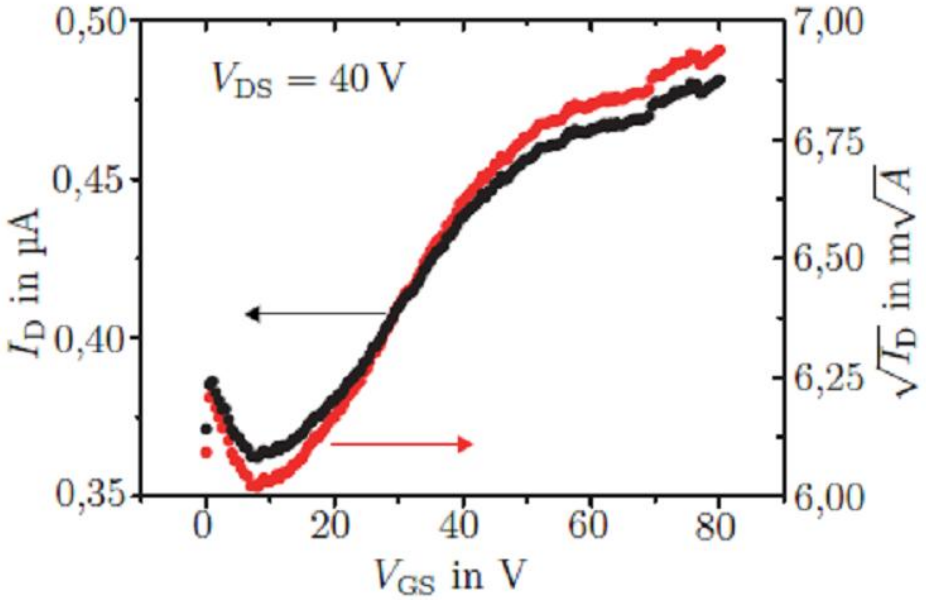


Figure 4.8: Transfer characteristics of the silicon nanoparticle transistor with $t_{ox} = 200\,nm$, $L = 8\,\mu m$ and $W = 16.000\,\mu m$. (HILLERINGMANN et al., 2011)

The natural oxide on the surface of the silicon nanoparticles is the main reason for the low drain current, as this oxide acts as a potential barrier. The mean particle size of the silicon nanoparticle is around 60 nm and considering the channel length of 16 μm,

there are at minimum 260 inter particle transitions in the channel. Considering that each transition acts as a potential barrier, the drain current is expected to be very small. The calculated field-effect mobility is about $10^{-7} cm^2/Vs$ only. Thereafter this kind of device is not suitable for any application.

In order to reduce the number of inter particle transitions, and therefore improve the mobility, it is necessary to reduce the transistor channel length. In the best case, only one particle should act as the transistor channel. By using a nanoscaled trench into the metal and inserting the semiconductor into this trench it is possible to integrate such device, as presented in Figure 4.9.

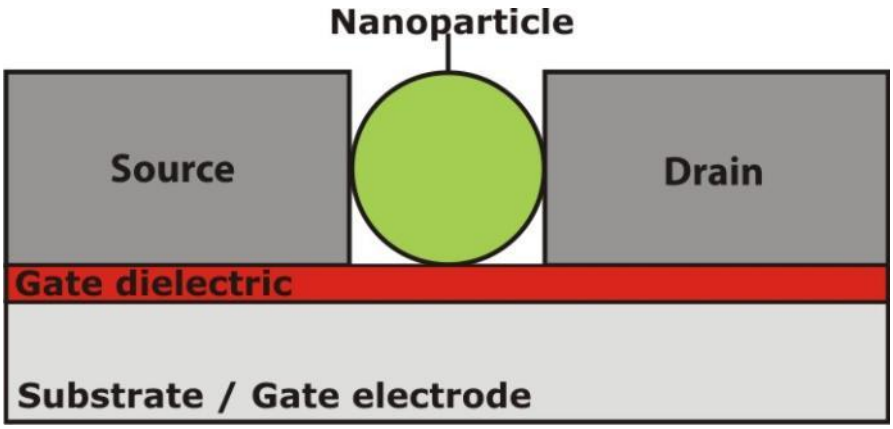


Figure 4.9: Schematic view of a silicon single particle FET with inverted coplanar setup. Adapted from (HILLERINGMANN et al., 2011)

To ensure the contact between both (drain/source) contacts, the trench must fit to the particle size, in other respects no contact will be formed. The test structure of $L = 60\ nm$ and $W = 100\ \mu m$ were used to get at least one particle out of the spin coating process (mean particle size of 60 nm in the dispersion). Figure 4.10 depicted the transfer curve of the integrated device. The p-type FET is a depletion device with a field-effect mobility of about $10^{-2} cm^2/Vs$, calculated assuming a completely filled transistor width with nanoparticle. As there are only few transistors operating, this assumption overestimates the real active transistor width, which means that there is a much higher mobility in the nanoparticle.

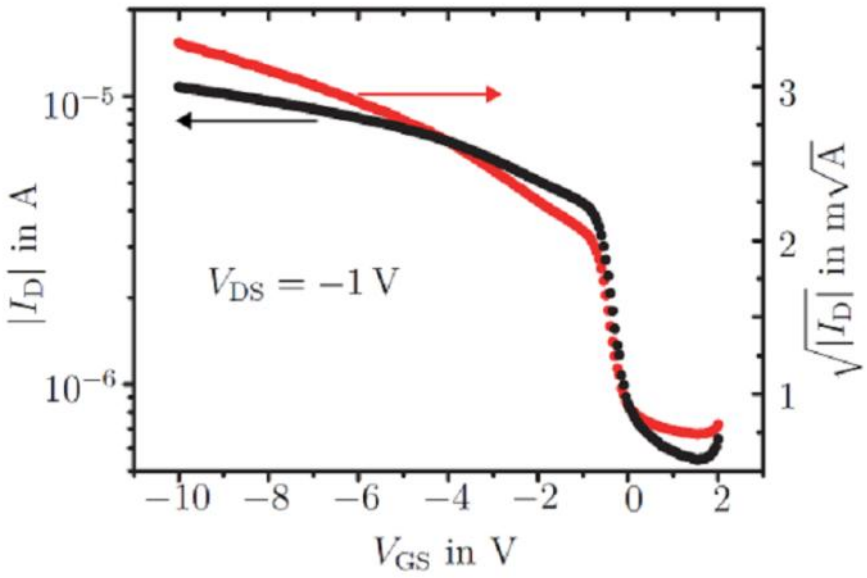


Figure 4.10: Transfer curve of a Si nanoparticle FET with L = 60 nm and W = 100 μm, t_{ox} = 15 nm after thermal treatment at 300°C. (HILLERINGMANN et al., 2011)

Since the yield of operating devices with the configuration above was very low, an inverted staggered configuration was integrated. Despite the higher yield in well operating devices, the performance improvement was not satisfactory. The silicon nanoparticles used in the above TFT are undoped; and phosphorous doping weakly influences the transistor characteristics, because the number of active dopants in a nanoparticle is very low; conversely, boron doping strongly affects the transistor because aluminium (metal used for the drain/source) and the p-type silicon built an ohmic contact. Therefore the potential barrier vanishes and the nanoparticles nearly electrically short-circuit the drain and source contacts.

Summing up, thin film transistors based in Si nanoparticles are not suitable for device integration mainly due to the natural oxide shell on the particle surface. Only by using a single particle as switch element the performance can be acceptable.

The natural oxide in the Si nanoparticles was the main reason for changing from silicon to zinc oxide nanoparticles. ZnO particles do not have any insulating shell caused by the atmosphere. An improvement in the particle interconnection was expected, since the potential barrier between neighboring particles should be lower than in silicon.

A water based dispersion of ZnO nanoparticles was used in the same template (inverted coplanar structure) as used for the Si nanoparticles based TFT. The transistor input and output curves are shown in Figure 4.11, where it is possible to observe an n-type enhancement mode FET. Field effect mobility of about $10^{-5} cm^2/Vs$ was extracted from the transfer characteristic.

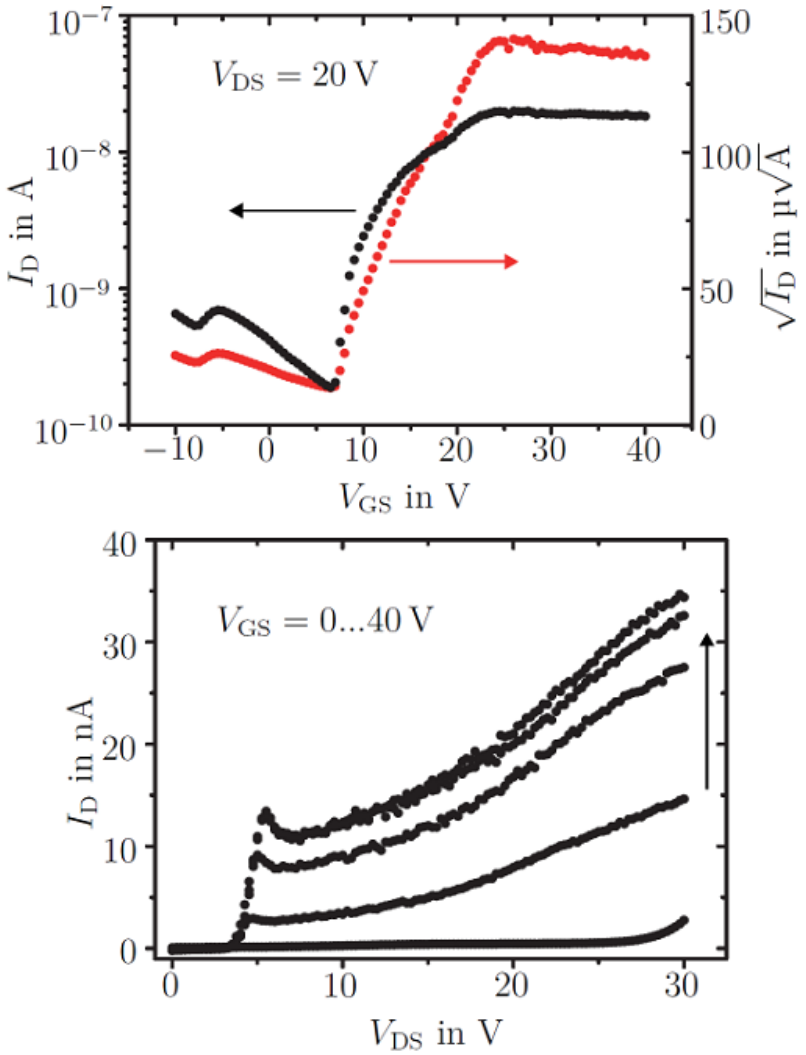


Figure 4.11: Characteristics of a thin film zinc oxide nanoparticle FET in inverted coplanar setup, $L = 8\,\mu m$, $W = 16.000\,\mu m$ and $t_{ox} = 300\,nm$. (HILLERINGMANN et al., 2011)

The main reason for the transistor low on-current is the contact resistance at the metal/nanoparticle contact, which can be improved by application of the inverted staggered setup. In order to enhance the adhesion in these transistors to photolithography steps, a thermal treatment was performed at 600ºC for 2 hours. The drain and source electrodes were deposited by evaporation of aluminium using a lift-off mask. Due to the resistance reduction at the metal/nanoparticle contact and the thermal treatment, the transistor presented much higher on-current, as depicted in Figure 4.12. The mobility is about $5.5\ 10^{-5} cm^2/Vs$ and a small hysteresis can be observed in the transfer curve. Moreover, the yield is high and these TFT may be qualified for low cost/low performance electronics.

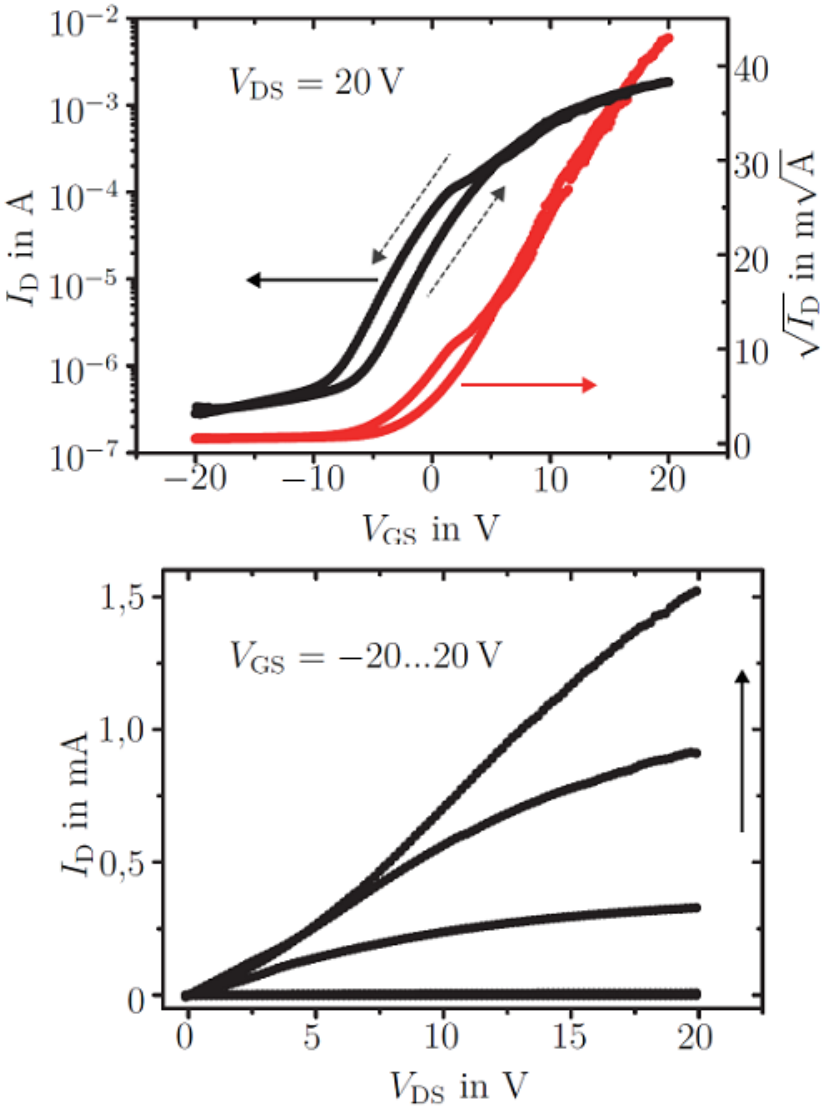


Figure 4.12: Characteristics of a thin film zinc oxide nanoparticle FET in inverted staggered setup, $L = 8\,\mu m$, $W = 16.000\,\mu m$ and $t_{ox} = 53\,nm$. (HILLERINGMANN et al., 2011)

Single nanoparticle zinc oxide transistors were also integrated to compare with the silicon based device. Since the drain and source electrodes must fit the particle size and it is difficult to get an active nanoparticle in the trench, the yield is very low. Nevertheless, using this configuration, it is possible to strongly reduce the applied voltage in this device. The transfer curve is depicted in Figure 4.13.

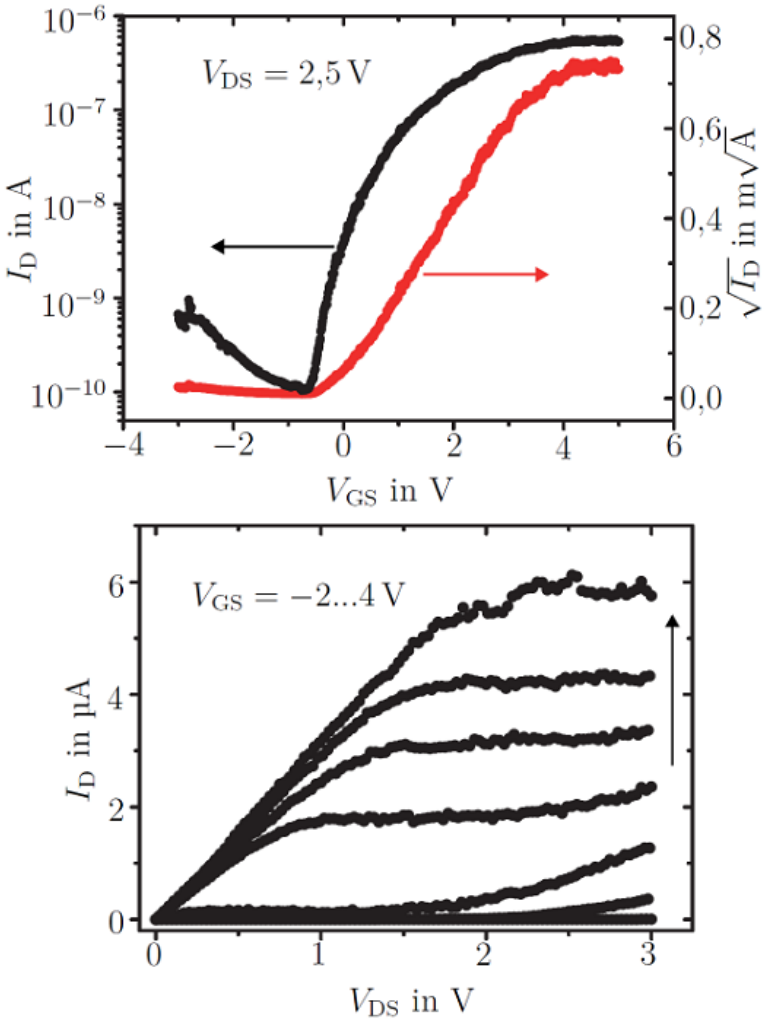


Figure 4.13: One particle zinc oxide FET in inverted coplanar setup, $L = 80\,nm$, $W = 100\,\mu m$ (metal structure), $t_{ox} = 31\,nm$. (HILLERINGMANN et al., 2011)

For circuit integration, the test structure applying the silicon substrate as the gate electrode is not suitable. For this reason, an aluminium gate electrode was evaporated and structured on top of a glass substrate. For the gate dielectric cross-linked PVP was used, and an inverted staggered setup was used as the TFT structure. For these transistors, the maximum integration process temperature was of 200ºC, which enables the process to some plastic substrates.

The transfer characteristic depicted in Figure 4.14 shows a considerable hysteresis when sweeping the gate voltage forwards and backwards. Moreover, when the transistor is heated up the hysteresis is inverted, i.e., during the incrementation of the gate voltage the threshold voltage is lower than during the decrementation. This behavior and the origin of the hysteresis will be investigated in this work.

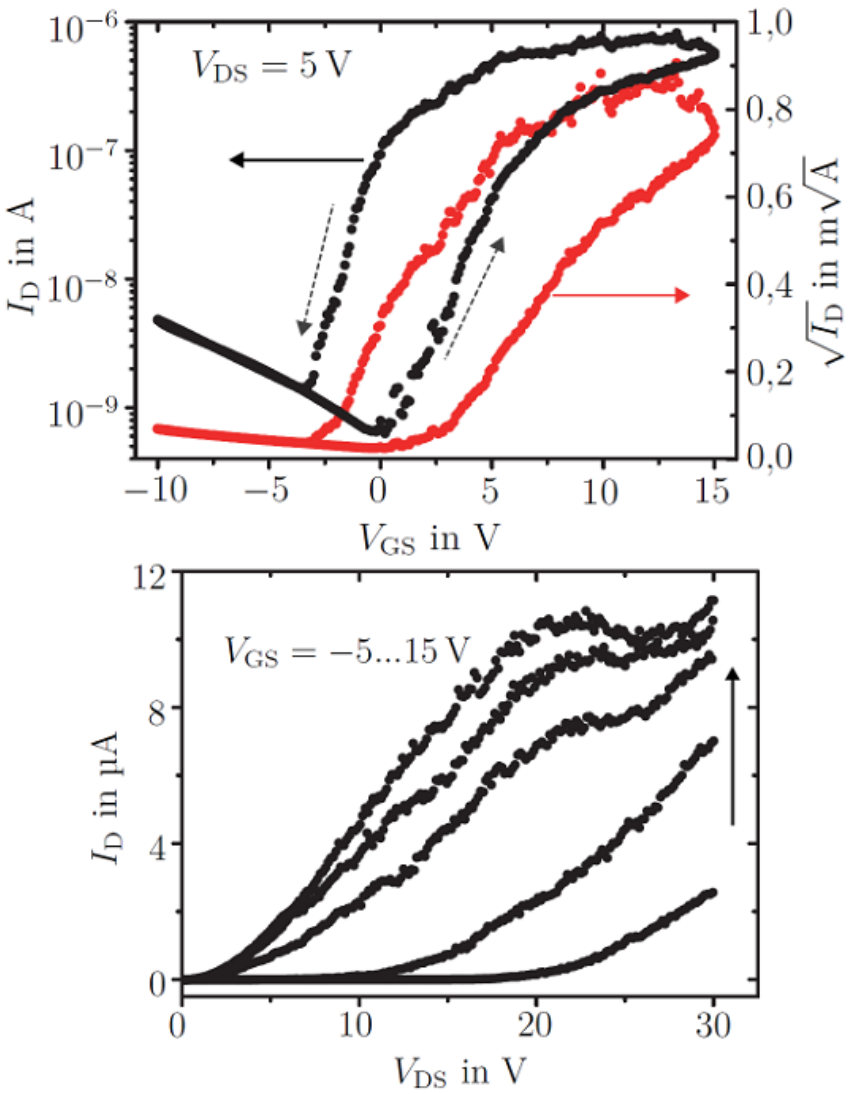


Figure 4.14: Characteristics of the zinc oxide nanoparticle film transistor integrated on glass, $L = 3\ \mu m$, $W = 1000\ \mu m$, $t_{ins} = 180\ nm$. (HILLERINGMANN et al., 2011)

Although the threshold voltage is not constant, the device integrated with a maximum thermal treatment of 200ºC has acceptable parameter with field effect mobility of about 0.07 cm^2/Vs and on/off-ratio of 10^5. This allowed the fabrication of a simple inverter consisting of a load transistor and a switch device, integrated on oxidized silicon wafer. Figure 4.15 shows a sketch and a light microscope photograph of the inverter.

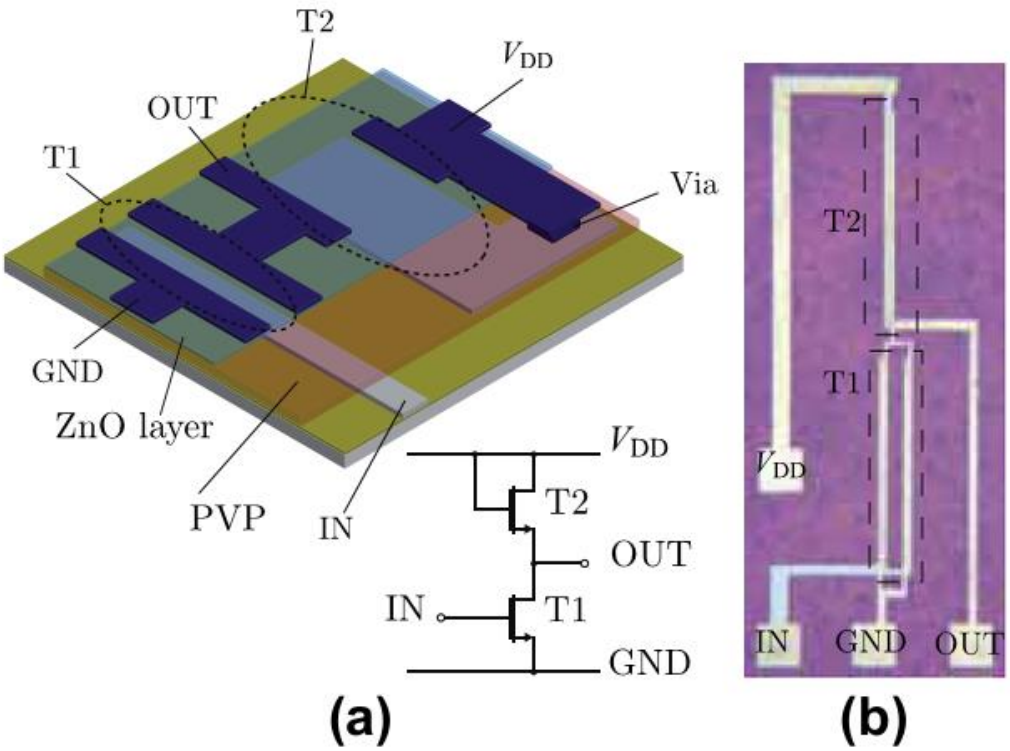


Figure 4.15: (a) 3D-graph, schematic and (b) optical micrograph of the presented inverter circuit. (WOLFF et al., 2011-b)

The transfer characteristic of the inverter and the power consumption are depicted in Figure 4.16. It is possible to observe that the non constant threshold voltage in the ZnO device has influence in the inverter parameters. It is clear that the inverter characteristic is far from the ideal. However, it demonstrates that zinc oxide nanoparticles have potential for integrating digital circuits.

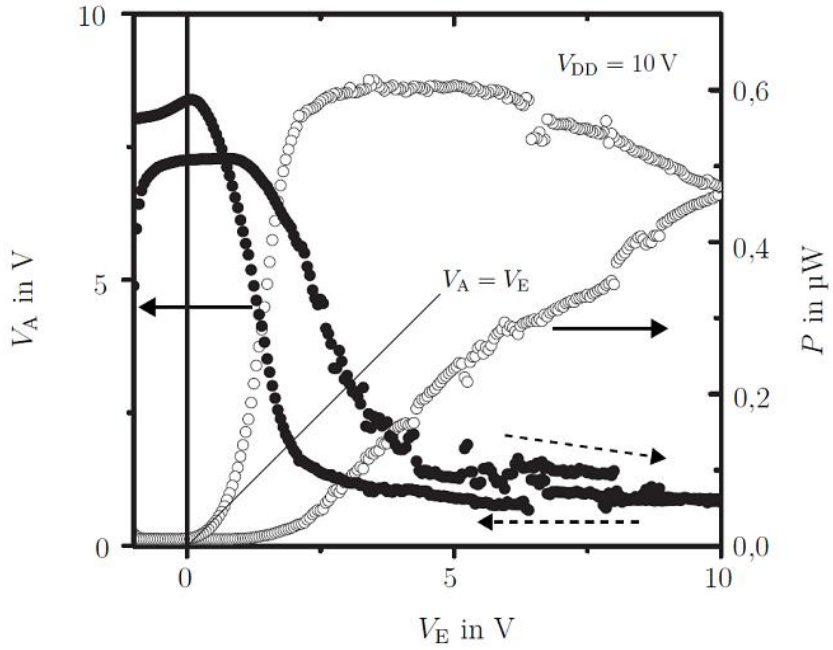


Figure 4.16: Transfer characteristic and power consumption of the zinc oxide nanoparticle inverter integrated on oxidized silicon substrates. V_E denotes the input voltage and V_A the output voltage. (WOLFF et al., 2011-b)

The author also contributed previously to ZnO nanoparticle TFT improvement. The performance was enhanced by the addition of liquid zinc acetate to get an electrical link between the nanoparticles in the semiconductor film as described in (VIDOR et al., 2011-b). In Figure 4.17, the transfer characteristics of both devices, with and without the deposition of the zinc salt, are presented in order to allow easy comparison. It is possible to observe that by applying a hydrothermal decomposition of a zinc salt the current increases and that the hysteresis almost vanishes.

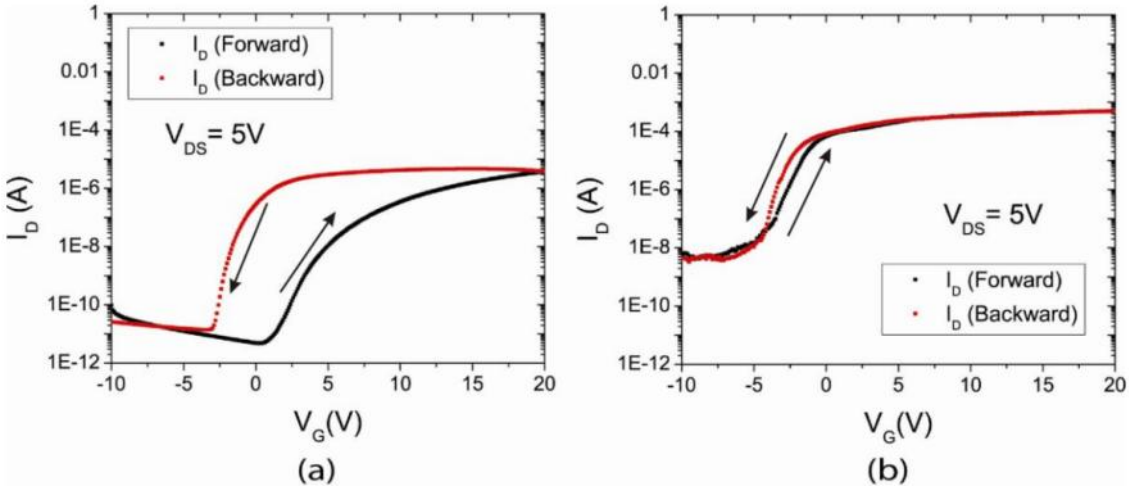


Figure 4.17: Transfer characteristics of (a) ZnO nanoparticle TFT with Al-S/D-contact (b) ZnO nanoparticle with zinc acetate TFT and Al-S/D-contact.

The performance enhancement and the significant reduction of the hysteresis were attributed to positive ions from the zinc acetate, which work as an electric shield over the traps. This mechanism was assumed to be the origin of the observed behavior, since it was the "forward" threshold voltage that was substantially shifted down. After two weeks, the transistors were once again characterized and it was verified that the electric shielding achieved by the addition of the zinc acetate was no longer affecting the device, leading to a hysteretic behavior similar to the one observed in non-treated transistors.

More detailed information about the author previous work can be found in (VIDOR et al., 2011-a) and (VIDOR et al., 2011-b), as well as the group previous work (HILLERINGMANN et al., 2011), (WOLFF et al., 2010), (WOLFF et al., 2011-a,b,c), (ASSION et al., 2011) and (SENSORIK, 2012).

4.2.2 ZnO TFT by other research groups.

Zinc oxide thin-film transistors are the focus of research of several groups (LEE et al., 2006), (BUBEL et al., 2009), (HOFFMAN et al., 2003), (FABER et al., 2009), (OKAMURA et al., 2008), (WOLFF et al., 2011-b), (BASHIR et al., 2009), (GRUPTA et al., 2011), (JUN et al., 2009), (FORTUNATO et al., 2004) and others. In this section, the research of other groups, as well as their devices, is briefly discussed to provide basis for comparison; additionally, the reader may get more familiar with ZnO based TFT.

Normally, ZnO FETs have been fabricated not only by epitaxial (NISHII et al., 2005) and sputtering techniques (HOFFMAN et al., 2003) (CARCIA et al., 2006), but also by solution processes, such as chemical bath deposition, (CHENG et al., 2006) (LI et al., 2007) spin-coating precursor followed by post-annealing, (NORRIS et al., 2003) (ONG et al., 2007) and spin-coating nanocrystals (nanoparticles) (SUN et al. 2005) (JUN et al., 2009) (WOLFF et al., 2010).

Among these integration processes, chemical bath deposition and the spin-coating of precursors followed by post-annealing require a long time and high temperature process, respectively. Therefore they are not suitable for fabricating low-cost TFTs on plastic substrates. The advantage of spin-coating nanocrystals is that the two main processes, nanoparticle synthesis and film formation, are essentially independent. That is, even if the nanoparticles are synthesized using high-temperature, high-pressure, chemical or gas-phase processes for the optimization of the particles, they can be used for fabricating TFTs on flexible substrates as long as the films made are formed using low-temperature and high throughput processes (OKAMURA et al., 2008) (JUN et al., 2009).

Hoffman et al. (2003) has demonstrated a fully functional transparent ZnO TFT. The integrated device structure is presented in Figure 4.18, in which it is possible to observe the main components of the TFT. The channel width and length are $15000\ \mu m$ and $1500\ \mu m$, respectively. The ZnO channel layer was deposited via ion beam sputtering in an argon and oxygen atmosphere; the substrate is unheated during the deposition and shadow mask was used to pattern the TFT channel. Then a rapid thermal annealing was performed at 600-800°C in O_2 atmosphere to improve the electrical quality of the semiconductor/gate dielectric interface and to enhance the crystallinity of the ZnO

layer. The optical transmission spectra through the source/drain region and the channel region of the TFT is depicted in Figure 4.19.

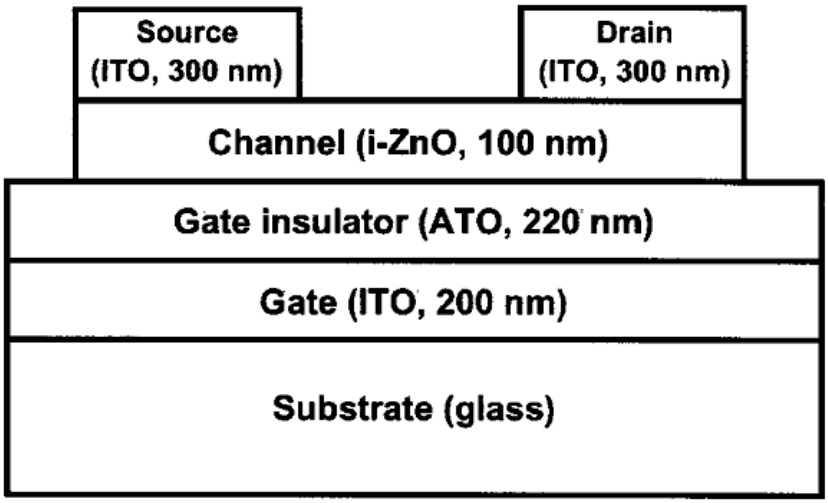


Figure 4.18: Transparent ZnO based TFT integrated by Hoffman et al. (2003). ITO denotes indium tin oxide and ATO antimony tin oxide.

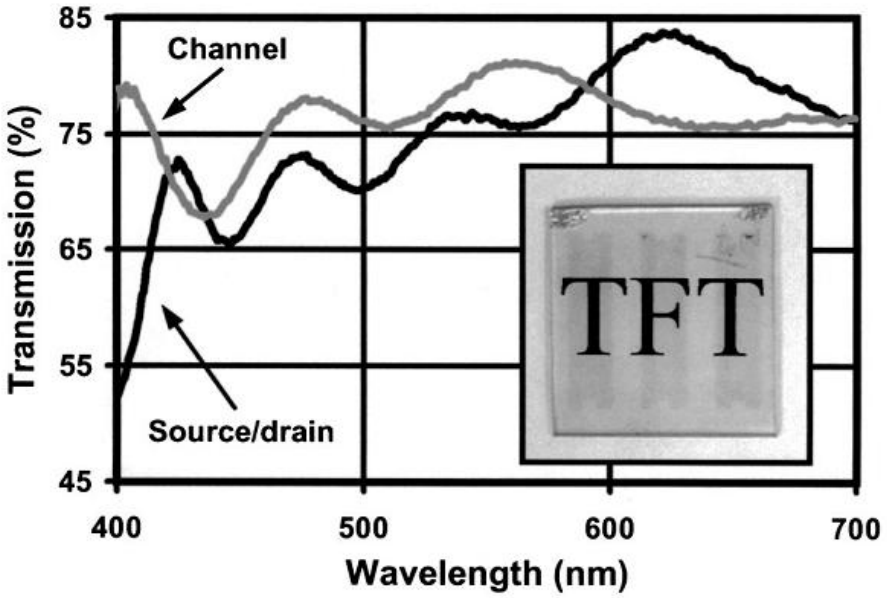


Figure 4.19: The optical transmission spectra for the entire transparent TFT structure, including the substrate. (HOFFMAN et al., 2003)

The mobility and the threshold voltage were found to be $0.35 - 0.45 cm^2/Vs$ and 10-15V, respectively and no hysteretic behavior was mentioned (HOFFMAN et al., 2003).

As discussed above, generally, thin-film transistors have been fabricated by deposition methods such as ion beam sputtering and pulsed laser deposition. Fortunato et al (2004) fabricated a ZnO thin-film transistor at room temperature by RF magnetron

sputtering and mobility of 70 cm^2/Vs was extracted, indicating that there is room for improvement in the performance of the device.

Fortunato (2004) reported results of integration and characterization of a high field-effect mobility ZnO TFT, whose gate dielectric is made of a silicon oxynitride compound and source/drain regions of a highly conductive gallium doped zinc oxide (GZO). The schematic device structure is presented in Figure 4.20.

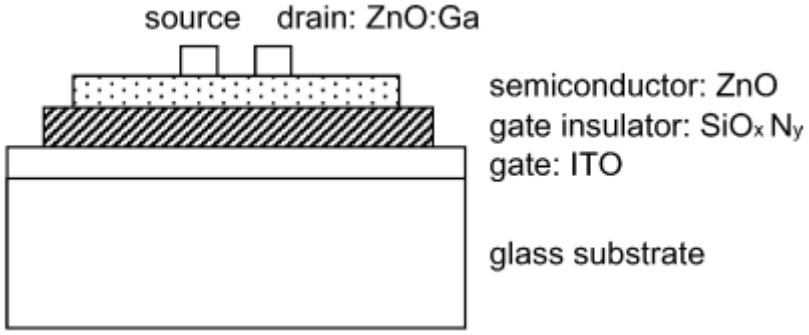


Figure 4.20: High performance ZnO TFT integrated by Fortunato et al (2004).

The fully functional transparent transistor fabricated by Fortunato et al. (2004) can be observed in Figure 4.21 (transfer characteristic and gate current leakage). Also it is possible to observe the optical transmission spectra for the entire ZnO TFT.

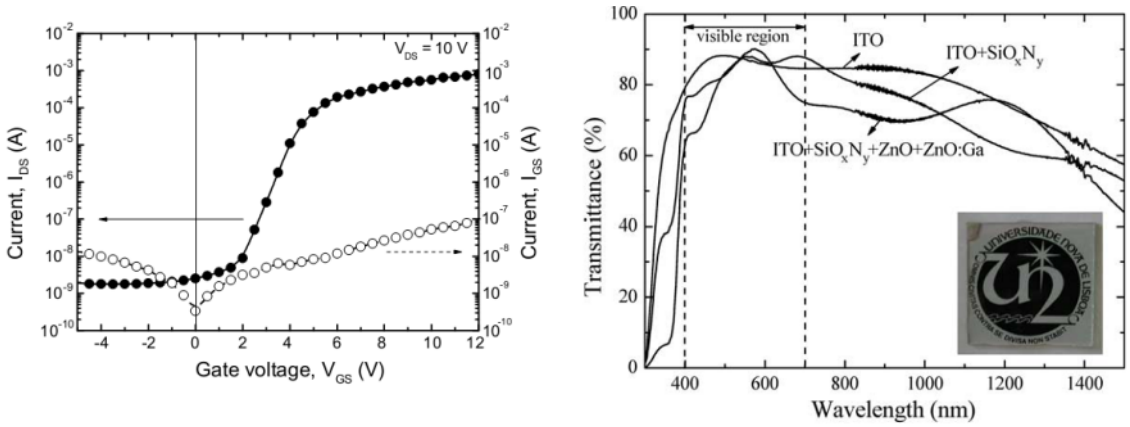


Figure 4.21: Transfer characteristic and gate leakage for ZnO TFT ($W/L = 5$) and optical transmission spectra of the entire ZnO TFT with its photograph on the corner. (FORTUNATO et al., 2004)

On the other hand, by using nanoparticulate ZnO, it is possible to directly process the semiconductor from a liquid dispersion without the necessity of a costly or high temperature process (BUBEL et al., 2009). Volkman et al. (2004) presented an air-stable (in comparison to organics candidates), printable, transparent TFT using nanoparticulate ZnO. In his work, nanoparticles were synthesized by reacting zinc acetate with sodium hydroxide (NaOH) in 2-propanol. By controlling the formation reaction, the resulting nanoparticles consist of about 3 nm of diameter. Silicon dioxide was used as gate dielectric and gold was used for source and drain electrodes. The transistor characteristics were strongly affected by the fabrication process of the nanoparticles, and an annealing step at 400ºC was necessary. Due to this annealing step,

such process is not suitable to some plastic substrates. The on-off ratio is greater than 10^3 and the field-effect mobility is typically in the range of $0.1 - 0.2\ cm^2/Vs$.

Although the ZnO nanoparticles present good prospective and can be produced at low cost and high quality, some problems using the nanoparticles to integrate TFT can be observed, as discussed below.

One of the issues regarding the use of ZnO nanoparticles for integrating TFT is the hysteretic behavior when using poly (4-vinylphenol) (PVP) (FABER et al., 2009), (WOLFF et al., 2011-b) and (LEE et al., 2006) or SiO_2 (LEE et al., 2007), (SUN et al., 2005) and (ASSION et al., 2011) as gate dielectric.

Faber et al. (2009) used the presence of the hysteresis in the transfer characteristic to propose the use of ZnO nanoparticle TFT as memory device. In Figure 4.22, the schematic cross-section of the TFT is depicted.

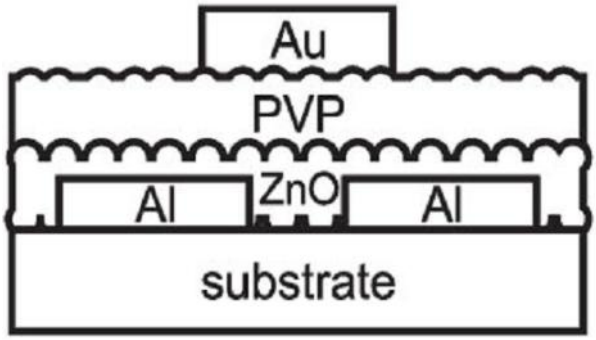


Figure 4.22: Schematic cross-section of the ZnO nanoparticle TFT integrated by Faber et al. (2009).

It is possible to observe in Figure 4.23 the proposed qualitative model to the origin of the hysteresis and its application as memory device. At the beginning, the traps over the ZnO and PVP interfaces are empty, as well as the associated carrier accumulation in the nanoparticles (Figure 4.23a). With the rise of the gate voltage, positive charges, possibly from the PVP (perhaps mobiles ions), are trapped in the interface. The same occurs with the carriers in the nanoparticles (Figure 4.23b). When the gate voltage is large enough, the interface is positively charged and the nanoparticulate ZnO film is filled (Figure 4.23c). However, sweeping the gate voltage backwards, the trapped charges in the interface continue accumulating a carrier channel in the nanoparticles (Figure 4.23d). In order to release these traps, a lower gate voltage is required, which leads to a downshift of the threshold voltage and the creation of the observed hysteresis (FABER et al., 2009).

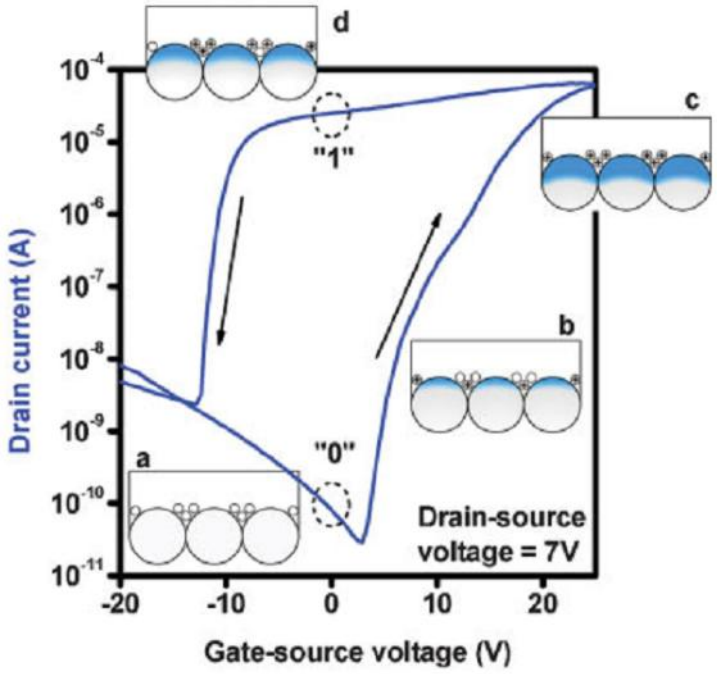


Figure 4.23: Transfer characteristic of a ZnO nanoparticle TFT with representative trapping mechanism. (FABER et al., 2009)

When using SiO_2 as gate dielectric, Nandi et al. (2003) attributes the hysteretic behavior to traps at the SiO_2 interface with the ZnO layer. In Nandi et al. (2003) work, the interface quality of low temperature (< 200ºC) plasma enhanced chemical vapor deposition (PECVD) SiO_2 and ZnO were investigated.

The influence of the interface roughness on the performance of the nanoparticulate zinc oxide TFT was studied by Okamura et al. (2008). Since nanoparticulate films are composed of nanoparticles and their agglomerates, the roughness of the interface to the insulating layer, in which the channel of the TFT is formed, is a critical issue.

To evaluate the interface roughness, Okamura et al. (2008) integrated both ZnO TFT and capacitors using different particles sizes (diameter around 10 to 20 nm). Silicon dioxide was used as gate dielectric and aluminium as contacts. As shown in Figure 4.24, the interface roughness prevents accumulated carriers from transporting along the channel if the interface roughness is comparable to or greater than the thickness of the accumulation layer induced by the gate voltage (OKAMURA et al., 2008). Small agglomerates results in a smoother interface and higher mobility, and large agglomerates results in a rougher interface and lower mobility.

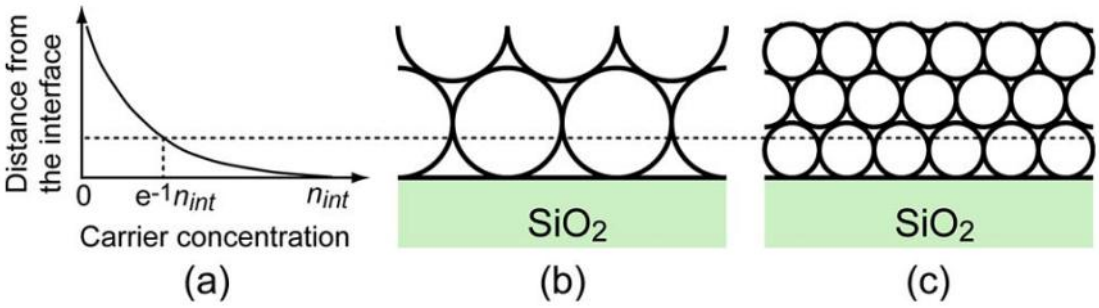


Figure 4.24: Magnified schematics at the interface of nanoparticulate FETs, under the condition of the carrier accumulation. (a) The carrier concentration depending on the distance from the interface in FETs. n_{int} denotes the carrier concentration at the interface. (b) A rough interface with big agglomerates results in low mobility. (c) A smooth interface with small agglomerates leads to high mobility. (OKAMURA et al., 2008).

Moreover, Wolff and Hilleringmann (2010) also reported a degradation of the charge mobility, caused by the accumulation of charges in the nanoparticles at the gate dielectric interface. When $V_{GS} > 0$ (channel charges are accumulated) and the electric field becomes so strong that the Debeye length is smaller than the nanoparticle radius, a great amount of channel charges are trapped and therefore unavailable for the lateral drain current, resulting in a decrease of the mobility.

Lee et al. (2007, 2008) fabricated a solution-processed ZnO thin-film transistor using nanoparticles. He states that in order to form a continuous pathway for charge carrier transport, the particles should be interconnected through annealing process. He reported (Lee et al., 2007) that the particles remained intact below 400ºC, while interparticle sintering began at around 400ºC. The use of nanoparticles of large diameter, ranging from 24 to 114 nm as presented in Lee et al. (2008) work, required a higher annealing temperature (around 600ºC) than that reported by Sun et al (2005) when using spherical ZnO of diameter of about 6 nm or the rod-like ZnO of major axis of about 65 nm (around 230ºC).

It was also reported that the microstructure of the channel plays an important role in determining the performance of the device (LEE et al. 2008). Using different particle morphology, results in a distinct channel grain structure, which significantly influences the number of intergranular hopping steps for electrons moving from the source to the drain electrodes. Using nanorods, the number of electron hopping steps to cross the channel is smaller in comparison to when ZnO nanospheres are used (LEE et al., 2008). This result is in agreement with the results found by Sun et al. (2005). He states that the mobility increases (compared to nanospheres) even when the nanorods are not uniaxially aligned to the direction of the current flow. Conversely, in his work the nanorods are partially aligned because of its self-organization. Nevertheless, an important performance improvement is believed to be related with the alignment of the nanorods (SUN et al., 2005).

Another relevant behavior reported by Sun et al. (2005) is the presence of a hysteretic behavior when the transistor is electrically characterized. The hysteresis is

observed using either nanorods or nanospheres ZnO compounds. Silicon dioxide and gold were used as gate dielectric and drain/source contacts, respectively.

Other groups already reported hysteresis in Zno based thin-film transistors (VERBAKEL et al., 2006), (WANG et al., 2010), (THEISSMANN et al., 2011), (MEYERS et al., 2008), (LEE et al., 2006) and (NOH et al., 2007) or when PVP is used as gate dielectric in organic transistors (BENSON et al., 2008), (HWANG et al., 2006), (JUNG et al., 2005) and (LIM et al., 2007). A more detailed discussion of hysteresis and its explanations are presented in Section 5, when a qualitative model for the hysteresis is proposed together with the results of the integrated devices in this work.

Jun et al. (2009) integrated flexible TFTs on a plastic (PES - Polyethersulfone) substrate based on a solution-processed ZnO nanoparticles. The channel layer was formed by spin-coating process and Al_2O_3 (aluminium oxide), deposited by atomic layer deposition method (ALD), was used as gate dielectric. In Figure 4.25 the schematic cross section of the TFT integrated by Jun et al. (2009) is presented beside an optical image of the TFT.

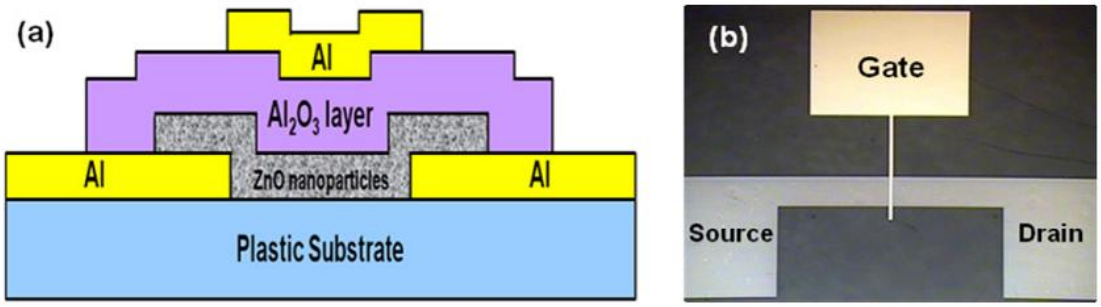


Figure 4.25: (a) Cross-sectional schematic of a top-gate ZnO TFT and (b) an optical image of the fabricated TFT. (JUN et al., 2009)

As reported by Jun et al. (2009), it was the first attempt to fabricate a fully functional ZnO TFT on flexible substrate through solution process. The TFT displays an n-channel device characteristic and operated in enhancement mode (Threshold voltage of 7.2 V). In the flat state, the device presented a very low field-effect mobility of $1.2\ 10^{-5}\ cm^2/Vs$ and I_{on}/I_{off} ratio as high as $1.5\ 10^3$. Figure 4.26 depicts the output and input characteristics of the transistor.

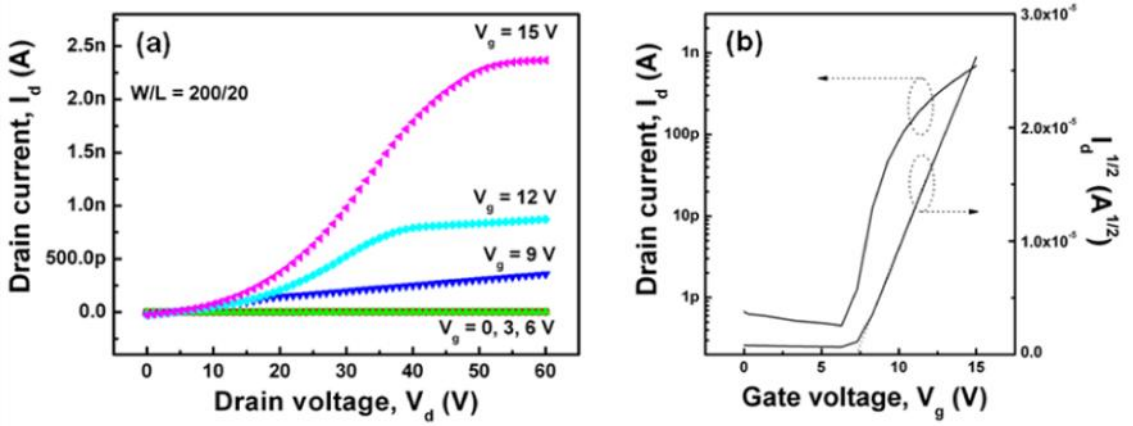


Figure 4.26: (a) Output and (b) transfer characteristics of the fabricated TFT with a channel layer composed of solution-processed ZnO nanoparticles in the flat state. (JUN et al., 2009)

When the TFT was in the bent state (upward or downward), some of the device parameters changed. When the TFT is in the upward state, the mobility and the I_{on}/I_{off} ratio decrease. When the TFT is in the downward state, the mobility and the on-current increase compared to the values in the flat state and the I_{on}/I_{off} ratio decreased. These variations are attributed to the structure of the active semiconductor in the device. Since the channel is composed of nanoparticles instead of a continuous film, the stress due to the strain does not affect the individual particle, however affects the network composed by them. It means that the mechanical stress is released through the deformation of the nanoparticle network, increasing and decreasing the physical distance between the particles (JUN et al., 2009). The threshold voltage remains unchanged in either upward or downward state, because the strain caused by the substrate bending does not change the carrier concentration in the device (JUN et al., 2009).

Also, Jun et al. (2009) reported that the device performance was restored when the TFT returned to the flat state. However, the devices failed after several cycles of bending tests. This may be caused by network destruction leading to the cracking or peeling of the nanoparticle layer during the bending tests.

4.2.3 Transport of current in nanoparticulate ZnO

It is well-known that when using nanoparticulate ZnO as active semiconductor channel in TFT the particles create networks for the electrons transport. It was discussed that the annealing can improve the particles interconnection (LEE et al., 2007) and that bending can affect the physical distance between the nanoparticles (JUN el at., 2009).

A more detailed study was done by Meulenkamp (1999), in which the electron transport in nanoparticulate ZnO films is discussed. A transistor-like electrode geometry was used to investigate the transport, as depicted in Figure 4.27.

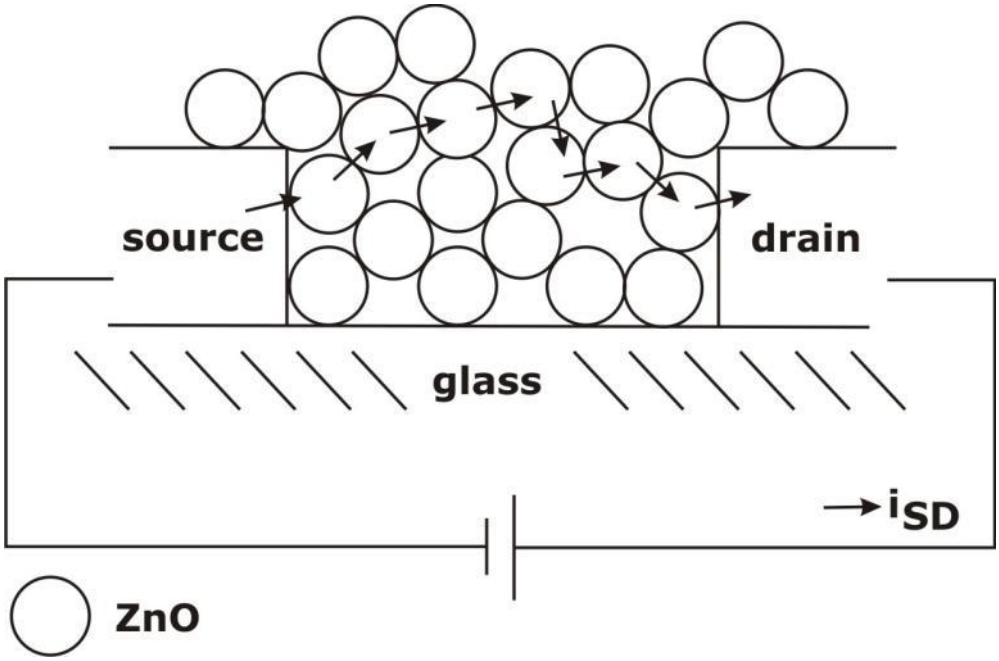


Figure 4.27: Schematic picture of the electrode geometry used to investigate the transport in ZnO nanoparticles. Adapted from (MEULENKAMP, 2009)

Meulenkamp (2009) states that the transport of electrons in nanoparticulate ZnO is not an intrinsic property of an individual crystalline nanoparticle, but a property of the film with its particular microstructure. Hence, it is possible to say that, in some cases, the particle diameter is smaller than the electron mean free path in bulk ZnO. Another secondary effect has to do with the energy barrier between particles, which is sensitive to the preparation conditions and the surface chemistry.

The nanoparticle film can be viewed as a resistor network, with resistors describing interparticle electron transfer. In this situation, the current flow in nanoparticulate ZnO is based on percolation paths (MEULENKAMP, 2009). The film porosity and heterogeneity also have a strong impact on the electron transport as they determine what part of the ZnO particles contributes to the conductivity, as well as the contact area between neighbors.

Because of the characteristic in the electron transport in ZnO nanoparticle films, in which there may be a preferable current path in the film combined with high density of traps, it can be expected that phenomena seen in nanoscaled MOSFET may also be observed. Examples of these phenomena are the random telegraph signal (RTS) or negative bias temperature instability (NBTI).

With the gradual downscaling of the FET devices, shrinking the device dimensions to atomic levels, variation between devices appear due to effects such as random dopant fluctuation and line edge roughness (KACZER et al., 2010). Figure 4.28 depicts an energy diagram of a MOSFET. The non-uniformity is due to random dopant fluctuations (RDF). This results in the formation of conduction (percolation) path for the electron transport from source to drain electrodes.

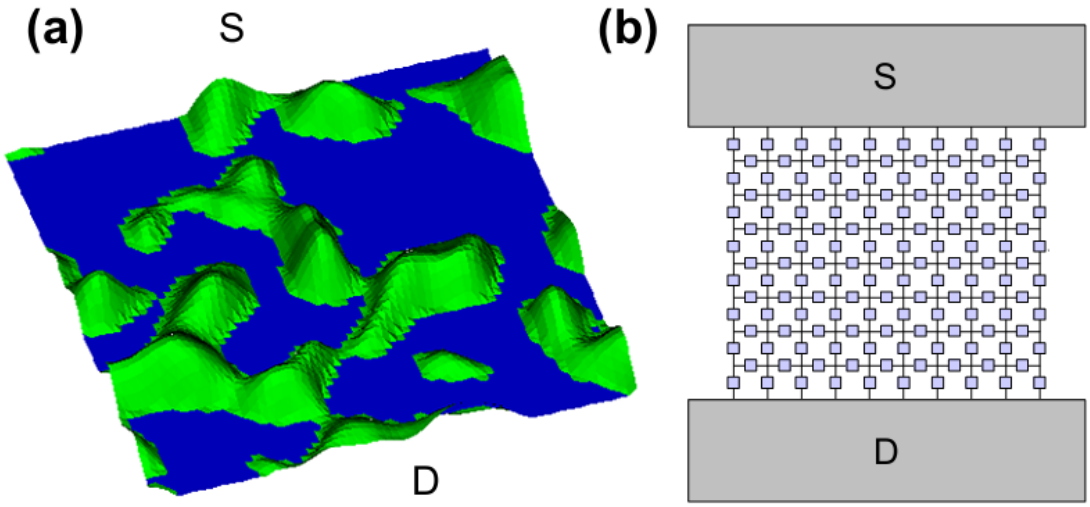


Figure 4.28: (a) An illustration of a percolation path as result of random dopant fluctuation and (b) a resistor network representing the conduction in the transistor. (KACZER et al., 2010)

Charging and discharging of individual defects or trap in a determined current path electrostatically affects the transistors and, consequently, its current. Silva et al. (2006) reported the effect of a single interface trap with alternating behavior (captures and emissions), which produced a discrete noise in the transistor current, as depicted in Figure 4.29. When the electron is trapped the current is decreased, whereas when the electron is released the current is increased, creating the observed steplike change in the current (SILVA et al., 2006), (MUELLER et al., 1998), (LEE et al., 2009).

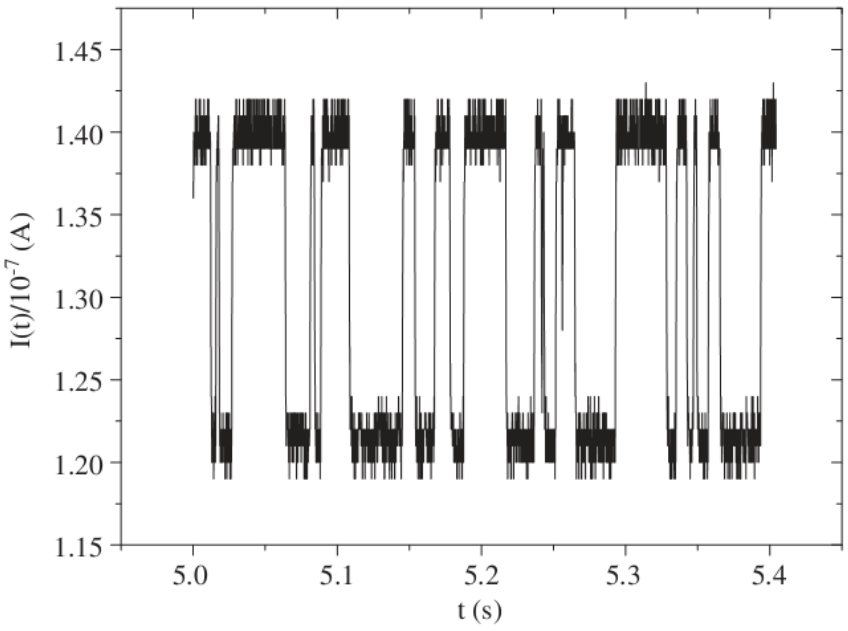


Figure 4.29: Discrete current fluctuations correspond to capture and emission of an electron by a particular trap. (SILVA et al., 2006)

In a non-uniform channel, as in percolation paths, different traps located at different channel positions impacts differently the transistor current (MUELLER et al., 1998). In Figure 4.30, two traps located at different sites are demonstrated together with the density of current in the channel. The trap located in A causes a higher amplitude variation in the transistor current compared to the traps located in B.

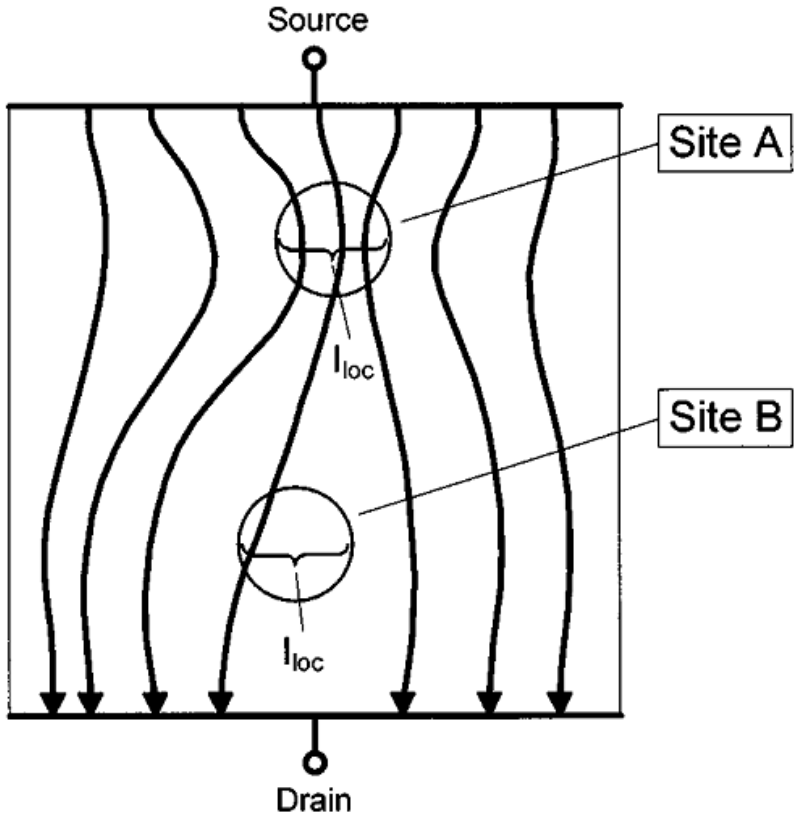


Figure 4.30: Schematic drawing of the current flow lines in a non-uniform channel. A trap switching at location A will cause a larger RTS amplitude than the one at location B. I_{loc} denotes local current. (MUELLER et al., 1998)

A similar effect was observed in the ZnO nanoparticle transistors integrated in this work as it will be discussed below in Section 5.

4.3 Transistor Integration Using Polymeric Gate Dielectric

In this subsection, the integration procedure for the ZnO nanoparticle TFT in which cross-linked PVP was used as gate dielectric layer is presented. Figure 4.31 represents the schematic cross-section of the transistor, and a bottom-gate/top-drain/source transistor is observed. This design shows a better performance than a top-gate/bottom-drain/source transistor, as reported by Konopka (2010). For this reason the structure presented in Figure 4.31 was picked. Connections between the gate and the source/drain metal layer, in this geometry, are only possible via connections through the gate insulator and the semiconductor.

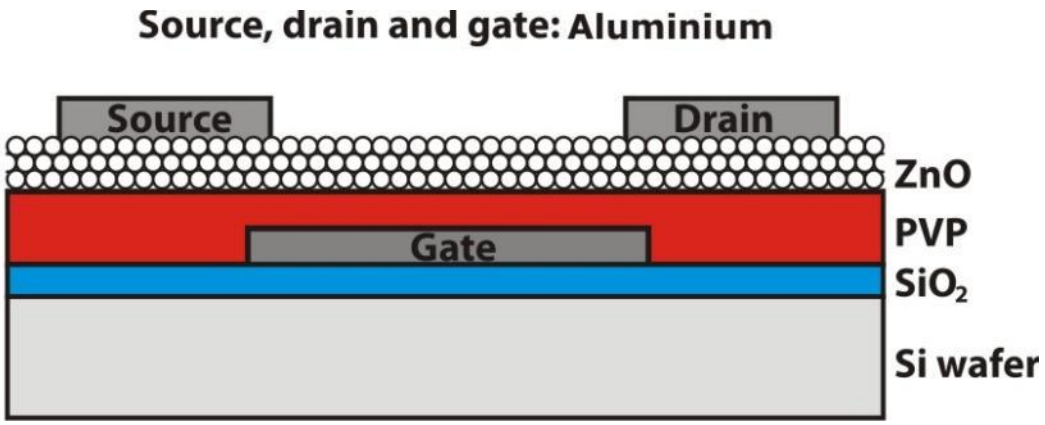


Figure 4.31: Schematic cross-section of ZnO nanoparticle TFT with PVP as gate dielectric.

Important aspects on the transistor integration process are the PVP as gate dielectric and the ZnO nanoparticle layer as the active semiconductor. Also, aluminium was used to integrate the drain, source and gate electrodes and the interconnections. The channel width is 500 µm and 1000 µm, and the channel length varies from 1 µm to 3 µm in the analyzed transistors. The fringing current due to the non patterned channel region will be negligible as consequence of the long channels used.

4.3.1 Wafer Preparation

The transistors were integrated over a standard 4-inch silicon wafer either p-type or n-type and crystal orientation of any type, as the wafer is just used for mechanical support and a thick layer of silicon oxide was grown to insulate the bulk silicon from the transistors. Before the oxide was grown, the wafer was cleaned (Clean A process, explained in Appendix A) in order to remove residual impurities. Around 300 nm of oxide were grown on the substrate via wet oxidation process, i.e., pyrogenic steam oxidation. Figure 4.32 represents the silicon oxide on the wafer, where (a) presents the wafer before the oxidation and (b) after the oxidation.

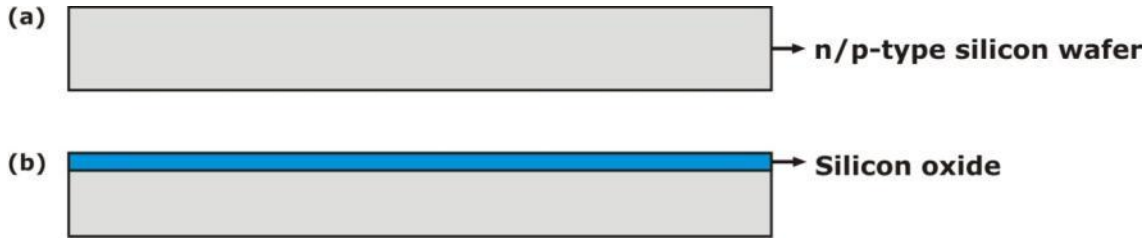


Figure 4.32: Cross section of the wafer with silicon oxide.

4.3.2 Gate Electrode Integration

Since the gate electrodes are made of aluminium, 50 nm of the metal were thermally evaporated at a rate of 4 Å/s. Subsequently, the wafers were baked out for 45 min at 150ºC in a convection oven, then 5 min in a HMDS (Bis(trimethylsilyl)amine) atmosphere at room temperature. The HMDS is used as an adhesion promoter for applying photoresist (Clariant AZ 5214E) via spin-coating process (CLARIANT, 2000).

The mask Gate(G) from Sen5 mask set (a mask set from the group Sensorik - Uni/Paderborn) was used in a positive photolithography process, in which a 365 nm wavelength light was applied for 2.7 s. After the development of the photoresist in a solution based on sodium hydroxide (NaOH), the wafers were baked out in the oven for 60 minutes at 130ºC for the resist hardening. Next, the aluminium was etched in a solution of phosphoric acid (H_3PO_4), acetic acid (CH_3COOH), nitric acid (HNO_3) and water at 80ºC. The wafers were then submerged in this etching solution until the exposed aluminium vanished. Oxygen plasma etching process applied during 4 min was used to strip off the photoresist from the wafers. Any other photoresist residue or particles on the wafer were removed through the Cleaning C process, which is explained in Appendix A. However, the cleaning procedure was taken without the ultrasonic bath in order to preserve the aluminium part that could be damaged during this process, shown in Figure 4.33, where (a) is the thermal evaporated aluminium, (b) the deposition of the photoresist, (c) the light exposure using the gate mask, (d) the resist development, (e) the aluminium etching, and (f) the resist stripping.

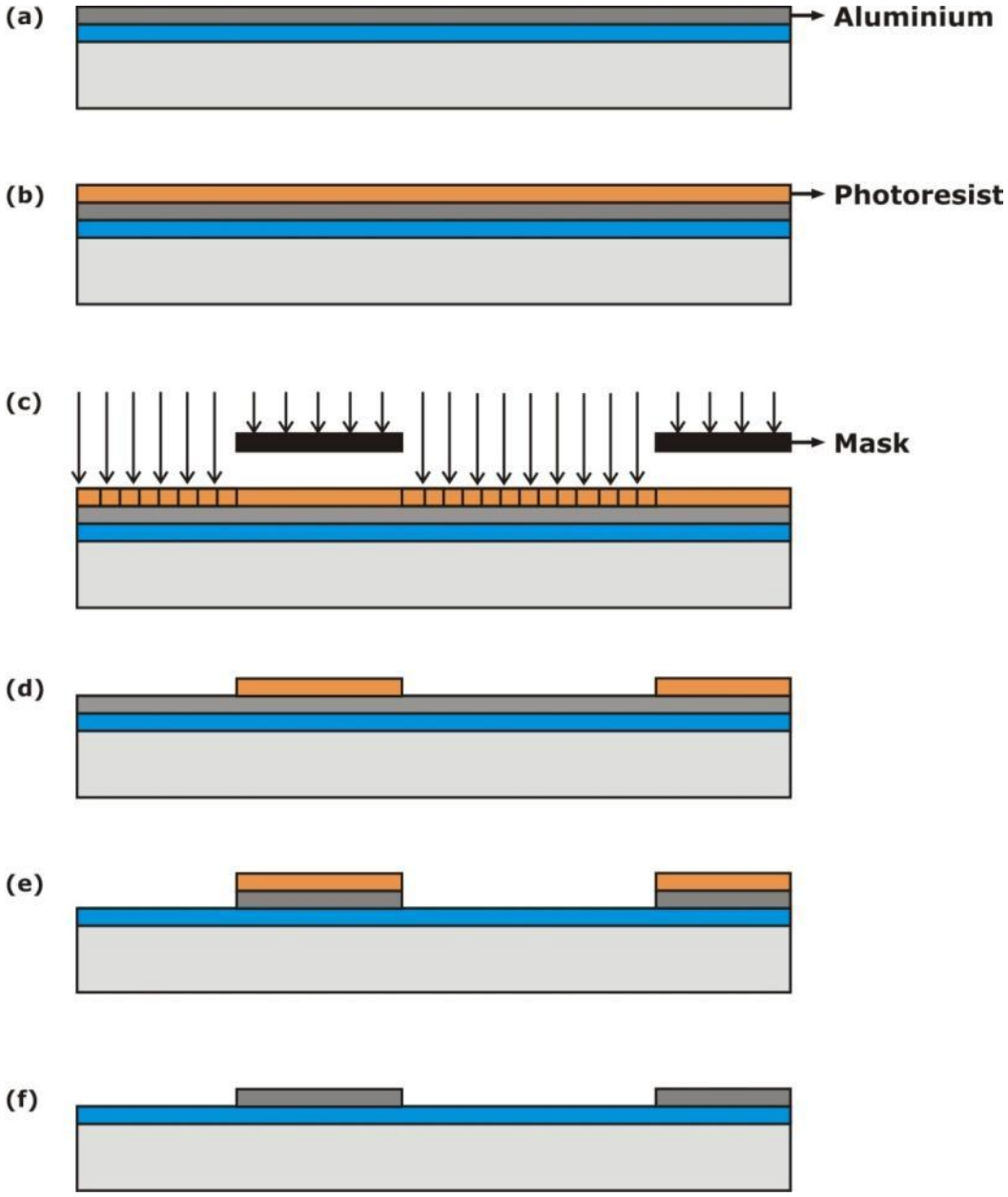


Figure 4.33: Cross-section of the wafer representing the gate integration.

4.3.3 Dielectric and Semiconductor Layer Integration

The next step consists in the deposition of PVP and ZnO nanoparticles solutions by spin-coating process. The PVP solution was prepared using 9 g of PGMEA (propylene glycol monomethyl ether acetate) as solvent; 0.17 g of Poly(melamine-co-formaldehyde)-methylated (PMCF-m, $M_w \approx 432$, Sigma-Aldrich) as cross-linker agent that was added while stirring, and then 0.83 g of PVP (Poly(4-vinylphenol)) ($M_w \approx 25{,}000$, Sigma-Aldrich) that was also added under the same condition. Before the deposition of the solution, an oxygen plasma etching process applied for 2 min was used in order to activate the surface. Two milliliters of PVP solution were deposited using a single-use syringe on the wafers at 800 rpm, followed by 30 s at 4000 rpm, which gives a 180 nm thickness, approximately. A soft bake-out at 100ºC for 60 s was performed.

The wafers were then annealed at 200ºC for 60 min to promote the cross-linker agent reaction with the PVP and ensure full removal of the solvent (Figure 4.34a).

For the ZnO nanoparticles layer integration (around 300 nm thick layer), two parts of nanoparticles solution (VP AdNano ZnO 20 DW) and one part of deionized water were mixed. Therefore, the effective ZnO nanoparticles concentration was 23 wt%. An ultrasonic agitation was performed for 30 min in order to break down the nanoparticle agglomerates. Next, it was applied 2 mL using a single-use syringe on the wafers at 500 rpm and then 30 s at 1000 rpm. A transparent ZnO nanoparticle layer was observed. The soft bake-out was performed at 110ºC for 5 min on the hotplate to fix the nanoparticles on the wafer, and after 60 min at 200ºC in the convection oven to completely remove the water (Figure 4.34b).

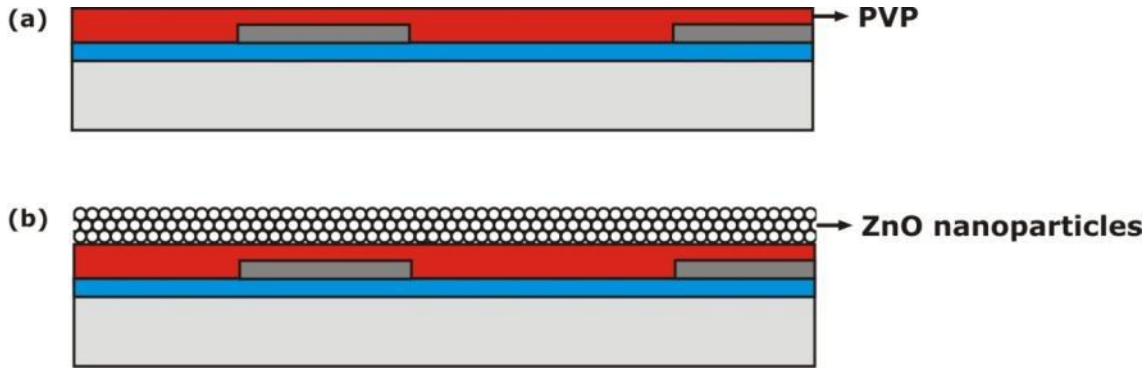


Figure 4.34: Cross section of the wafer representing the dielectric and semiconductor layers integration.

Figure 4.35 presents scanning electron microscope (SEM) micrographs of the ZnO nanoparticles layer and a regular surface can be observed. Table 4.1 and Table 4.2 show the concentration of the solutions.

Table 4.1: PVP solution concentration.

PVP Solution	
Solvent:	PGMEA
Poly(melamine-co-formaldehyde):	1.7 wt%
PVP:	8.3 wt%

Table 4.2: ZnO solution concentration.

ZnO solution	
Solvent:	Water
ZnO nanoparticles:	23 wt%

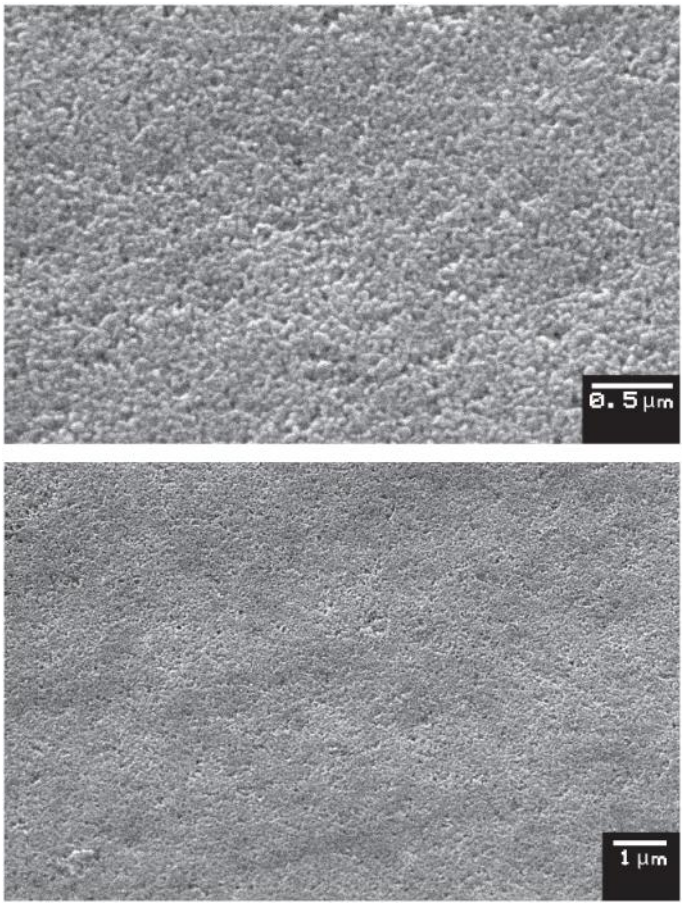


Figure 4.35: SEM micrographs of ZnO nanoparticle layer.

4.3.4 Vias

The vias were defined using the standard photolithography, the same procedure used for gate electrodes, using the mask Vias (V) from Sen5 mask set (Figure 4.36a-c) though. A wet-etching solution was used to etch the ZnO nanoparticles; the wafer was submerged in Pad Etch, a water based solution with 11-15% of hydrofluoric acid (HF), 30-34% of acetic acid (CH_3COOH) and 4-8% of propylene glycol (WILLIAMS et al., 2003) for 10 s. The oxygen reactive plasma etching process was performed to remove the PVP. The plasma was generated at 80 mTorr, the oxygen flow was 18 sccm and the RF power was 100 W. Subsequently, the wafer was submerged in acetone for 5 minutes to remove the resist. The vias integration process is represented in Figure 4.36d-e. An important aspect is that the vias connections are located far enough from the transistor active region (channel); therefore the resistance through the nanoparticles is high enough and does not interfere with the transistor functionality.

4.3.5 Drain and Source Electrode Integration

The drain and source pads were defined using the mask Leiter(L) from the Sen5 mask set. The photoresist (Clariant AZ 5214E) was applied via spin-coating process and a negative photolithography process was performed, based on the photoresist datasheet (CLARIANT, 2000). The development of the photoresist was done before the wafers were placed in the chamber for the thermal aluminium evaporation. It was deposited

200 nm of aluminium at a rate of 4 Å/s (Figure 4.36f-i). Lift-off technique was the final step, the photoresist was etched for 3 minutes in a NMP solution (N-Methyl-2-pyrrolidone), and then it was ultrasonic bathed in acetone until only the drain and source structures remained (Figure 4.36j).

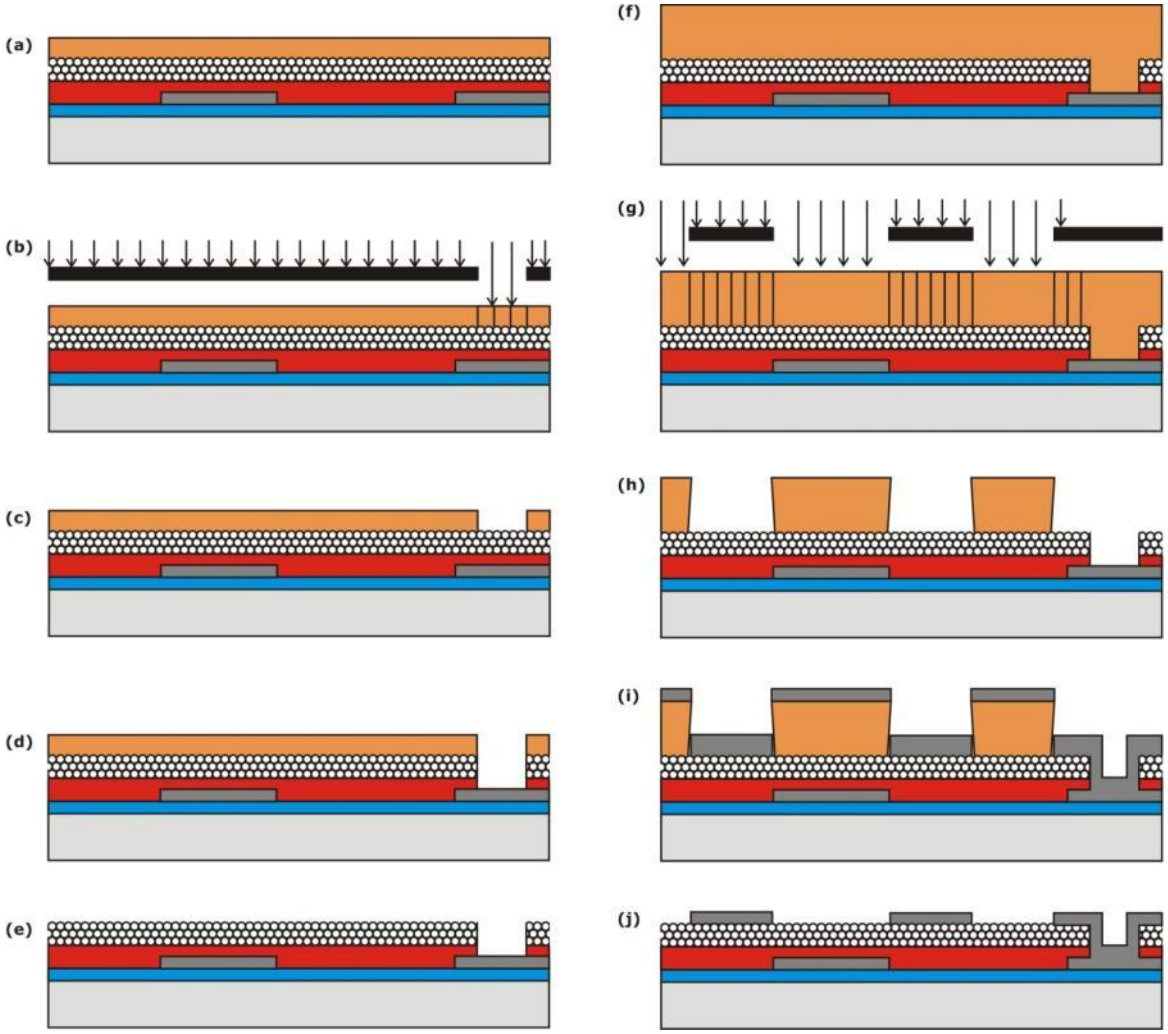
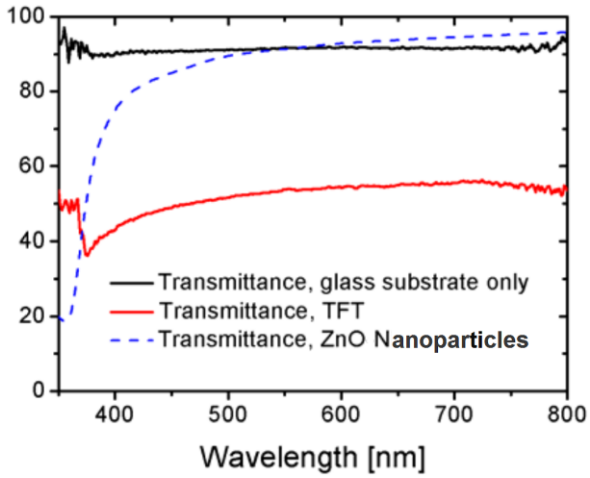


Figure 4.36: Cross section of the wafer representing the vias and drain/source electrodes integration.

4.3.6 Optical Transparency

The same base transistor was integrated by Wolff et al. (2011-a) in a borosilicate glass substrate (Schott BOROFLOAT ® 33) and the optical transparency of the device was evaluated. Figure 4.37a shows the transmittance in the visible wavelength spectrum. It can be seen that over 50% of the light source intensity is transmitted through the sample as shown in the red trace, whereas 5% are absorbed by the glass substrate as shown in the black curve. From the ZnO nanoparticle datasheet (DEGUSSA, 2006), the nanoparticles absorb approximately 5-20% of the intensity as shown in the blue dashed curve. Therefore, the opaque metal (aluminium) and the dielectric layer (PVP) are responsible for the remaining percentage of absorption. By using transparent conductive oxides like indium tin oxide (ITO), the metal electrode absorption can be avoided. In Figure 4.37b the sample appears to be transparent, even

using opaque electrodes; the main reason is because the electrodes are tiny and therefore they are not visible to the naked eye.



(a) (b)

Figure 4.37: (a) Optical transmittance of the glass substrate, TFT and ZnO nanoparticles, and (b) Samples on a glass substrate. (WOLFF et al., 2011-a)

4.3.7 Integration Difficulties

During the transistors' integration difficulties were observed. The influence of the humidity in the air, of the temperature of the wafers' surface; and of the temperature difference between the wafer and the solutions are not completely clear yet. Also, the number of revolution per minute in the spin-coating process influenced the deposition quality. In the ZnO nanoparticles deposition process, the nanoparticle water-based solution did not attach to the polymer layer due to its hydrophobic character. Figure 4.38 presents the resulting interaction of the PVP layer and the nanoparticle solution after the ZnO nanoparticles deposition. Only isolated agglomerated nanoparticles could be found.

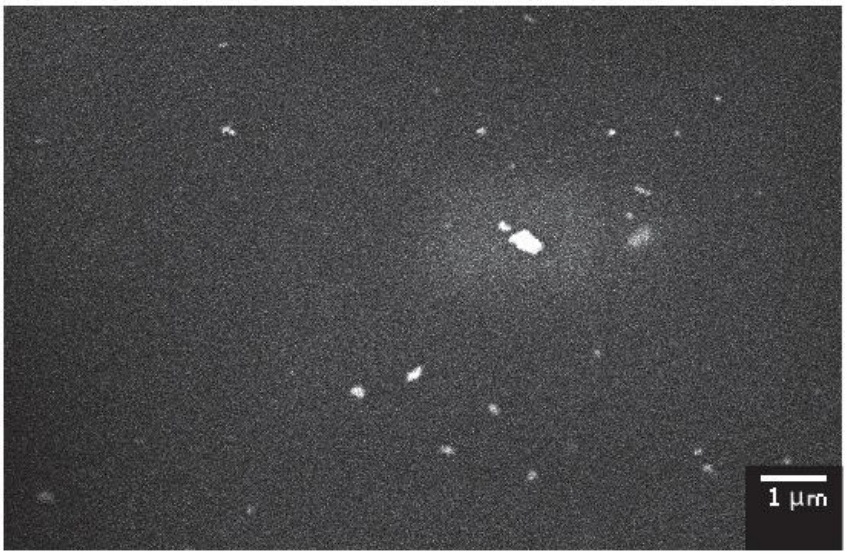


Figure 4.38: ZnO agglomerated nanoparticles on a PVP layer (in detail).

Figure 4.39a shows the border between the PVP and ZnO nanoparticles layers, since it was not possible to cover the whole wafer with nanoparticles dispersion. It was observed an agglomeration of nanoparticles in the border. Figure 4.39b presents a defect on the ZnO nanoparticle layer, in which a lack of nanoparticles could be seen. The shape of the defect suggests a crystalline reaction during the annealing of the nanoparticles.

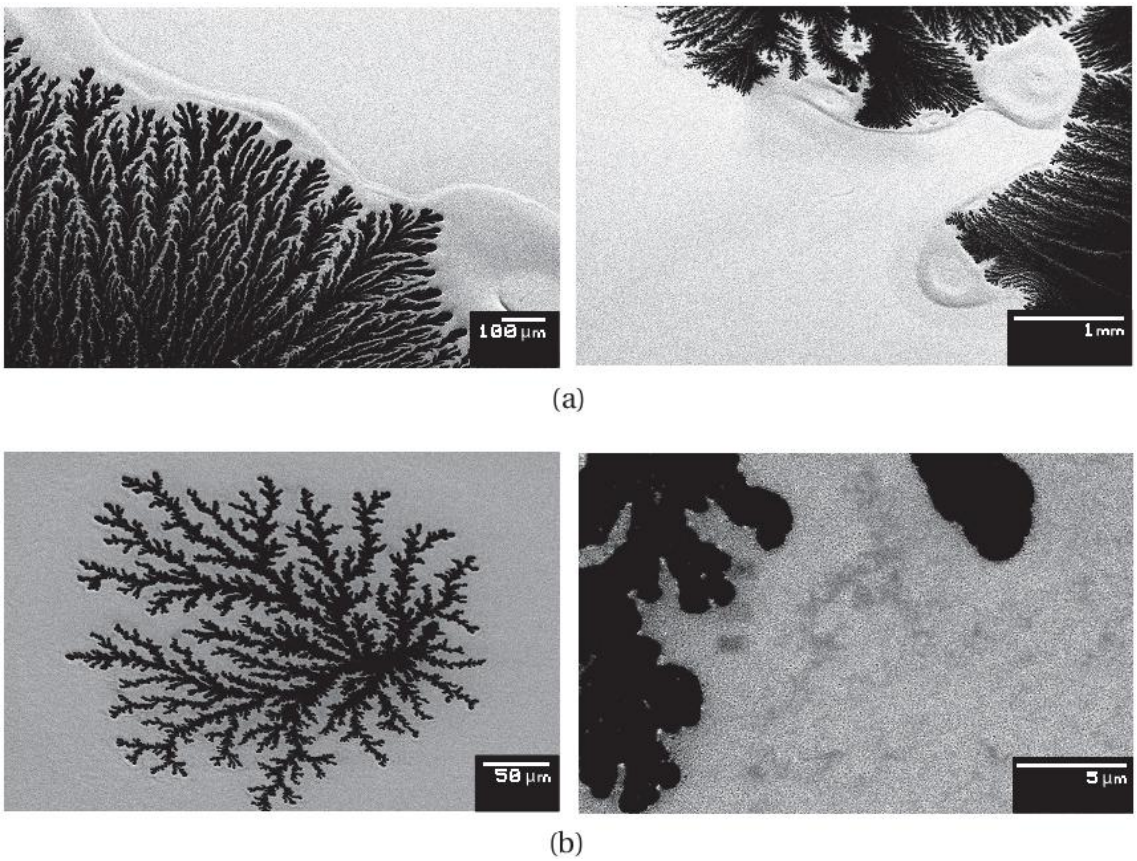


Figure 4.39: (a) ZnO nanoparticle layer border; and (b) defect on ZnO nanoparticle layer (in detail).

Another difficulty was the time degradation in these transistors; it means that the time interval among processes may interfere in the transistors performance. Also, the time between each measurement and the atmosphere in which the wafers were placed influenced their characteristics.

4.4 Transistor with Silicon Dioxide as Gate Dielectric

In this subsection, it is presented the integration procedure for the ZnO nanoparticle TFT in which low-temperature plasma enhanced chemical vapor deposition (PECVD) SiO_2 was used as gate dielectric layer. It is important to clarify that this transistor was not integrated by the author. Fabian Assion from University of Paderborn integrated this transistor and shared the data with the author. The complete

and more detailed fabrication procedure can be found in (ASSION, 2010) and (ASSION et al., 2011). Figure 4.40 represents the schematic cross-section of the transistor, and a top-gate device is observed. The TFTs have a channel length (L) of 0.3 µm and channel width (W) of 100 µm. The integration process is based on sidewall-etchback technique (HORSTMANN et al., 1996). The top-gate structure was chosen due to process issues, as discussed below.

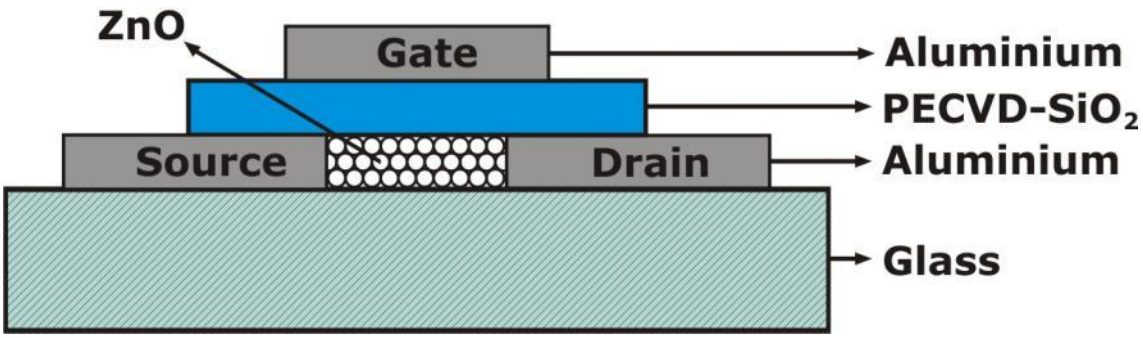


Figure 4.40: Schematic cross-section of ZnO nanoparticle TFT with PECVD-SiO_2 as gate dielectric. Adapted from (ASSION et al., 2011)

Borosilicate glass (Schott BOROFLOAT ® 33) was used as substrate for the transistor integration (SCHOTT, 2010). The maximum temperature of the manufacturing process has been limited to 150ºC, which enables the use of low-cost substrates such as Polyethylene Naphthalate (PEN) and Polyimide (PI) (DUPONT, 2010).

The main task in the integration process for this transistor is the creation of a nanoscale space between the source and drain regions, which may have the same size of the used ZnO particles. Low-cost lithographic methods as the ones found in universities have resolution of about 1 µm, which is insufficient for single/few particles transistors. Therefore, to overcome this issue, a process based on the sidewall-etchback technique was used (HORSTMANN et al., 1996). In this case, photoresist was previously patterned using conventional photolithography (Figure 4.41a). After a PECVD oxide (300 nm thick layer) was deposited conformally as depicted in Figure 4.41b. Since the photoresist is sensitive to high temperatures, the deposition of SiO_2 was done at low temperatures (100ºC). The channel length of the transistor is determined by the thickness of the oxide, as explained below.

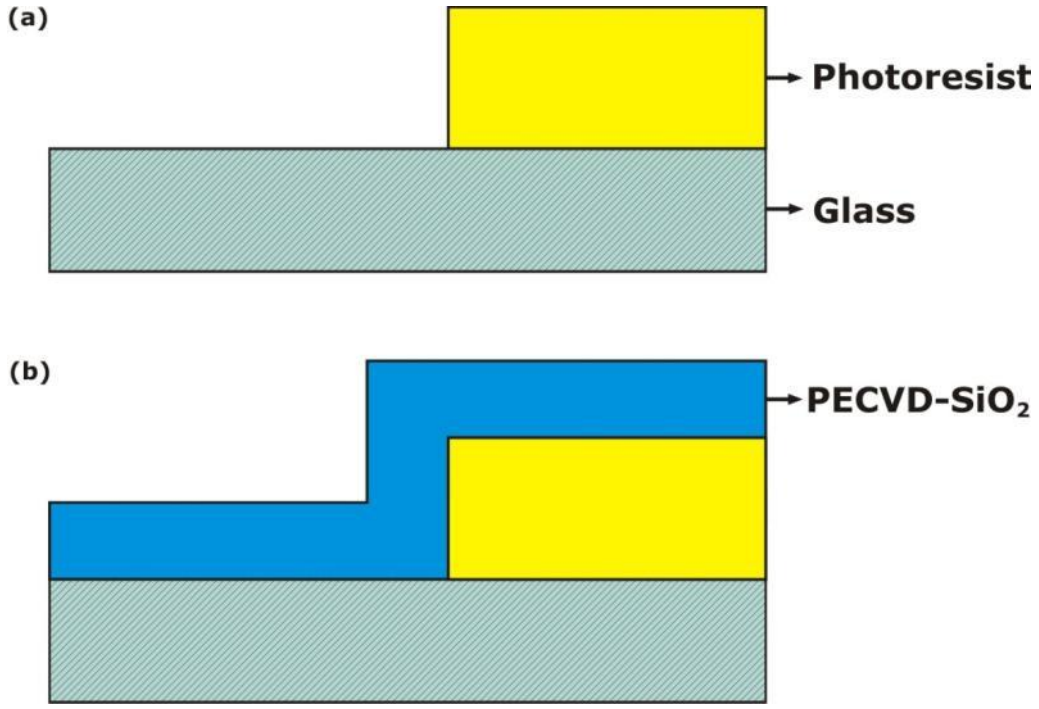


Figure 4.41: Part of the integration process of the TFT with SiO_2 as gate dielectric. Adapted from (ASSION et al., 2011)

By previously measuring the oxide layer thickness and knowing the etching rate, it is possible to determine the required process time for anisotropically etch the oxide using reactive ion etching (RIE) as shown in Figure 4.42a. After, using oxygen plasma, the photoresist was ashed, leaving a thin structure, spacer, over the substrate (Figure 4.42b).

This step was one of the reasons for choosing a top-gate instead of a bottom-gate device. For the bottom-gate structure, it is very critical the process time because the gate dielectric (previously deposited) is directly below the oxide. If the process take too long, the dielectric layer may be permanently damage; and for short etching times it is also problematic, because a few nanometers of oxide on the photoresist can prevent the removal of the resist by O_2 plasma. On the other hand, for the top-gate structure is significantly less demanding in this regard, as an over-etching attacks only the substrate and therefore only arise unevenness. Other parts of the transistor are undamaged.

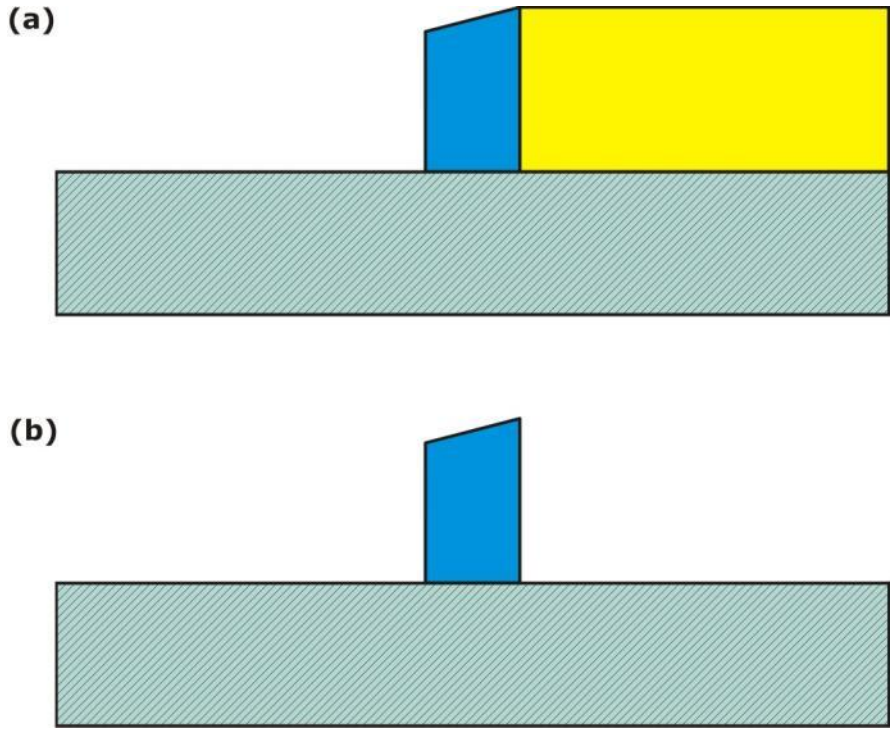


Figure 4.42: Part of the integration process of the TFT with SiO_2 as gate dielectric. Adapted from (ASSION et al., 2011)

Then the structures (spacers) were covered with aluminium (150 nm thick layer) in a high-vacuum evaporation process (Figure 4.43a). As long as one adheres strictly to the high-vacuum condition during the evaporation, the process brings out a non-conformal deposition. If the layer thickness is less than the spacers' height, the upper part of the line sidewalls is not covered with aluminium. Exhibiting unshielded sidewalls, the spacers can be removed by ultrasonic bath and trifluoromethane RIE under tilted position, which results into nanoscaled gaps. The process is shown in Figure 4.43b.

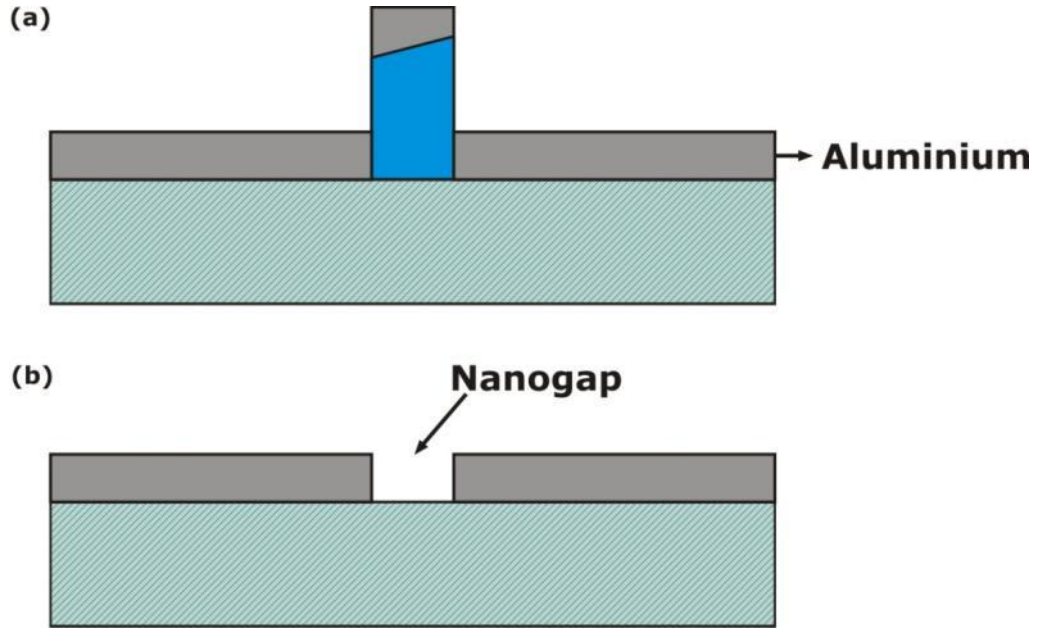


Figure 4.43: Part of the integration process of the TFT with SiO_2 as gate dielectric. Adapted from (ASSION et al., 2011)

Steps from Figure 4.41 through Figure 4.43 represent the integration of nanotrenches using conventional lithography, and the structures are orientated and defined by deposition and etching processes. Additionally, as it was previously presented, the thickness of the deposited oxide defines the size of the nanogap.

Subsequently, the source and drain contacts were structured. This was done using conventional lithography procedure and chlorine-RIE etching process in pure silicon tetrachloride atmosphere. Figure 4.44a shows the structure before application of the ZnO dispersion. A water based solution of ZnO nanoparticle (1,5 wt%) was afterwards spin-coated on the substrate as depicted in Figure 4.44b and subsequently dried at 65 ºC. In order to break up agglomerates and to homogenize the dispersion, the solution was previously treated in an ultrasonic bath.

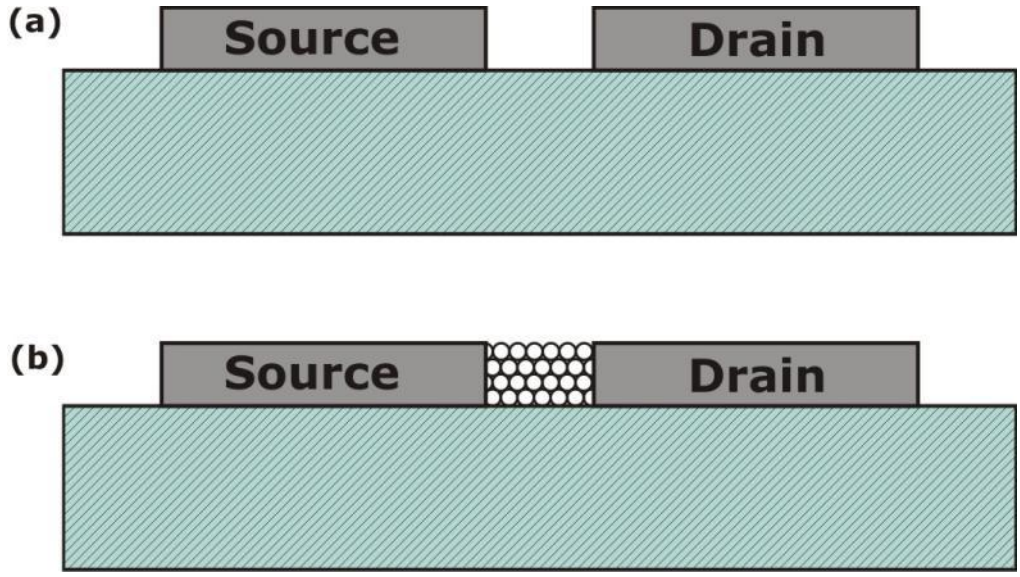


Figure 4.44: Part of the integration process of the TFT with SiO_2 as gate dielectric. Adapted from (ASSION et al., 2011)

After the deposition of ZnO nanoparticles (150 nm thick layer), the wafer was placed in a PECVD system at only 130ºC, and the silicon dioxide gate dielectric was coated (Figure 4.45a). The dielectric fixed the nanoparticles and increases its adhesion to the substrate, consequently preventing the nanoparticles from vanishing during the next process step. Subsequently, aluminium was evaporated, and then a lift-off technique was used to structure the gate electrodes (Figure 4.45b). After patterning the gate electrodes, it was still missing the opening of the source and drain contacts. These are below the dielectric (SiO_2) and were etched using fluorine chemistry in a RIE system. Finishing the exposure of the contacts, the nanoparticulate ZnO transistor in a top-gate architecture is done as shown in Figure 4.45c.

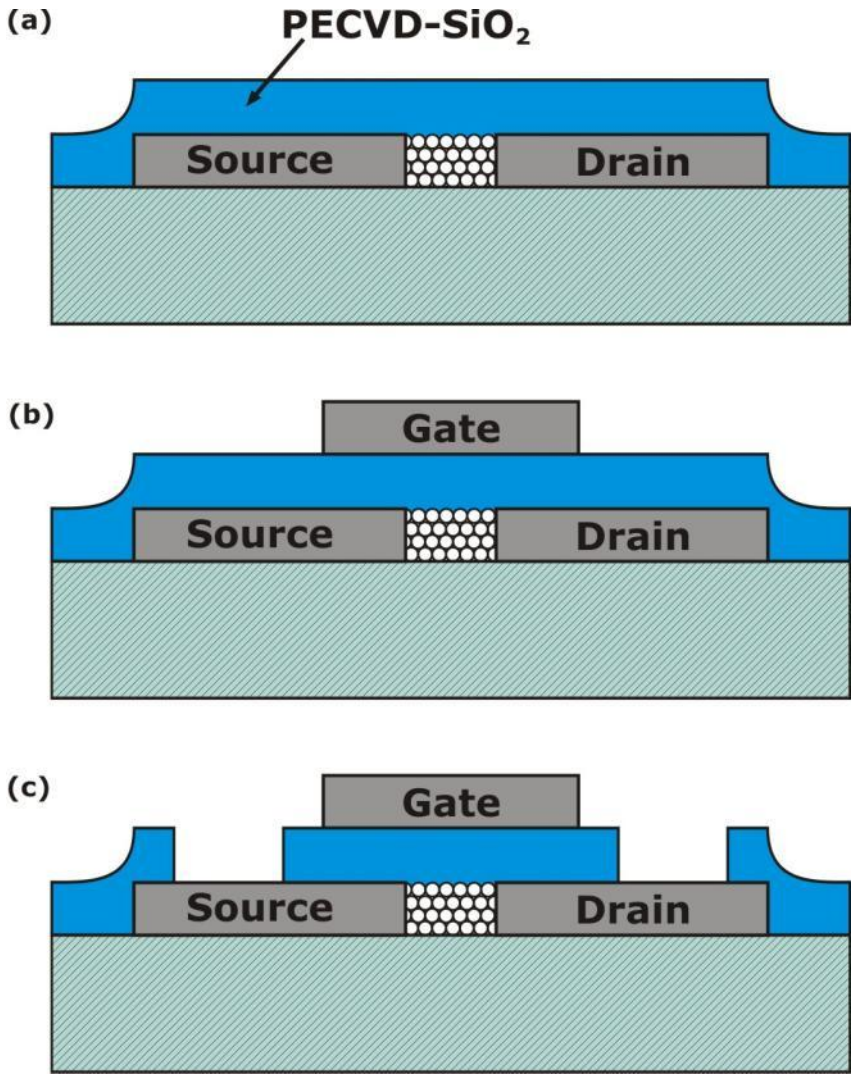


Figure 4.45: Part of the integration process of the TFT with SiO_2 as gate dielectric. Adapted from (ASSION et al., 2011)

4.5 Transistor Characterization

The transistors were characterized in a dark environment under ambient atmosphere and relative humidity ranging from 38% to 45% using an Agilent 4156A - Precision semiconductor parameter analyzer. For the investigation in this work, the most interesting and important characteristics is the threshold voltage, however the field-effect mobility, the I_{on}/I_{off} ratio and the subthreshold voltage slope were also characterized. Additionally, stress tests were also used to characterize the transistors, in which fixed electrical bias are applied in the drain and gate electrode and the transistor drain current is analyzed.

Figure 4.46 shows, in detail, the probes used in the transistor characterization process.

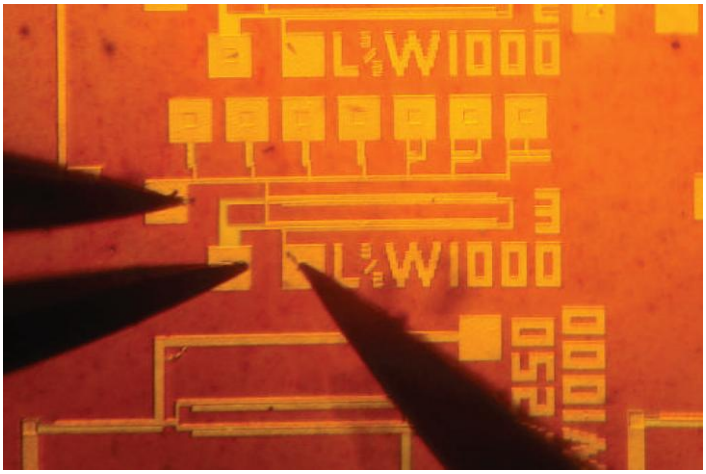


Figure 4.46: Probes used in the characterization process (detail).

In Appendix B, the methods used to characterize the transistors and the background theory will be briefly discussed.

5 RESULTS AND DISCUSSIONS

In the following section studies found in the literature related to the hysteretic behavior of the ZnO nanoparticle transistor are presented. Conjointly, electrical characterization and experimental results of devices integrated by our group will be presented and discussed.

5.1 Hysteresis Studies

In the previous section, the key points of ZnO nanoparticle TFT operation were presented. It was also shown that the presence of the hysteresis in ZnO based transistors is reported by several authors (FABER et al., 2009), (VERBAKEL et al., 2006), (LEE et al. 2006), (SUN et al., 2005), (NANDI et al., 2003) and (WANG et al., 2010).

Here we present the results of our theoretical and experimental efforts towards providing a qualitative model for the hysteresis. For this sake two kinds of thin-film transistors were integrated. One integrated using cross-linked PVP as gate dielectric and the other using PECVD-SiO_2. Before the characterization of the integrated transistors, however, studies related to the hysteresis will be briefly discussed.

Lim et al. (2007) reported that using PVP as gate dielectric may influence the threshold voltage, shifting it according to the sweeping direction of the gate voltage on organic transistors. Faber et al. (2009) proposed that the emission and capture of positive charges by traps located in the nanoparticles/PVP interface causes the hysteretic behavior as explained in the previous section. However, this model (FABER et al., 2009) does not explain the reason for the drain current increase when the gate voltage sweeps backwards, neither the inversion of the hysteresis direction when the transistor is heated up. This behavior was observed in the transistors fabricated in this work, as discussed below.

The presence of hydroxyl (OH-) groups in the gate dielectric surface changes the PVP from a nonpolar to a polar character (LIM et al., 2007), (VERES et al., 2004) and (JUNG et al., 2005). Also, polymer dielectrics, which contain a significant amount of hydroxyl groups inside or at the surface, are responsible for the hysteresis in organic transistors, as well as for the higher gate current leakage (LIM et al., 2007), (LEE et al., 2006) and (KIM et al., 2008).

The qualitative model proposed in this work is based on (VERES et al, 2004), (HWANG et al., 2006) and (HWANG et al., 2008), in which a hysteresis mechanism for pentacene thin-film transistors with PVP as gate dielectric was presented. The slow polarization of dipoles, such as hydroxyl groups in the PVP bulk, reoriented by an applied electric field, was considered as the main reason for the observed behavior.

Figure 5.1 shows the trapping mechanism in the polymeric gate dielectric, in which it is possible to observe the dipoles in the PVP bulk and the electron traps associated to the OH- group at the semiconductor/dielectric interface. The direction of the hysteresis, considering the influence of PVP, will be determined by the dominant mechanism on the device depending on measurement and process conditions such as annealing temperature, time, concentration of cross-linker agent and dielectric thickness (VERES et al, 2004), (JUNG et al., 2005), (HWANG et al., 2006) and (HWANG et al., 2008).

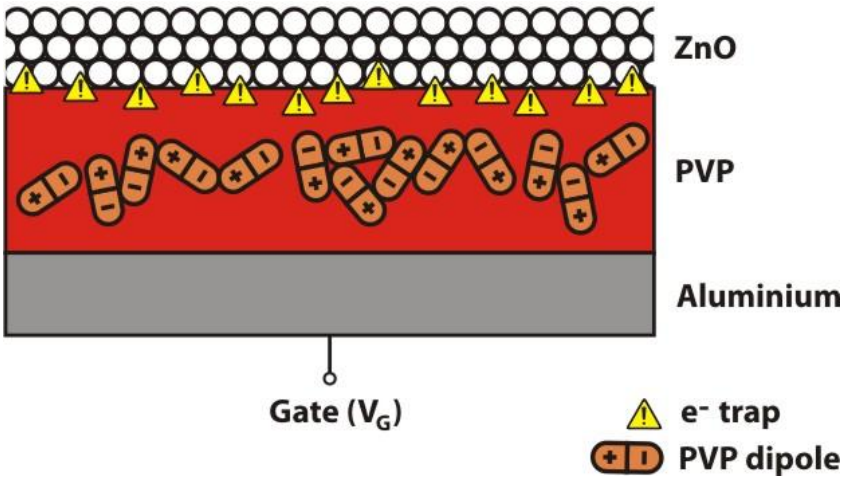


Figure 5.1: Trap mechanism in ZnO nanoparticle TFT with PVP as gate dielectric.

Traps in the nanoparticles may also play a vital role in the hysteresis. Hirschwald (1985) reported, in early studies, the upward band bending by ionosorbed negatively charged oxygen molecules in the surface and grain boundary of ZnO films. Located on the surface, absorbed oxygen molecules capture free electrons from the ZnO reducing the conductivity near the surface (JIN et al., 2008), (HIRSCHWALD et al., 1985), (WANG et al., 2010) and (VERBAKEL et al., 2006). The desorption of the oxygen molecules upon UV illumination is associated with a generation of electron-hole pairs. The generated holes migrate to the surface and release the absorbed oxygen molecule, increasing the concentration of free electrons in the ZnO film. As explained by (VERBAKEL et al., 2007a) and (VERBAKEL et al., 2007b), in addition to the UV interaction, it is also possible to induce desorption of oxygen by the application of bias (voltage) or the injection of positive charges through the metal/ZnO film contact (VERBAKEL et al., 2007a). The oxygen traps mechanism in nanoparticulate ZnO is depicted in Figure 5.2, representing the increase of free carriers (electrons). Interactions between the nanoparticle surface and the atmosphere are highlighted by the large surface of nanomaterial compounds (DEGUSSA, 2006) and (XU et al., 2000) and its effects may influence the entire bulk of the ZnO film (JIN et al. 2008).

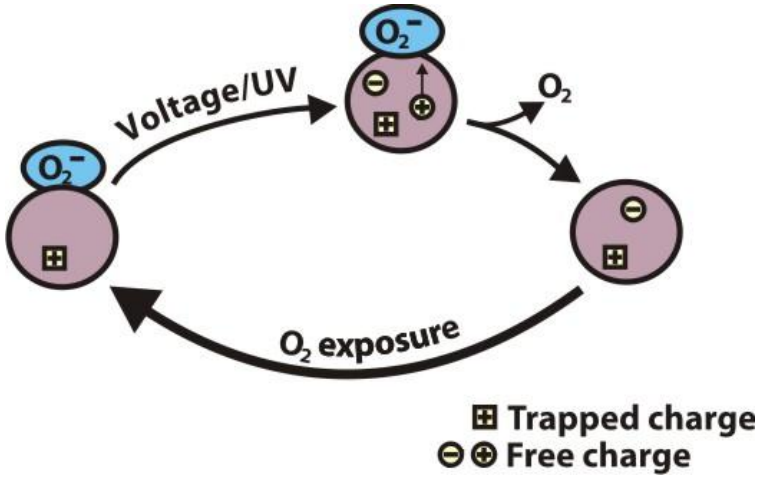


Figure 5.2: Oxygen trap mechanism in nanoparticulate ZnO. Adapted from (VERBAKEL et al., 2007a)

5.2 Results

The results of the characterization and relations with the previously mentioned studies will be presented in this subsection. First, the characteristics of the ZnO TFT with PVP as gate dielectric will be present. Subsequently the ones for PECVD-SiO_2 as gate dielectric are presented.

The device with PVP as gate dielectric shown in Figure 4.31 presents a highly pronounced anti-clockwise hysteresis in the transistor transfer curve at room temperature when the gate voltage is scanned from -10, 20 to -10 V, as shown in Figure 5.3. The hysteresis can be reproduced again in the same transistor, as well as in other transistors integrated by this process, under similar environmental conditions. The characteristics of the transistors are strongly dominated by its hysteretic behavior.

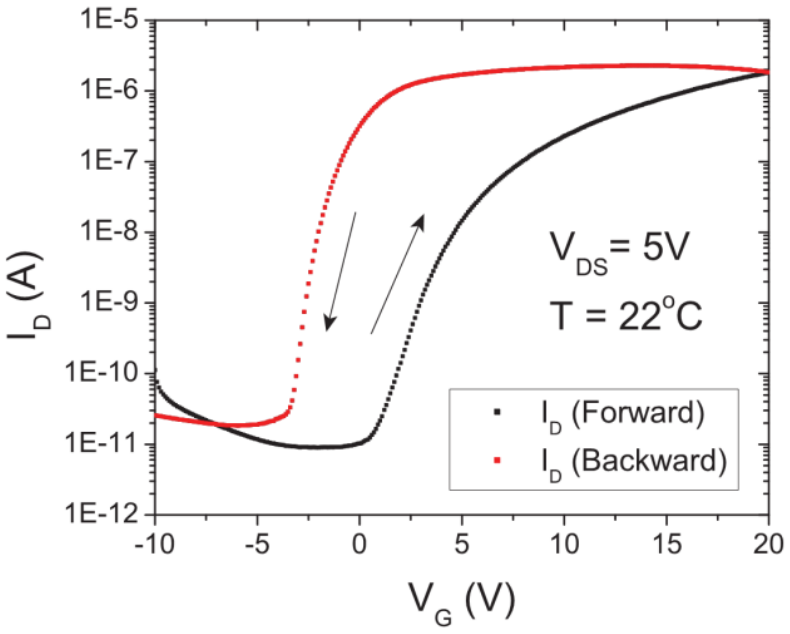


Figure 5.3: ZnO nanoparticle TFT transfer characteristic at room temperature ($W = 1000\ \mu m$, $L = 3/2\ \mu m$, Sweep Rate = $2\ V/s$).

The threshold voltage, field-effect mobility, I_{on}/I_{off} ratio and sub-threshold slope voltage are extracted in both forward and backward sweep of the gate voltage. The characteristics depicted in Table 5.1 are the mean value of 16 (sixteen) samples.

Table 5.1: Electrical characteristics of ZnO nanoparticle TFT ($W = 1000\ \mu m$, $L = 3/2\ \mu m$) depending on the gate voltage sweeping direction.

	$V_D\ (V)$	$V_T\ (V)$	$\mu_{FE}\ (cm^2/Vs)$	I_{on}/I_{off} ratio	S(V/dec)
Forward sweeping	5	9.17	$5.21 \cdot 10^{-3}$	$5.43 \cdot 10^{5}$	1.08
Backward sweeping	5	-2.75	$6.92 \cdot 10^{-3}$	$2.74 \cdot 10^{5}$	0.37

In Appendix C, it is possible to find the distribution of the characteristics over the samples and more details about the device, as well as the device characteristic for other drain voltages.

The hysteretic behavior depicted in Figure 5.3 has the polarization of the PVP as the key factor. The dipoles slowly become oriented by the gate voltage applied, enhancing its effect; therefore, increasing the drain current even when the gate voltage starts to sweep backwards. In order to turn off the transistor, a lower gate voltage is required. The polarization of dipoles in the polymeric material was predicted to be a slow process (HWANG et al., 2006) and (HWANG et al., 2008). This is in agreement with the observed current increase, despite the invariant bias voltage, as shown in the stress test in Figure 5.4. A time constant of about 120 seconds was extracted considering a first order exponential function. This result is consistent with the hysteresis direction presented in Figure 5.3. Also, the slow polarization reinforces the drain current increase when the gate voltage is swept back.

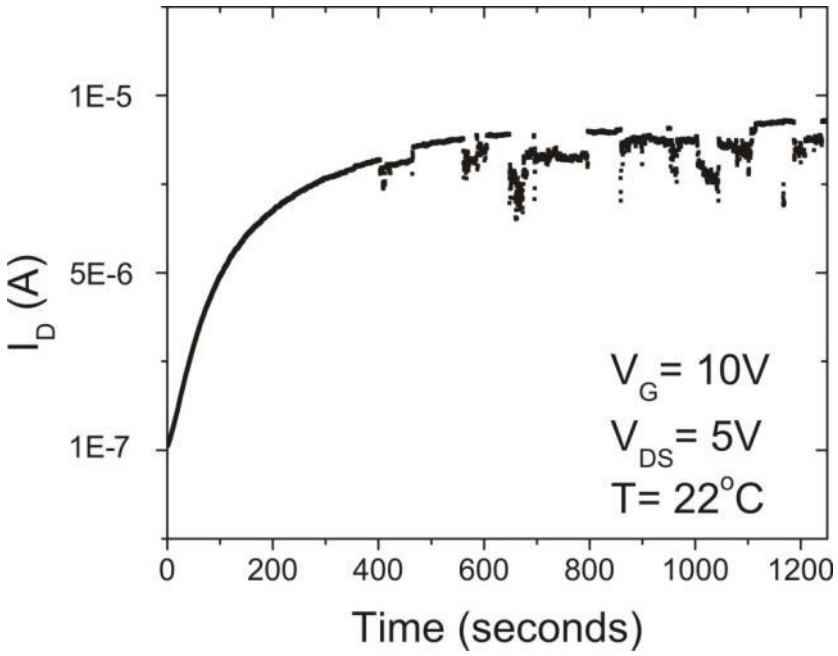


Figure 5.4: Stress test at room temperature in a ZnO nanoparticle TFT ($\boldsymbol{W = 1000\ \mu m}$, $\boldsymbol{L = 3/2\ \mu m}$, $\boldsymbol{V_G = 10\ V}$, $\boldsymbol{V_D = 5\ V}$).

The increase of the drain current at fixed electric bias was also reported by Faber et al. (2009). His device presented a faster response than the one extracted in this work as it can be observed in Figure 5.5; nevertheless, it is possible to observe that by applying a higher gate voltage, the polarization of PVP is faster due to the higher electric field interacting with the PVP dipoles.

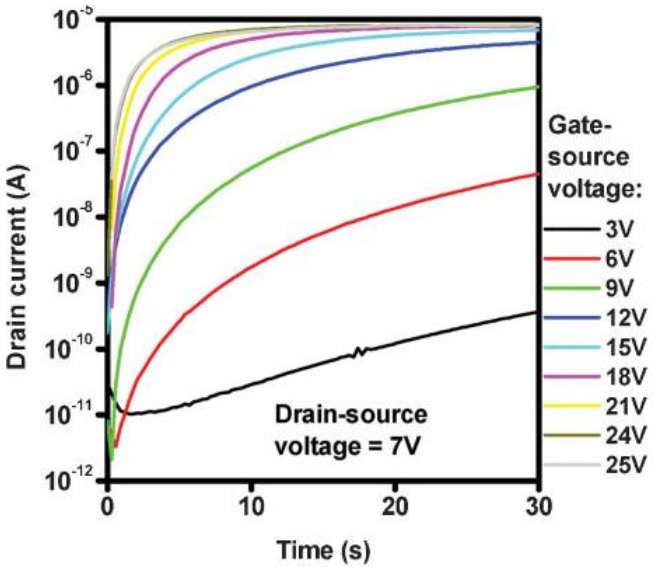


Figure 5.5: Time-dependent response of the drain current to the application of a positive gate-source voltage, showing that the response is more rapid for larger gate-source voltages. (FABER et al., 2009)

It is well-known that the electron transport mechanism in nanoparticulate ZnO films is based on percolation paths as was discussed in the previous section (MEULENKAMP, 1999). Hence, the discrete current observed in the Figure 5.4 is attributed to the capture and release of traps located in a specific current path in the nanoparticle film. It electrostatically affects the transistor and, consequently, its current (KACZER et al., 2010), (MUELLER et al., 1998), (SILVA et al., 2006) and (LEE et al., 2009).

This phenomenon is observable in nanoscale MOSFET through the creation of percolation paths due to the random dopant fluctuation (RDF) (KACZER et al., 2010) and (MUELLER et al., 1998). On the other hand, it can be assumed that the transistor integrated in this work is relatively large compared to a nanoscale MOSFET and its dopants, which are of the order of angstroms. In the case of ZnO nanoparticle TFT, the primary nanoparticle size used to integrate the transistor are in the order of 15-30 nm of diameter, and they are normally found in the form of agglomerates with 100 nm (DEGUSSA, 2006). The transistor integrated here have dimension of micrometers; nevertheless, the current transport is through the formed particle network, creating the percolation paths (MEULENKAMP, 1999). Therefore, it is possible to say that the same phenomena may occur even considering a relative large transistor.

The different levels in the current shown in Figure 5.4 are related to active traps located in a given current path. Assuming an electron trap located in one specific current path in the ZnO nanoparticle network, and the trap being filled with an electron, the current in the transistor is decreased. However, when the electron is released the current increases, and a discrete current can be observed (MUELLER et al., 1998), (SILVA et al., 2006) and (LEE et al., 2009). Figure 5.6, for instance, represents a schematic of the electron “flow” from source to drain through the nanoparticles. For simplicity, just a few paths are shown. In an average device, a greater number of paths as well as a denser network are expected. Considering three active traps locates at different site A, B and C as shown in Figure 5.7. The trap located at B will have a greater influence than the traps located at A in the device current, assuming a higher current density in B. The trap located at C will present nearly no influence in the device current, since it is not located in an active current path (MUELLER et al., 1998).

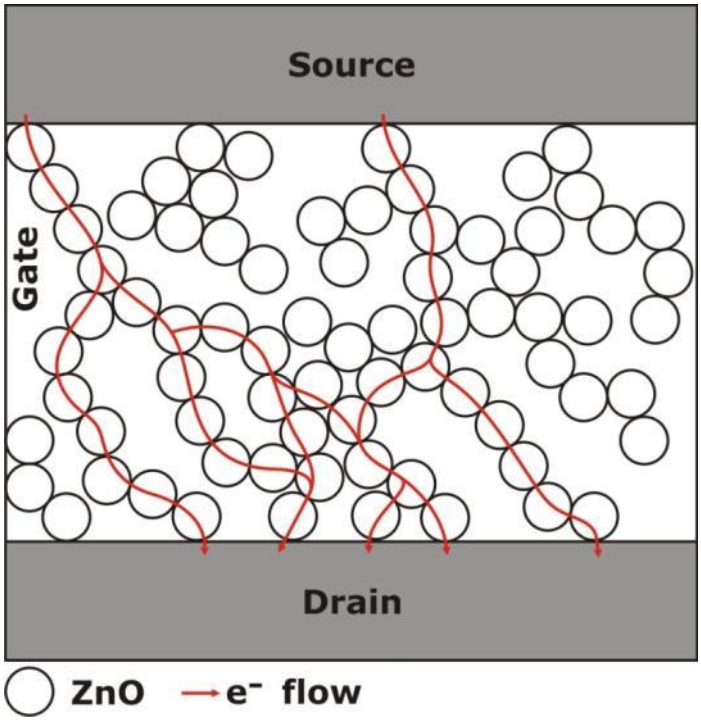


Figure 5.6: Electron flow in a nanoparticulate ZnO film.

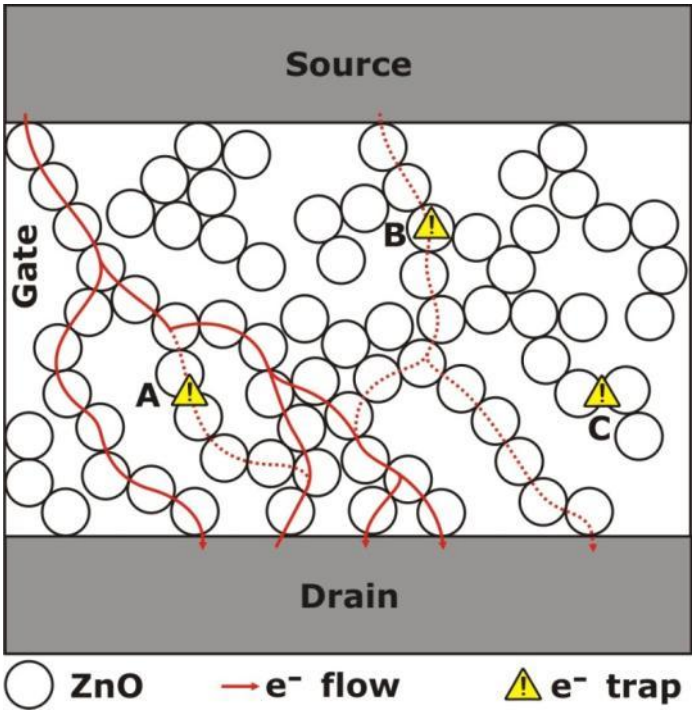


Figure 5.7: Electron flow in a nanoparticulate ZnO film under effect of active traps.

Another test performed on the transistor was the measurement of the device for multiple cycles. The result is shown in Figure 5.8, with a three-second pause between each characterization. The arrow shows the repetition direction, i.e., the first

measurement was the one with the lowest drain current at the end of the forward sweeping of the gate voltage.

By comparison to the transfer characteristics in Figure 5.8, it is possible to observe mainly three aspects. First, by applying multiple cycles to the transistor with a short break between each measurement, an increase of the drain current at the end of the forward sweep is observable. This result is in agreement with the stress test, in which the drain current increase due to the polarization of the polymeric dielectric.

Second, it is possible to observe that in the first electrical characterization, the "forward" curve is shifted to the left compared to the other two measurements. This can be attributed to a randomly orientation of the PVP dipoles at the first measurement. And for last, as depicted in Figure 5.8, the "backward" curve is left shifted at subsequent characterization, indicating that more PVP dipoles are getting orientated by the applied electric field and also the presence of a residual polarization of the dielectric.

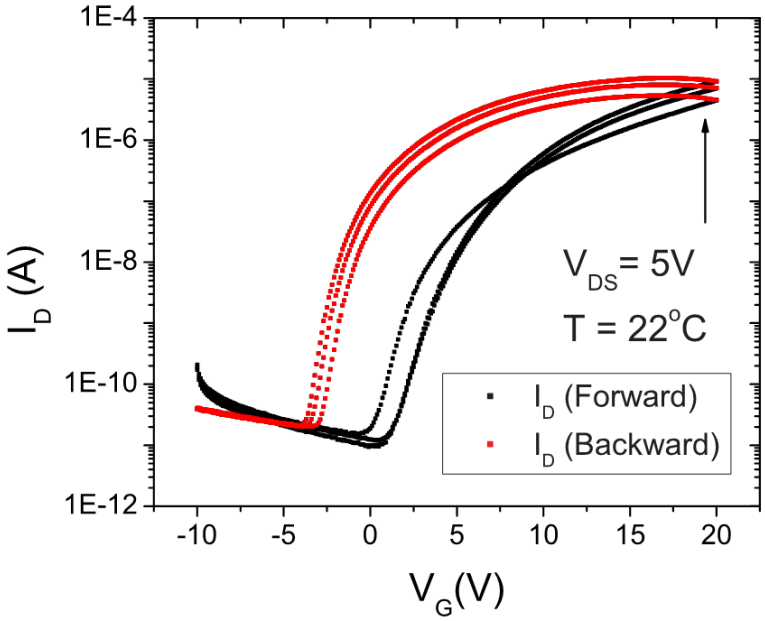


Figure 5.8: Multiple electrical characterization on ZnO nanoparticle TFT at room temperature ($W = 1000\ \mu m$, $L = 3/2\ \mu m$, Sweep Rate = $2\ V/s$).

In Figure 5.9 the transistor was electrically characterized in a slower sweep rate (0,003 V/s). In comparison to the I-V curve shown in Figure 5.3, the on current level is higher with slower sweep rate. This test is also in agreement with the slow polarization of the PVP and the stress test depicted in Figure 5.4. The change in the hysteresis when slowly sweep the gate voltage is also in concordance with the results of (FABER et al., 2009)

Conjointly, Figure 5.9 presents a similar step-like behavior as the one shown in Figure 5.4. Another example of the traps influence in the current path is depicted in Figure 5.10, in which a discrete current is observed. The characteristic of the Figure 5.9 and Figure 5.10, contributes to reinforce that the discrete current in the stress test (Figure 5.4) is related to capture and release of traps, and not noise originated from the measure procedure.

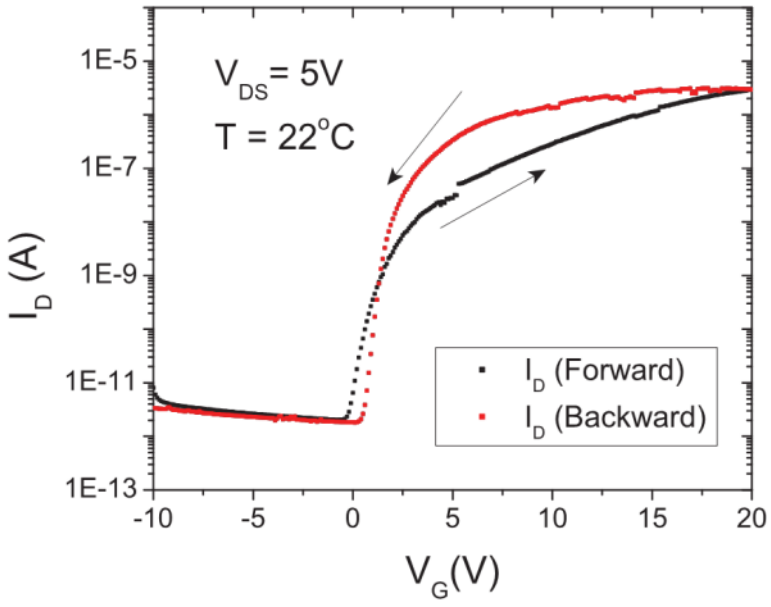


Figure 5.9: ZnO nanoparticle TFT transfer characteristic at room temperature with Sweep Rate = 0.003 V/s ($W = 1000\ \mu m$, $L = 3/2\ \mu m$).

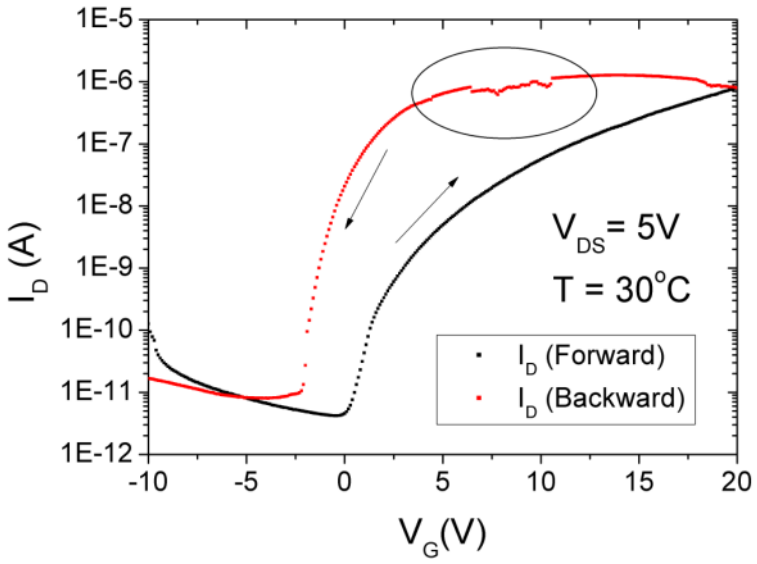


Figure 5.10: ZnO nanoparticle TFT transfer characteristic at 30ºC ($W = 1000\ \mu m$, $L = 3/2\ \mu m$, Sweep Rate = 2 V/s).

The gate current leakage, depicted in Figure 5.11, is in the order of magnitude of $10^{-10}\ A$. When a negative gate voltage is applied, the drain current in the transistor is attributed to the gate current leakage through the dielectric. This can be observed by the drain current comparison between Figure 5.3 and Figure 5.11 for $V_G < 0\ V$. The leakage through the gate dielectric is affected by the PVP polarization which works as an electron transport barrier when the gate voltage is swept back, lowering the drain current.

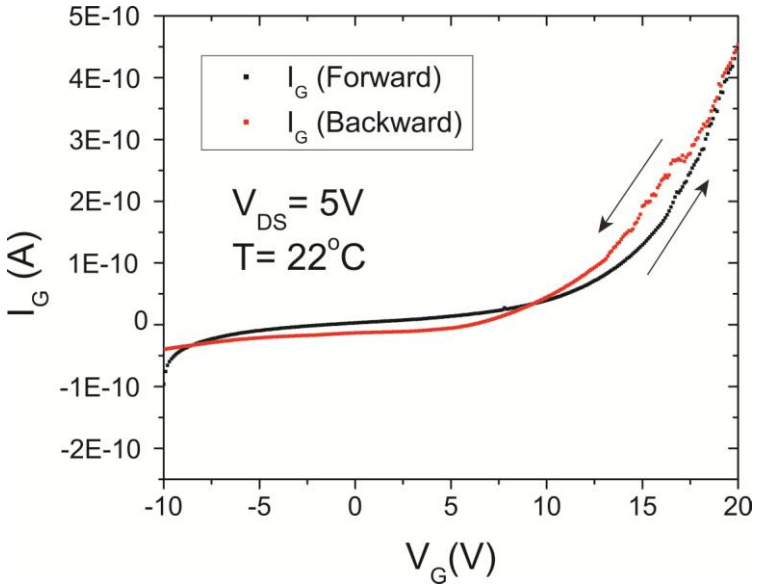


Figure 5.11: ZnO nanoparticle TFT gate leakage current at room temperature ($W = 1000\ \mu m$, $L = 3/2\ \mu m$ Sweep Rate = $2V/s$).

In the output characteristic of TFT shown in Figure 5.12, it is not possible to see a clear saturation in the drain current. This behavior was already reported by Walther (2008), in which the humidity influences the ZnO nanoparticle TFT, neutralizing the surface fields by adsorbed water molecules. Furthermore, a poor contact (large resistance) between the semiconductor and drain/source electrodes is observed in the linear region. One of the possible reasons for the poor contact is the technique (lift-off) chosen to structure the drain and source contacts, in which impurities, i.e. resist residuals, probably form a barrier layer. Although cleaning of the layer surface in organic solvents enhance the contact properties (JAGADISH et al., 2006), the cleaning process cannot be applied, because it has to be performed in presence of the photoresist (after the development), which would harm the resist in turn. Higher drain voltage has not been applied due to the transistors' break down.

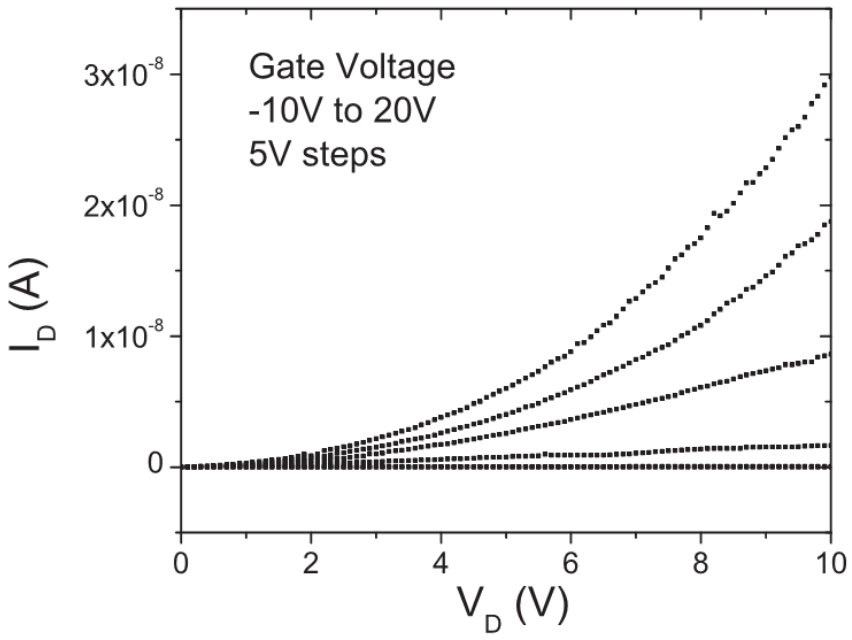


Figure 5.12: Output characteristic of a nanoparticle ZnO TFT ($W = 1000\,\mu m$, $L = 3/2\,\mu m$).

Heating up the transistor using a hot plate resulted in a drastic change in the transfer function of the device, as shown in Figure 5.13. The direction of the hysteresis in the I_D-V_G curve modifies from anti-clockwise to clockwise. This behavior may be attributed to a change in the mechanism dominating the hysteretic characteristic. At lower temperatures, the PVP bulk polarization is the main reason for the hysteresis. Elevating the temperature, the dipoles in the polymer became randomly oriented and/or partially annealed (OLDRAM et al., 2003), resulting in a reduction of its effects upon transistor characteristics. On the other hand, at higher temperatures trap activity may increase. At this point, the dominant phenomenon is the trapping of carries in the nanoparticle and at the gate dielectric interface, mainly caused by the OH- groups. The traps in the surface reduce the gate voltage applied and act as scattering centers for the electron transport, degrading the drain current when the gate voltage is swept backwards (OLDRAM et al., 2003) and (ZUPAC et al., 1993). Moreover, the change in the hysteretic behavior is in accordance with the stress test at higher temperatures, as shown in Figure 5.14. The drain current degradation observed in this case occurred at a higher rate (time constant of, approximately, 17 s) than that observed for a similar test at room temperature.

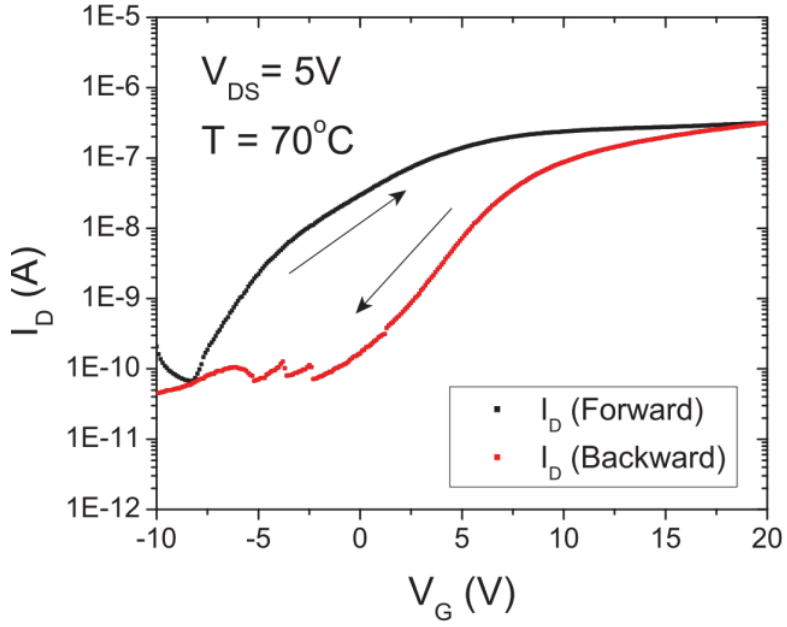


Figure 5.13: ZnO nanoparticle TFT transfer characteristics at 70ºC ($W = 1000\ \mu m$, $L = 3/2\ \mu m$, Sweep Rate = $2\ V/s$).

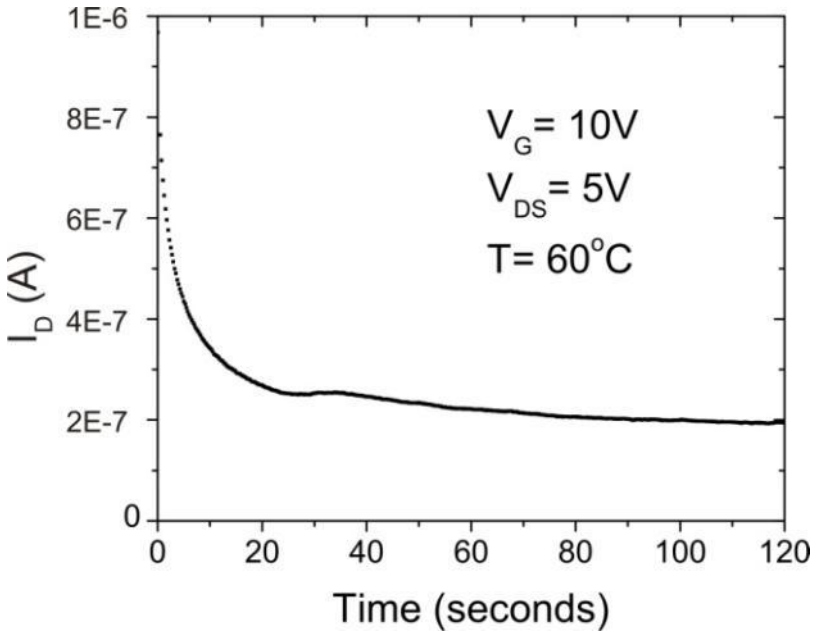


Figure 5.14: Stress test at 60ºC in a ZnO nanoparticle TFT ($W = 1000\ \mu m$, $L = 3/2\ \mu m$, $V_G = 10\ V$, $V_D = 5\ V$).

Considering the stress test at higher temperature shown in Figure 5.14, no discrete current could be noticed. This may be related to the probability of a trap to be active at a determined scenario, to the temperature influence on the release and capture time constant in the transistor, or even to the equipment capability in resolving a faster trap.

Figure 5.15 shows the variation of the threshold voltage as a function of temperature. It is possible to observe that the hysteresis changes its direction at around

55ºC, and that the 'forward' threshold voltage is more sensitive to temperature variations, mainly due to the temperature dependence of charge state of the interface traps. When the transistor is cooled down to room temperature, the hysteresis returns to its initial direction (anti-clockwise).

The I_{on}/I_{off} ratio clearly decreases with increasing temperature, as shown in Figure 5.16. This may also be indirectly observed by comparing Figure 5.3 and Figure 5.13. The off-current in Schottky diodes at the drain and source contact is strongly correlated with the temperature, and the leakage current through the barrier increases (RHODERICK et al., 1988). The on-current decreases because it is affected by the electron trapping at the nanoparticle and the PVP interface.

In Appendix C, there is more information about the characteristic variation under different temperatures, as well as a set of transfer characteristic from several temperatures.

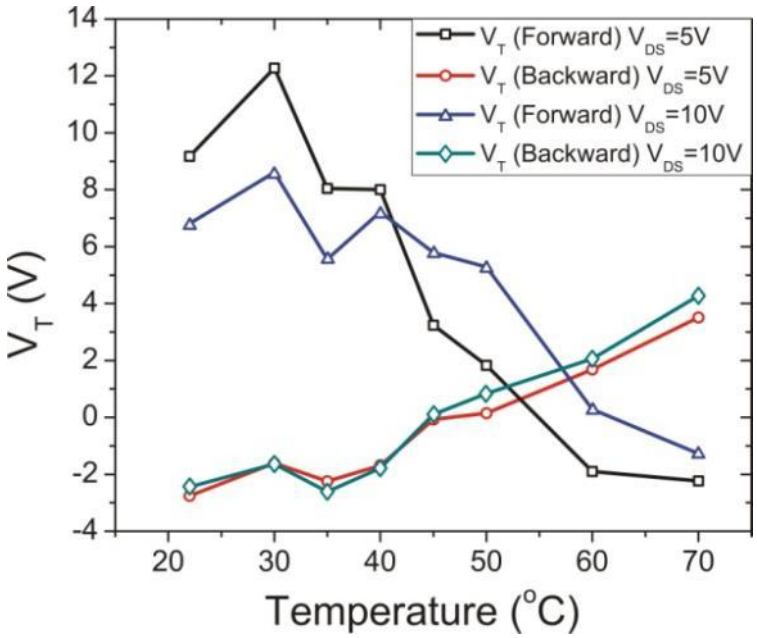


Figure 5.15: Threshold voltage under different temperatures in a ZnO nanoparticle TFT ($W = 1000\ \mu m$, $L = 3/2\ \mu m$, Sweep Rate = $2\ V/s$).

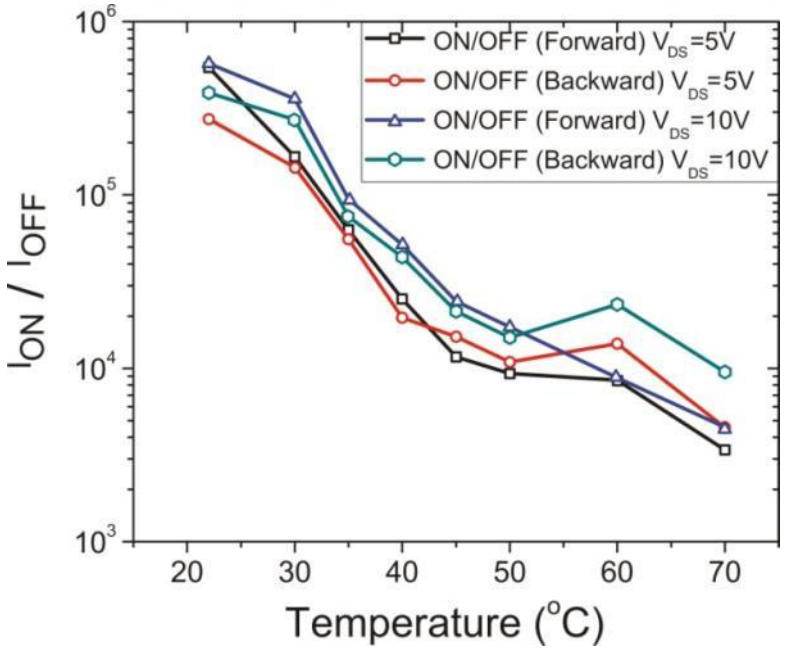


Figure 5.16: I_{on}/I_{off} ratio at different temperatures in a ZnO nanoparticle TFT ($W = 1000\ \mu m$, $L = 3/2\ \mu m$, Sweep Rate = $2V/s$).

The drain voltage also affects the characteristics of ZnO nanoparticle transistors. The threshold voltage dependency on the applied drain voltages is shown in Figure 5.17. At higher drain voltages, the difference between the 'forward' and 'backward' threshold voltage decreases. Furthermore, it is possible to observe that the 'forward' threshold voltage presents a higher dependence upon variation in the drain voltage. This effect is attributed to energy bands tilting and Schottky barrier lowering as a function of the drain voltage, increasing the current in the transistor even in long channel transistor as predicted by (WOLFF et al., 2011-b) and (WOLFF et al. 2010). The 'backward' threshold voltage is almost invariant to the drain voltage since the PVP polarization is the major influence when sweeping the gate voltage backwards. Also, the lateral electric field assists the trapping mechanism at the nanoparticle/PVP interface, enhancing the variation of the 'forward' characteristic.

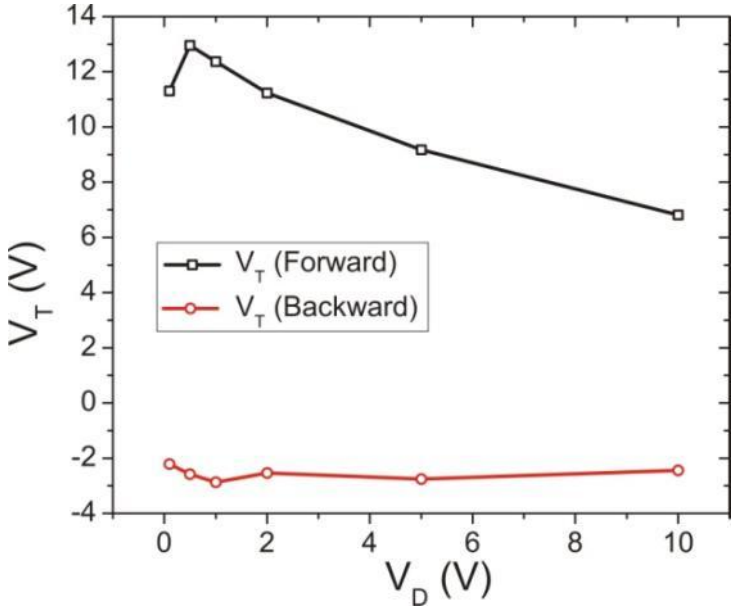


Figure 5.17: Threshold voltage under different drain voltages in a ZnO nanoparticle TFT at room temperature ($W = 1000\ \mu m$, $L = 3/2\ \mu m$, Sweep Rate = $2\ V/s$).

The presence of oxygen traps can also be observed on the SiO_2 gate dielectric based device. The I-V curve depicted in Figure 5.18 was obtained by scanning the gate voltage from -4, 4 to -4V. The anti-clockwise hysteresis observed reinforces the fact that the slow polarization of the PVP bulk is not the only mechanism responsible for the shift in the threshold voltage. The desorption of oxygen molecules increase the concentration of mobile carriers in the nanoparticles, hence increasing the transistor current. Furthermore, this process may explain the hysteresis direction observed in the transistor with silicon dioxide as gate dielectric. Additionally, oxygen vacancies in the nanoparticles can act as mobile charged dopants. By applying an electric field, these dopants drift, causing a hysteretic behavior, as observed in TiO_2-based devices (STRUKOV et al., 2008). Conjointly, this effect was discussed by (WANG et al., 2010) in a memristive device based on ZnO nanocrystals. Oxygen ions close to the Al/ZnO interface drift into the semiconductor bulk or interface depending on the applied bias, increasing or reducing the number of oxygen vacancies and affecting the barrier to electron injection (WANG et al., 2010).

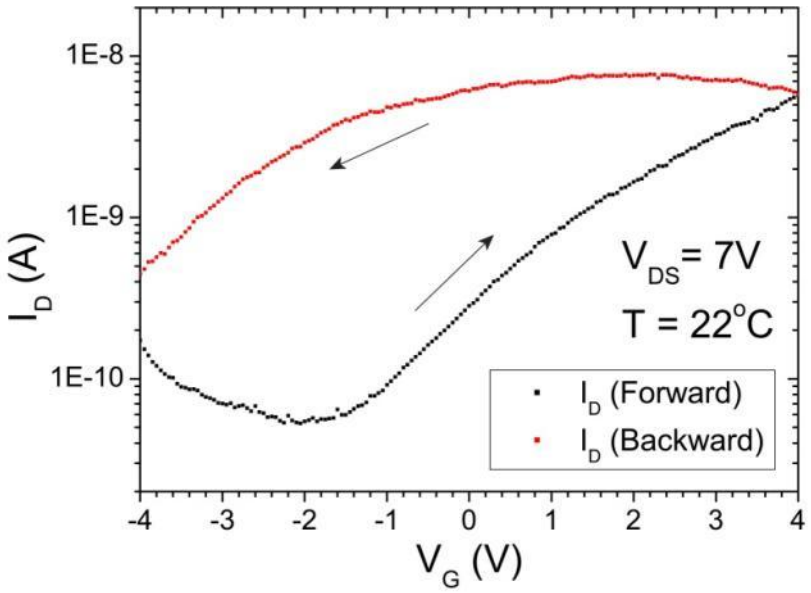


Figure 5.18: Transfer characteristic of ZnO nanoparticle TFT with SiO_2 as gate dielectric at room temperature ($W = 100\ \mu m$, $L = 300\ nm$, Sweep Rate = $2\ V/s$).

Another study (NANDI et al., 2003) shows that a low temperature PECVD-SiO_2 layer presents a higher defect density than in thermally-grown oxides. These defects in the ZnO-film interface are mentioned as the reason for the presence of the hysteresis. Conversely, the anti-clockwise hysteresis presented in the transistor integrated in this work, suggests that the oxygen traps mechanism dominates the traps in the SiO_2 interface, which presents a clockwise hysteretic behavior (NANDI et al., 2003).

The stress test in the SiO_2-based device at room temperature is shown in Figure 5.19. In a first moment, the drain current increases, suggesting desorption of molecular oxygen trapped in the nanoparticulate ZnO surface, as well as supporting the hysteresis direction in the transfer characteristic. On the other hand, subsequently, the drain current decreases, which is attributed to the electron trapping in the gate dielectric (CROSS et al., 2008). This result indicates that desorption of oxygen saturates over time, and the trapping of carries at the SiO_2 interface becomes dominant, reducing the drain current. In addition, this can be used to explain the distinct result found by (NANDI et al., 2008), (THEISSMANN et al., 2011), (BUBEL et al., 2010) and (MEYERS et al., 2008). The reduction of the drain current due to the trapping of carriers at the gate dielectric (SiO_2) interface was also reported by Hwang et al. (2006) in a stress test in an organic based transistor.

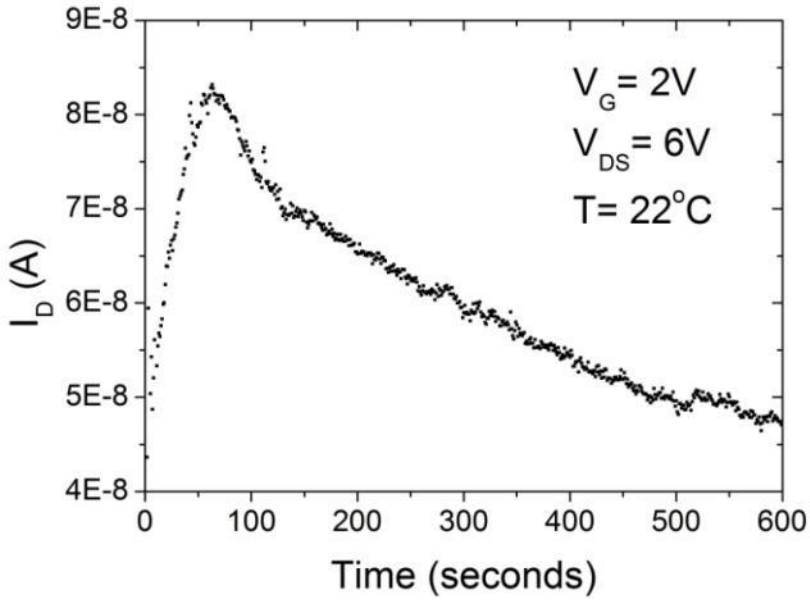


Figure 5.19: Stress test at room temperature in a ZnO nanoparticle TFT and PECVD-SiO_2 as gate dielectric ($W = 100\ \mu m$, $L = 300\ nm$, $V_G = 2\ V$, $V_D = 6\ V$).

Further work regarding environmental conditions is necessary to consolidate the qualitative model proposed in this work, especially tests under different temperatures and atmospheres in the device with PECVD-SiO_2. It was reported, however, by Wang et al. (2010) that under vacuum or nitrogen atmosphere, ZnO nanocrystals did not show any hysteretic behavior due to the absence of oxygen during the device characterization.

The output characteristic of the transistor with PECVD-SiO_2 as gate dielectric is shown in Figure 5.20. In this device, it is possible to observe a saturation regime of the drain current, mainly because of the contact improvement between the semiconductor and the drain/source metal. The threshold voltage, field-effect mobility, I_{on}/I_{off} ratio and sub-threshold voltage slope of the TFT with SiO_2 as gate dielectric is shown in Table 5.2.

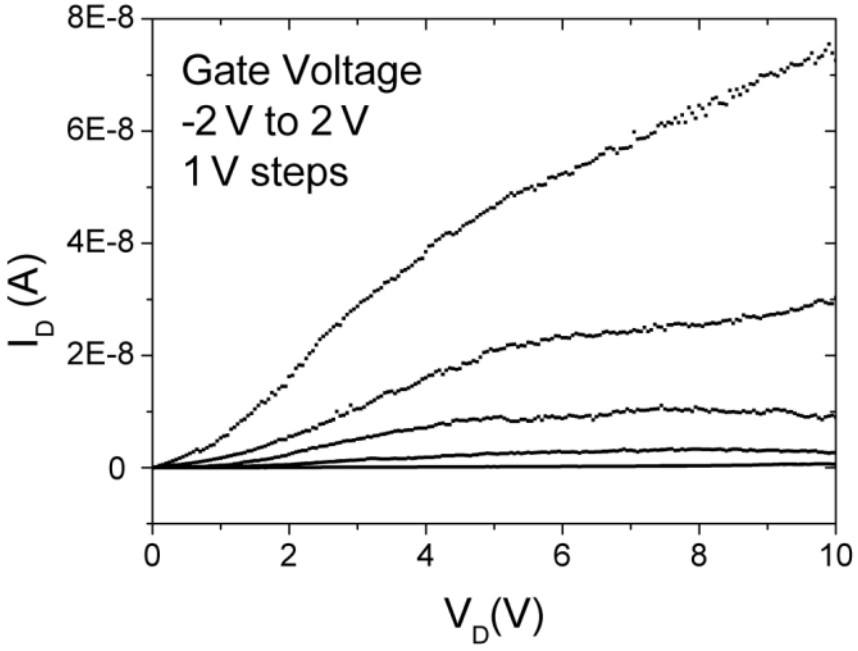


Figure 5.20: Output characteristic of ZnO nanoparticle TFT with SiO_2 as gate dielectric at room temperature ($W = 100\ \mu m$, $L = 300\ nm$, Sweep Rate = $2\ V/s$).

Table 5.2: Electrical characteristics of ZnO nanoparticle TFT with SiO_2 as gate dielectric ($W = 100\ \mu m$ and $L = 300\ nm$) depending on the gate voltage sweeping direction.

	$V_D\ (V)$	$V_T\ (V)$	$\mu_{FE}\ (cm^2/Vs)$	I_{on}/I_{off} ratio	S(V/dec)
Forward sweeping	7	1.66	$2.10 \cdot 10^{-4}$	107	1.90
Backward sweeping	7	−3.54	$2.53 \cdot 10^{-4}$	18	2.07

At the moment, the efforts are focused on evaluating the transistor characteristics in a wider range of temperature, under different atmospheres and additional illumination under ultra-violet (UV) light. Application of a magnetic field may be helpful to evaluate the hysteresis origin; since the polarization of the polymeric dielectric could be done in absence of electric bias.

Unfortunately, the samples used in this work were damaged by destructive tests and affected by aging (degradation over time), hence no other characterization experiment could be performed. There were three attempts to integrate a new set of samples. However, the result was unsuccessful, due to the hydrophobic property of the PVP when the water based solution of ZnO nanoparticle was deposited. In the last couple of months the use of a HMDS atmosphere to improve the deposition of the nanoparticulate ZnO layer was evaluated. Unfortunately, no device was completely and functionally integrated.

Also, an improvement in the drain and source contact resistance with the active semiconductor layer is under research. The technique uses conventional

photolithography and chlorine-RIE (Reactive Ion Etching) to structure the drain/source contact.

And for the last, two different device structures to characterize the hysteresis in the I-V curve of nanoparticulate ZnO based TFT were used. Besides the difference in the transistor dimensions (length and width), a bottom-gate configuration was used for the transistor with PVP as gate dielectric, and a top-gate configuration for the transistor with SiO_2 as dielectric. The change in the structure was mainly due to the fact that during the period of the device integration, the group was focused in the performance of the transistor and it was believed that a smaller structure would be more effective. Conversely, due to integration difficulties (low yield) and performance degradation this approach did not show good prospective and further work is needed to improve the performance and the hysteretic behavior.

6 CONCLUSION

In summary, this work presented the integration process for two kind of nanoparticulate ZnO thin-film transistor, one using PVP as gate dielectric and the other using PECVD-SiO_2 as dielectric. The main goal of the work was the analysis and characterization of the hysteresis in the transfer curve when the gate voltage is swept forward and backward.

Different phenomena that may originate the hysteretic behavior were studied. It was shown that PVP polarization and dielectric interface traps, both caused by the hydroxyl groups and the desorption of oxygen at the surface of the nanoparticle, may lead to the hysteresis observed in the I-V curve. A more extensive study was done in the device with polymeric dielectric, in which the temperature, time stress and drain voltage influence were investigated in detail. In these transistors, the major phenomenon for the hysteresis was attributed to the polymer polarization and traps at the interface.

A drastic change in electrical behavior was observed when the transistor is heated up. The width of the hysteresis depends on the device temperature during the measurement. At room temperature, increasing the applied gate voltage results in a higher threshold voltage and decreasing it leads to a lower threshold voltage. However, increasing the temperature reduces the width, until it completely vanishes at about 55°C. At higher temperatures the hysteresis is inverted, during the incrementation of the gate voltage the threshold voltage is lower than during the decrementation. This influence on the hysteresis direction was attributed to a trade-off between the slow polarization of the PVP and the density of traps at the gate dielectric interface.

The stress tests at different temperature for the transistor with PVP were in agreement with the direction of the hysteresis in the transfer curve and also with the literature, which predicted that the polarization of the PVP is slow (in the order of tens of seconds). Conjointly, the stress test at room temperature has shown discrete current fluctuations that were attributed to the capture and release of carriers by traps at determined percolation paths.

The characterization of the transistors that use SiO_2 as gate dielectric indicated that oxygen traps at the nanoparticle surface also play an important role in the hysteresis. These traps influence the free carrier concentration in the nanoparticulate ZnO film, therefore affecting the device current. In the stress test, it was possible to observe a increase of the drain current at the beginning, followed by a decrease of the current, indicating a saturation of the oxygen desorption and increase of traps at the dielectric interface. This analysis also helps understanding different results reported in the literature.

As future work further studies regarding the hysteresis should be conducted, considering different atmospheres and temperatures or even other transistor structures.

7 FUTURE WORKS

In order to give sequence to this work, some guidelines are given for better understanding the hysteresis origin, to improve the integration process and to enhance the transistor performance:

(a) Transistor electrical characterization under different atmospheres, such as nitrogen, oxygen, hydrogen, vacuum or a lower/higher humidity atmosphere;
(b) Capacitance measurement to investigate the hysteretic behavior, improving the results found for the polarization of the PVP or the traps at the dielectric interface;
(c) Evaluation of other transistor structures and different W/L ratio;
(d) Evaluation of different ZnO nanostructures as the active semiconductor in order to verify the effect of the superficial area on the particle and the interaction with the atmosphere;
(e) Evaluation of different semiconductor layer thickness as researched by (CHUNG et al., 2008) and (LEVIY et al., 2008);
(f) Mathematically model the hysteretic behavior of ZnO nanoparticle TFT considering the transistor geometry and ambient conditions such as temperature and atmosphere;
(g) Another opportunity of further work is the use of a different gate dielectric. Instead of PVP, the use of poly (4-vinyl phenol-co-methyl methacrylate) (PVP-PMMA), as suggested by Kim et al. (2008), which reduces the effects of hydroxyl groups in the polymer bulk;
(h) The concentration of the cross-linker also plays a role in the effect of the hydroxyl group in the PVP bulk, as well as, in the characteristics of the TFTs and should be studied as suggested by Lim et al. (2007);
(i) Evaluation of a passivation layer over the ZnO nanoparticles to isolate the particles from the environment (BUBEL et al., 2010) and (CHANG et al., 2006), on the other hand another step process could increase the process cost;
(j) Since one of the difficulties in the transistors integration was the deposition of the nanoparticles water based solution and the hydrophobic behavior of the PVP surface, for future works, the use of another solvent for the nanoparticles should be explored. As example of the diethylene glycol as Lee et al. (2008) used, however the use of glycol may interfere in the temperature process. Another possibility is the study on the variation of the ZnO nanoparticle concentration in the solution.

PUBLICATIONS BY THE AUTHOR

VIDOR, F.; WIRTH, G. I.; ASSION, F.; WOLFF, K.; HILLERINGMANN, U. Characterization and Modeling of the Hysteresis in ZnO Nanoparticle Thin-Film Transistor. . **IEEE Transactions on Nanotecnology, 2012. Submitted and under revision**

ASSION, F.; HILLERINGMANN, U.; VIDOR, F.; WIRTH, G. I. Electronic Device Integration on Foils Using Semiconductor Nanoparticles. In: Smart Systems Integration, 2012, Zurich. **Proceedings...** Germany: Smart Systems Integration 2012, VDE-Verlag, 2012.

VIDOR, F. F.; WOLFF, K. ; HILLERINGMANN, U. Performance Improvement and Hysteresis Reduction for Printable ZnO-Nanoparticle Thin-Film Transistors. In: Smart Systems Integration Conference, 2011, Dresden. **Proceedings...** Germany: Smart Systems Integration Conference 2011, VDE-Verlag, 2011-a.

VIDOR, F.; WIRTH, G. I.; WOLFF, K.; HILLERINGMANN, U. Study on the Performance Enhancement of ZnO Nanoparticles Thin-Film Transistors. In: ECS TRANSACTIONS - SBMICRO 2011, Joao Pessoa, Brazil. **Proceedings...** USA: The Electrochemical Society (ECS), v. 39. p. 109-115, 2011-b.

HILLERINGMANN, U.; WOLFF, K.; ASSION, F.; VIDOR, F.; WIRTH, G. I. Semiconductor Nanoparticles for Electronic Device Integration on Foils. In: IEEE AFRICON 2011, Livingstone, Zambia. **Proceedings...** USA: IEEE Africon 2011, IEEE, p. 1-6 , 2011.

WOLFF, K.; VIDOR, F; HILLERINGMANN, U. Inverter Circuits Based on Low-Temperature Solution-Processed ZnO Nanoparticle Thin-Film Transistors. In: Nanotech 2011 Conference and Expo, 2011, Boston. **Proceedings...** USA: Nanotechnology 2011: Advanced Materials, CNTs, Particles, Films and Composites, v.1. p. 347-350, 2011-c.

REFERENCES

ASSION, Fabian. **Integration von nanoskaligen Feldeffekttransistoren mit Zinkoxid-Nanopartikeln**. Master Thesis, Universität Paderborn, 2010.

ASSION, F.; WOLFF, K.; HILLERINGMANN, U. Integration von nanoskaligen Feldeffekttransistoren mit Zinkoxid-Nanopartikeln auf Glassubstrat. In: 3rd VDE/VDI/GMM-WORKSHOP **Proceeding...** Mikro-Nano-Integration, Stuttgart, Germany, p. 73 – 78, March 2011.

AXISA, F.; SCHMITT P. M.; GEHIN C.; DELHOMME G.; MCADAMS E.; DITTMAR A. Flexible technologies and smart clothing for citizen medicine, home healthcare and disease prevention. **IEEE Transactions on Information Technology in Biomedicine**, v.9, n.3 p. 325–336, 2005.

BASHIR, A.; WÖBKENBERG, P. H.; SMITH, J.; BALL, J. M.; ADAMAPOULOS, G.; BRADLEY, D. D. C.; ANTHOPOULOS, T. D. High-Performance Zinc Oxide Transistors and Circuits Fabricated by Spray Pyrolysis in Ambient Atmosphere. **Advanced Materials**, v.21, n.21, p. 2226–2231, doi: 10.1002/adma.200803584, Jun. 2009.

BENSON, N.; MELZER, C.; SCHMECHEL, R.; SEGGERN, H. Electronic states at the dielectric/semiconductor interface in organic field effect transistors. **Physica Status Solidi A**, v.205, n.3, p 475-487, doi: 10.1002/pssa.200723421, 2008

BUBEL, S.; MECHAU, N.; HAHN, H.; SCHMECHEL, R. Trap states and space charge limited current in dispersion processed zinc oxide thin films. **Journal Applied Physics**, v.108, p. 124502, doi:10.1063/1.3524184, 2010.

BUBEL, S.; NIKOLOVA, D.; MECHAU, N.; HAHN, H. Influence of stabilizers in ZnO nanodispersions on field-effect transistor device performance. **Journal of Applied Physics**, v.105, n.6, p. 064514-4, 2009.

CARCIA, P. F.; MCLEAN, R. S.; REILLY M. H. High-performance ZnO thin-film transistors on gate dielectrics grown by atomic layer deposition. Applied Physics Letters, v.88, n.12, p. 123509, doi: 10.1063/1.2188379, 2006.

CLARIANT. Datasheet AZ 5214 E Image Reversal Photoresist, p.1-4, 2000.

CHENG, H.C.; CHEN, C. F.; LEE, C. C. Thin-film transistors with active layers of zinc oxide (ZnO) fabricated by low-temperature chemical bath method. **Thin Solid Films**, v.498, n.1-2, p. 142-145, doi: 10.1016/j.tsf.2005.07.101, 2006.

CHOI J. H.;KHANG D. Y.; MYOUNG, J. M. Fabrication and characterization of ZnO nanowire transistors with organic polymer as a dielectric layer. **Solid State Communications**, v.148, n.3-4, p. 126–130, 2008.

COLEMAN, C. C. **Modern Physics for Semiconductor Science**, 1st Ed. Berlin: Wiley-VCH, 2008.

CROSS, R. B. M.; DE SOUZA, M. M. The Effect of Gate-Bias Stress and Temperature on the Performance of ZnO Thin-Film Transistors. **IEEE Transactions on Device and Materials Reliability**, v.8, n.2, p. 277-282, doi: 10.1109/TDMR.2008.916307, 2008.

DA SILVA, R.; WIRTH, G. I.; BREDERLOW, R.; Novel analytical and numerical approach to modeling low-frequency noise in semiconductor devices. **Physica A: Statistical Mechanics and its Applications**, v.362, n.2, Apr. 2006.

DEGUSSA, AG. Datasheet - AdNano Zinc Oxide. **Advanced Nanomaterials**, Hanau, Germany, 2006.

DUPONT. Datasheet Teonex Q83. Hopewell, USA, 2010.

FABER, H.; BURKHARDT, M.; JEDAA, A.; KÄLBLEIN, D.; KLAUK, H.; HALIK, M. Low-temperature solution-processed memory transistors based on zinc oxide nanoparticles. **Advanced Materials**, v.21, n.30, p. 3099–3104, 2009.

FAN, Z.; LU, J. G. Zinc oxide nanostructures: synthesis and properties. **Journal for Nanoscience and Nanotechnology**, v.5, n.10, p. 1561–1573, 2005.

FORTUNATO, E.; PIMENTEL, A.; PEREIRA, L.; GONÇALVES, A.; LAVAREDA, G.; ÁGUAS, H.; FERREIRA, I.; CARVALHO, C.N.; MARTINS, R. High field-effect mobility zinc oxide thin film transistors produced at room temperature. **Journal of Non-Crystalline Solids,** v.338-340, p.806–809, 2004.

GUPTA, D.; YOO, S.; LEE, C.; HONG, Y. Electrical-Stress-Induced Threshold Voltage Instability in Solution-Processed ZnO Thin-Film Transistors: An Experimental and Simulation Study. **IEEE Transactions on Electron Devices**, v.58, n.7, p. 1995 - 2002, doi:10.1109/TED.2011.2138143, 2011.

HILLERINGMANN, U.; WOLFF, K.; ASSION, F.; VIDOR, F.; WIRTH, G. I. Semiconductor Nanoparticles for Electronic Device Integration on Foils. In: IEEE AFRICON 2011. **Proceedings...** Livingstone, Zambia. IEEE Africon 2011. Piscatway, USA : IEEE, 2011. p. 1-6 , 2011.

HIRSCHWALD, W. H. Zinc oxide: an outstanding example of a binary compound semiconductor. **Accounts of Chemical Research**, v.18, n.8, p. 228-234, doi: 10.1021/ar00116a001, 1985.

HOFFMAN, R. L.; NORRIS, B. J.; WAGER, J. F. ZnO-based transparent thin-film transistors. **Physics Letters**, v.82, n.5, p. 733–735, 2003.

HONG, D.; YERUBANDI, G.; CHIANG, H. Q. ; SPIEGELBERG, M. C.; WAGER, J. F. Electrical Modeling of Thin-Film Transistors, **Critical Reviews in Solid State and Materials Sciences**, v.33, n.2, p. 101-132, doi: 10.1080/10408430701384808, 2008.

HORSTMANN, J. T.; HILLERINGMANN, U.; GOSER, K. Characterisation of sub-100 nm-MOS-transistors processed by optical lithography and a sidewall-etchback technique. In: INTERNATIONAL CONFERENCE ON MICRO- AND NANOFABRICATION MNE'95, **Proceedings...** Aix en Provence, France, Microelectronic Engineering 30, pp. 431–434, 1996.

HWANG, D. K.; LEE, K.; KIM, J. H.; IM, S.; PARK, J. H.; KIM, E. Comparative studies on the stability of polymer versus SiO2 gate dielectrics for pentacene thin-film transistors. **Applied Physics Letters**, v.89, p. 093507, 2006.

HWANG, D. K.; OH, M. S.; HWANG, J. M.; KIM, J. H.; IM, S. Hysteresis mechanisms of pentacene thin-film transistors with polymer/oxide bilayer gate dielectrics. **Applied Physics Letters**, v.92, p. 013304, 2008.

IEEE Standard 1620/2008: IEEE Standard for Test Methods for the Characterization of Organic Transistors and Materials. IEEE Computer Society, p.1-20, 2008

JAGADISH, C.; PEARTON, S. **Zinc Oxide Bulk, Thin Film and Nanostructures, Processing, Properties and Applications.** 1st Ed. Elsevier, 2006.

JANOTTI, A.; VAN DE WALLE, C. G. Native point defects in ZnO. **Physical Review B**, v.76, p. 165202, 2007

JIN, Y.; WANG, J.; SUN, B.; BLAKESLEY, J. C.; GREENHAM, N. C. Solution-Processed Ultraviolet Photodetectors Based on Colloidal ZnO Nanoparticles. **Nano Letters**, v.8, n.6, p. 1649-1653, doi: 10.1021/nl0803702, 2008.

JUN, J. H.; PARK, B.; CHO, K.; KIM, S. Flexible TFTs based on solution-processed ZnO nanoparticles. **Nanotechnology**, v.20, p. 505201, doi:10.1088/0957-4484/20/50/505201, 2009.

JUNG, T.; DODABALAPUR, A.; WENZ, R.; MOHAPATRA, S. Moisture induced surface polarization in a poly(4-vinyl phenol) dielectric in an organic thin-film transistor. **Applied Physics Letters**, v.87, p. 182109 , doi:10.1063/1.2117629, 2005.

KACZER, B.; GRASSER, T.; ROUSSEL, P. J.; FRANCO, J.; DEGRAEVE, R.; RAGNARSSON, L.; SIMOEN, E.; GROESENEKEN, G.; REISINGER, H. Origin of NBTI variability in deeply scaled pFETs, **IEEE International Reliability Physics Symposium (IRPS)**, vol.2, no.6, p.26-32, doi: 10.1109/IRPS.2010.5488856, May 2010.

KIM, S. H.; JANG, J.; JEON, H.; YUN, W. M.; NAM, S.; PARK, C. E. Hysteresis-free pentacene field-effect transistors and inverters containing poly(4-vinyl phenol-co-methyl methacrylate) gate dielectrics. **Applied Physics Letters,** v.92, p. 183306, doi:10.1063/1.2924772, 2008.

KONOPKA, Tim. **Integration von dünnschichttransistoren mit zno-nanopartikeln**. Master Thesis, Universität Paderborn, 2010.

LEE, S.; KOO, B.; SHIN, J.; LEE, E.; PARK, H.; KIM, H. Effects of hydroxyl groups in polymeric dielectrics on organic transistor performance. **Applied Physics Letters**, v.88, p. 162109, 2006.

LEE, S.; JEONG, S.; KIM, D.; PARK, B. K.; MOON, J. Fabrication of a solution-processed thin-film transistor using zinc oxide nanoparticles and zinc acetate. **Superlattice and Microstructures**, v.42, n.1-6, p. 361–368, 2007.

LEE, S.; JEONG, S.; LEE, J.; JEON, M.; MOON, J. Solution-processed ZnO nanoparticles-based semiconductor oxide thin-film transistors. **Superlattice and Microstructures**, v.44, n.6, p. 761–769, 2008.

LEE, S.; CHO, H. J.; SON, Y.; LEE, D. S.; SHIN, H. Characterization of oxide traps leading to RTN in high-k and metal gate MOSFETs. IN: ELECTRON DEVICES MEETING (IEDM). **Proceedings...** 2009 IEEE International. doi: 10.1109/IEDM.2009.5424227, 2009.

LEHDE, Christian. **Polymere Gate-Dielektrika für Nanopartikel-Transistoren**. Bachelor Thesis, Universität Paderborn, 2010.

LI, C.; LI, Y.; WU, Y.; ONG, B. S.; LOUTFY, R. O. ZnO field-effect transistors prepared by aqueous solution-growth ZnO crystal thin film. **Journal of Applied Physics**, v.102, n.7, p. 076101, doi: 10.1063/1.2773683, 2007

LIM, S. C.; KIM, S. H.; KOO, J. B.; LEE, J. H.; KU, C. H.; YANG, Y.; ZYUNG, T. Hysteresis of pentacene thin-film transistors and inverters with cross-linked poly(4-vinylphenol) gate dielectrics. **Physics Letters**, v.90, n.17, p. 173512/173512–3, 2007.

LIU, C.; CHEN, C.; LEU, J. Fabrication and CO Sensing Properties of Mesostructured ZnO Gas Sensors. **Journal of Electrochemical Society**, v.156, n.1, p. J16-3, 2009.

MATALAB. MathWorks. Available at: <http://www.mathworks.com>. Visited on: April. 2012.

MEULENKAMP, E. A. Electron Transport in NanoparticulateZnO Films: J. Phys. Chem. B, v.103, n.37, p. 7831–7838, doi: 10.1021/jp9914673, 1999.

MEYERS, S.; ANDERSON, J. T.; HUNG, C. M.; THOMPSON, J.; WAGNER, J. F.; KESZLER, D. A. Aqueous Inorganic Inks for Low-Temperature Fabrication of ZnO TFTs. **Journal of the American Chemical Society**, v.130, n.51, doi:17603-17609, 2008.

MORKOÇ, H.; ÖZGÜR, Ü. **Zinc Oxide: Fundamentals, Materials and Device Technology**. 1st Ed. Weinheim: Wiley, 2009.

MUELLER, H. H.; SCHULZ, M. Random telegraph signal: An atomic probe of the local current in field-effect transistors. J. **Applied Physics**, v.83, p. 1734, doi:10.1063/1.366892, 1998.

NANDI, S. K.; CHATTERJEE, S.; SAMANTA, S. K.; BOSE, P. K.; MAITI, C. K. Electrical characterization of low temperature deposited oxide films on ZnO/n-Si substrate. **Bulletin of Material Science**, v.26, n.7, p. 693–697, 2003.

NISHII, A. O.; OHTANI, K.; OHNO, H.; KAWASAKI M. High-Mobility Field-Effect Transistors Based on Single-Crystalline ZnO Channels. **Japanese Journal Applied Physics,** v.44, p. L1193-L1195, doi: 10.1143/JJAP.44.L1193, 2005.

NOH, S. H.; CHOI1, W.; OH, M. S.; HWANG, D. K.; LEE, K.; IM, S.; JANG, S.; KIM, E. ZnO-based nonvolatile memory thin-film transistors with polymer dielectric/ferroelectric double gate insulators. **Applied Physics Letters**, v.90, n.25, p.253504, doi: 10.1063/1.2749841, 2007.

NORRIS, B. J.; ANDERSON, J.; WAGER, J. F.; KESZLER, D. A. Spin-coated zinc oxide transparent transistors. **Journal of Physics D: Applied Physics**, v.36, n.20, p. L105, doi: 10.1088/0022-3727/36/20/L02, 2003.

OCTAVE. Available at: <http://www.gnu.org/software/octave>. Visited on: April. 2012.

ONG, B. S.; LI, C.; LI, Y.; WU, Y.; LOUTFY, R. Stable, Solution-Processed, High-Mobility ZnO Thin-Film Transistors. **Journal of the American Chemical Society**, v.129, n.10, p. 2750-2751, 2007.

OKAMURA, K.; MECHAU, N.; NIKOLOVA, D.; HAHN, H. Influence of interface roughness on the performance of nanoparticulate zinc oxide field-effect transistors. **Applied Physics Letters,** v.93, p. 083105, doi:10.1063/1.2972121, 2008.

OLDHAM, T. R.; MCLEAN, F. B. Total ionizing dose effects in MOS oxides and devices, **IEEE Transactions on Nuclear Science**, v.50, n.3, p. 483- 499, doi: 10.1109/TNS.2003.812927, Jun. 2003.

PIERRET, R. F. **Semiconductor Device Fundamentals**. 2nd Ed. R. Indiana: Addison Wesley, 1996.

PMCF-m, Poly(melamine-co-formaldehyde) methylated, Datasheet. Available at: <http://www.sigmaaldrich.com>. Visited on: Dec. 2011,

PVP, Poly(4-vinylphenol), Datasheet. Available at: <http://www.sigmaaldrich.com>. Visited on: Dec. 2011,

QIN, L.; CHEN, Q.; CHENG, H.; CHEN, Q.; LI, J.; WANG, Q. Viscosity sensor using ZnO and AlN thin film bulk acoustic resonators with tilted polar c-axis orientations. **Journal of Applied Physics**, v.110, n.9 p. 094511-11, 2011.

RIDEOUT, V. L. A review of the theory, technology and applications of metal-semiconductor rectifiers, **Thin Solid Films**, v. 48, n. 3, pp. 261 - 291, 1978.

RHODERICK, E. H.; WILLIAMS, R. H. **Metal-Semiconductor Contacts.** 2nd Ed. New York: Oxford, 1988.

SCHOTT Technical Glass Solutions GmbH. **Datasheet Schott Borofloat 33**. Jena, Germany, 2010.

SCHRODER, D. K. **Semiconductor Material and Device Characterization**. 3rd Ed. New Jersey: Wiley, 2006.

SENSORIK. Fachgebiet Sensorik. Available at: <http://sensorik.uni-paderborn.de>. Visited on: Mar. 2012.

SILVA, R; WIRTH, G. I.; BREDERLOW, R. Novel analytical and numerical approach to modeling low-frequency noise in semiconductor devices, **Physica A: Statistical Mechanics and its Applications**, v.362, n.2, April 2006.

STRUKOV, D. B.; SNIDER, G. S.; STEWART, D. R.; WILLIAMS, R. S. The missing memristor found. **Nature**, v.453, p. 80-83, doi:10.1038/nature06932, May 2008.

SUN, B.; SIRRINGHAUS, H. Solution-Processed Zinc Oxide Field-Effect Transistors Based on Self-Assembly of Colloidal Nanorods. **Nano Letters**, v.5, n.12, p. 2408-2413, doi: 10.1021/nl051586w, 2005.

SUN, B.; PETERSON, R. L.; SIRRINGHAUS, H. Low-Temperature Sintering of In-Plane Self-Assembled ZnO Nanorods for Solution-Processed High-Performance Thin Film Transistors. **The Journal of Phisical chemistry C Letters**, v.111, n.51, p.18832, doi: 10.1021/jp077740f, 2007.

SZE, S. M.; NG K. K.**Physics of Semiconductor Devices**, 3rd Ed, New Jersey: Wiley-Interscience, 2006.

THEISSMANN, R.; BUBEL, S.; SANLIALP, M.; BUSCH, C.; SCHIERNING, G.; SCHMECHEL, R. High performance low temperature solution-processed zinc oxide thin film transistor. **Thin Solid Films**, v.519, n.16, p. 5623-5628, doi:10.1016/j.tsf.2011.02.073, Jun. 2011.

UPPALAPATI, S.; CHADA, S.; ENGELHARD, M. H.; YAN, M. Photochemical reactions of poly(4-vinylphenol) thin films. **Macromolecular**, v.21, n.4, p. 461–470, 2010.

VAN DE WALLE, C. G. Hydrogen as a Cause of Doping in Zinc Oxide. **Physical Review Letters**, v.85, n.5, p. 1012, Jul. 2000.

VERBAKEL, F.; MESKERS, S. C. J.; JANSSEN, R. A. J. Electronic memory effects in diodes from a zinc oxide nanoparticle-polystyrene hybrid material. **Applied Physics Letters**, v.89, p. 102103, doi:10.1063/1.2345612, 2006.

VERBAKEL, F.; MESKERS, S. C. J.; JANSSEN, R. A. J. Electronic memory effects in diodes of zinc oxide nanoparticles in a matrix of polystyrene or poly(3-hexylthiophene). **Applied Physics**, v.102, p. 083701, doi:10.1063/1.2794475, 2007.

VERBAKEL, F.; MESKERS, S. C. J.; JANSSEN, R. A. J. Surface Modification of Zinc Oxide Nanoparticles Influences the Electronic Memory Effects in ZnO−Polystyrene Diodes. **The Journal of Physical Chemistry C**, v.111, n.28, p. 10150-10153. doi: 10.1021/jp072999j, 2007.

VERES, J.; OGIER, S.; LLOYD, G.; LEEUW, D. Gate Insulators in Organic Field-Effect Transistors. **Chemistry of Materials**, v.16, n.23, p. 4543-4555, doi: 10.1021/cm049598q, 2004.

VICCA, P.; STEUDEL, S.; SMOUT, S.; RAATS, A.; GENOE, J.; HEREMANS, P. A low-temperature-cross-linked poly(4-vinylphenol) gate-dielectric for organic thin film transistors. **Thin Solid Films**, v.519 n.1, p. 391–393, 2010.

VIDOR, F. F.; WOLFF, K. ; HILLERINGMANN, U. . Performance Improvement and Hysteresis Reduction for Printable ZnO-Nanoparticle Thin-Film Transistors. In: Smart Systems Integration Conference, 2011, Dresden. **Proceedings...** Germany: Smart Systems Integration Conference 2011: VDE-Verlag, 2011-a.

VIDOR, F.; WIRTH, G. I.; WOLFF, K.; HILLERINGMANN, U. Study on the Performance Enhancement of ZnO Nanoparticles Thin-Film Transistors. In: ECS TRANSACTIONS - SBMICRO 2011, Joao Pessoa, Brazil. **Proceedings...** USA : The Electrochemical Society (ECS), v. 39. p. 109-115, 2011-b.

VOLKMAN, S. K.; MATTIS, B. A.; MOLESA, S. E.; LEE, J. B.; VORNBROCK, A. F.; BAKHISHEV, T.; SUBRAMANIAN, V. A novel transparent air-stable printable n-type semiconductor technology using ZnO nanoparticles. In: Electron Devices Meeting, 2004. **Proceedings...** USA: IEDM Technical Digest. IEEE International, p.769-772, doi: 10.1109/IEDM.2004.1419287, 2004.

XU, J.; PAN, Q.; SHUN Y.; TIAN, Z. Grain size control and gas sensing properties of ZnO gas sensor. **Sensors and Actuators B: Chemical**, v.66, n.1–3, p.277-279, doi.10.1016/S0925-4005(00)00381-6, Jul. 2000.

WALTHER, S.; SCHÄFER, S.; JANK, M. P. M.; THIEM, H.; PEUKERT, W.; FREY, L.; RYSSEL, H. Influence of annealing temperature and measurement ambient on TFTs based on gas phase synthesized ZnO nanoparticles. **Microelectronic Engineering**, v.87, n.11, p. 2312-2316, doi:10.1016/j.mee.2010.03.009, Nov. 2010.

WANG, J.; SUN, B.; GAO, F.; GREENHAM, N. C.; Memristive devices based on solution-processed ZnO nanocrystals. **Physica Status Solidi A,** v.207, n.2, p. 484–487, doi:10.1002/pssa.200925467, 2010.

WANG, Z. L. Zinc oxide nanostructures: growth, properties and applications. **Journal of Physics: Condensed Matter**, v.16, n.25, p. R829–R858, 2004.

WILLIAMS, K. R.; GUPTA, K.; WASILIK, M. Etch rates for micromachining processing - part II. **Journal of Microelectromechanical Systems**, v.12, n.6, p. 761–778, 2003.

WOLFF, K.; HILLERINGMANN, U. N-type Single Nanoparticle ZnO Transistor Processed at Low Temperatures, IN: PROCEEDINGS OF THE 39th EUROPEAN SOLID STATE DEVICE RESEARCH CONFERENCE. **Proceedings...** ESSDERC, p. 460 – 463, 2009.

WOLFF, K.; HILLERINGMANN, U. Analysis and Modeling of Pseudo-Short-Channel Effects in ZnO-Nanoparticle Thin-Film Transistors, IN: PROCEEDINGS OF THE 40th EUROPEAN SOLID STATE DEVICE RESEARCH CONFERENCE. **Proceedings...** ESSDERC, p. 226 – 229, 2010.

WOLFF, K. ; HILLERINGMANN, U. Integration Techique for Optically Transparent ZnO Nanoparticle Thin-film Transistors. In: Smart Systems Integration Conference, 2011, Dresden. Proceedings... Germany: Smart Systems Integration Conference 2011: VDE-Verlag, 2011-a.

WOLFF, K.; HILLERINGMANN, U. Solution processed inverter based on zinc oxide nanoparticle thin-film transistors with poly(4-vinylphenol) gate dielectric. **Solid-State Electronics,** v.62, p. 110-114, doi:10.1016/j.sse.2011.01.046, 2011-b.

WOLFF, K.; VIDOR, F; HILLERINGMANN, U. Inverter Circuits Based on Low-Temperature Solution-Processed ZnO Nanoparticle Thin-Film Transistors. In: Nanotech 2011 Conference and Expo, 2011, Boston. **Proceedings...** USA: Nanotechnology 2011: Advanced Materials, CNTs, Particles, Films and Composites, v.1. p. 347-350, 2011-c.

WONG, W. S.; SALLEO, A. **Flexible Electronics: Materials and Applications**. 1st Ed. New York: Springer, 2009.

XU, J.; PAN, Q.; SHUN, Y.; TIAN, Z. Grain size control and gas sensing properties of ZnO gas sensor. **Sensors and Actuators B: Chemical**, v.66 n.1–3, p. 277-279, 2000.

ZUPAC, D.; GALLOWAY, K. F.; KHOSROPOUR, P.; ANDERSON, S. R.; SCHRIMPF, R. D.; CALVEL, P. Separation of effects of oxide-trapped charge and interface-trapped charge on mobility in irradiated power MOSFETs, **IEEE Transactions on Nuclear Science**, v.40, n.6, p. 1307-1315, doi: 10.1109/23.273537, Dec. 1993.

APPENDIX A CLEANING PROCESSES

Cleaning A process:

• Ultrasonic bath for 10 minutes in a NCW-1001 (a kind of detergent) based solution;

• Deionized water bath for 1+1+3 minutes ("+" means to completely change the water);

• Etching solution (H_2O_2 and H_2SO_4) for 10 minutes at 80ºC;

• Deionized water bath for 1+1+3 minutes;

• Drying process.

Cleaning C process:

• Oxygen plasma for 2 minutes;

• Acetone bath for 2 minutes;

• Deionized water bath for 1+1+3 minutes;

• Ultrasonic bath for 10 minutes in a NCW-1001 based solution;

• Deionized water bath for 1+1+3 minutes;

• Isopropanol bath for 5 minutes;

• Deionized water bath for 1 minute;

• Drying process.

APPENDIX B MEASUREMENT METHODS

This section shows the measurement methods used to characterize the transistors. The background theory will be shown briefly. The most interesting and important characteristics are the threshold voltage, the field-effect mobility, the I_{on}/I_{off} ratio and the subthreshold voltage slope. The data were extracted using a 4156A - Precision semiconductor parameter analyzer.

B.1Threshold Voltage

The threshold voltage (V_T) is commonly defined as the transistor turn-on voltage. However, due to the non-linear nature of the drain current curve, the threshold voltage is not uniquely defined, because there is not a single gate voltage at which the current starts to "flow". There are several methods to extract the threshold voltage, as explained by Schroder (2006). Three of these methods will be presented here, namely, linear extrapolation, subthreshold drain current and transconductance derivative. Figure B.1 shows the different values extracted in each technique in a modeled MOSFET; $L = 1.5\ \mu m$, $t_{ins} = 25\ nm$, and $V_D = 0.1\ V$.

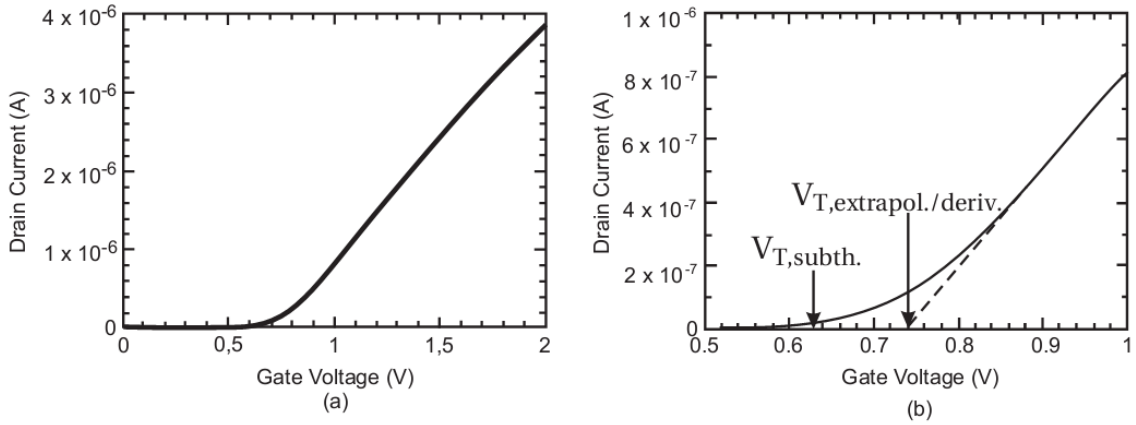


Figure B.1: (a) $I_D - V_{GS}$ curve of a MOSFET near the threshold voltage; (b) enlarged zoom-in of (a). Adapted from (SCHRODER, 2006).

B.1.1 Linear Extrapolation

The linear extrapolation is an easy method to obtain the threshold voltage. It consists on measuring the drain current as the function of the gate voltage sweep. Eq. 4.1

presents the drain current of $V_{GS} = V_T + 0.5V_{DS}$ as zero. However, this equation is only valid above the threshold voltage, so the current is not zero and just an asymptotically approach.

In order to extract the threshold voltage, the ID versus VGS curve is extrapolated to $I_D = 0$. By using Eq. B.1, it is possible to determine the threshold voltage.

$$V_T = V_{GS,extrapolated} - \frac{V_{DS}}{2} \tag{B.1}$$

However, Eq. B.1 is only valid for negligible series resistance, and it is normally low enough not to affect the threshold voltage extraction. Due to the subthreshold current (below V_T), the series resistance and the mobility degradation effect (above V_T), the $I_D - V_{GS}$ curve does not follow a straight line. In order to avoid these issues, it is necessary to find the point in the curve with maximum transconductance to extrapolate and find the intersection with $I_D = 0$. Summing up, this method is sensitive to series resistance and mobility degradation.

B.1.2. Subthreshold Drain Current

The subthreshold method uses the drain current versus the gate voltage function in a semilog plot ($\log(I_D)$ versus V_{GS}). In this scale, the subthreshold drain current varies linearly with gate voltage. The gate voltage from which the linear current departs is taken as the threshold voltage. However, this value is normally lower than the linear extrapolation one.

Figure B.1 shows the values extracted from the threshold voltage using both techniques: subthreshold drain current and linear extrapolation. It is observed a difference in the drain current at the extracted threshold voltage for each technique.

B.1.3. Transconductance Derivative

The transconductance derivative method is based on the ideal MOSFET, in which the drain current is zero for $V_{GS} < V_T$ and proportional to the gate voltage for $V_{GS} > V_T$. The first derivative ($\partial I_D / \partial V_{GS}$) is a step function, and the second derivative ($\partial^2 I_D / \partial V_{GS}^2$) tends to infinite at gate voltage equals the threshold voltage. In a real transistor, the second derivative is not infinite, however a maximum is observed. The threshold voltage extracted is very similar to the one extracted with the linear extrapolation.

B.2 Threshold Voltage - Practice

Previously, it was presented three techniques to extract the threshold voltage. The linear extrapolation was the method chosen, due to the quick and reliable extraction of V_T. Even though the transconductance derivative method has positive aspects, when working with scripts in some mathematical software, as Matlab (2012) or Octave (2012), when the second derivative is applied, it is hard to identify the maximum point in the curve because of the noise present in the data. The subthreshold method was not

chosen because the point in the ZnO nanoparticle TFT from which the linear current slope departs is not accurately determined, adding a considerable error in the extraction of the threshold voltage.

B.3 Field Effect Mobility

Normally, the field effect mobility is cited as an important performance metric to compare different devices. The mobility influences the frequency or time response in two different ways. First, at low electric field, the carrier velocity is proportional to the mobility. And higher mobility means higher frequency, once carriers need less time to travel through the device. Second, higher mobility devices present higher current, so the capacitances are charged faster, resulting in higher frequency response.

As explained by Schroder (2006), the field effect mobility is determined from the transconductance, defined as:

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=constant} \tag{B.2}$$

The drain current defined in Eq. 4.1 can be reduced to Eq. B.3, when the drain voltage is small ($V_{DS} << V_{GS} - V_T$).

$$I_D = \frac{\mu_{FE} C_{ins} W}{L}(V_{GS} - V_T)V_{DS} \tag{B.3}$$

When the field effect mobility is determined, the transconductance is usually taken as:

$$g_m = \frac{W}{L}\mu_{FE} C_{ins} V_{DS} \tag{B.4}$$

The field effect mobility is extracted using Eq. B.5, obtained when Eq. B.4 is solved for the mobility.

$$\mu_{FE} = \frac{L g_m}{W C_{ins} V_{DS}} \qquad ; C_{ins} = \frac{\varepsilon_o \varepsilon_r}{t_{ins}} \tag{B.5}$$

This method is the same indicated in the IEEE standard 1620 (2008), where the mobility value of the majority carriers of semiconductor material is reported in $cm^2/(Vs)$; and derived from transfer characteristic of the device.

B.4 Subthreshold Voltage Slope

For gate voltages lower than the threshold voltage, the current is supposed to be zero, as predicted in Eq. 4.1. However, this equation does not correctly represent the drain current in the subthreshold region. At this point, the current power-law

dependence makes a transition to an exponential dependence (WONG et al., 2009). The standard drain current equation in the subthreshold region is:

$$I_D = \frac{W}{L} K \mu_{FE} C_{ins} \left(1 - e^{-\frac{qV_{DS}}{K_B T}}\right) e^{\frac{qV_{GS}}{nK_B T}} \quad \text{(B.6)}$$

where K is a constant that depends on the material and the structure of the device, n is the ideality factor ($n \geq 1$), K_B is Boltzmann's constant and T is the absolute temperature.

The subthreshold voltage slope determines the voltage excursion below the threshold voltage to switch the transistor fully on or off. In practical terms, a high subthreshold voltage slope is the desired, which requires less gate voltage excursion for turning the transistor into fully off to fully on, or vice-versa, (WONG et al., 2009).

B.5. Subthreshold Voltage Slope - Practice

The subthreshold region is easily observed using a logarithmic scale ($\log(I_D)$ versus V_{GS}), in which the drain current is represented by a straight line. The subthreshold voltage slope is commonly expressed as Eq. B.7, and the typical unit used is volts/decade, representing the increment in gate voltage needed to change the drain current by a factor of 10.

$$S = \frac{\partial log I_D}{\partial V_{GS}} \quad \text{(B.7)}$$

At the low end, the subthreshold characteristic smoothly merges into a leakage current one, and in the upper end it turns into the saturation, as shown in Figure B.2. For experimental analyses, the maximum slope extracted from the transfer curve is reported, analogous to the mobility in the region above the threshold voltage. For a nearly ideal subthreshold region, i.e., the ideality factor from Eq. B.6 is very close to the unit, and values of 60 mV/decade at 300 K are achieved for crystalline Si-based devices (WONG et al., 2009).

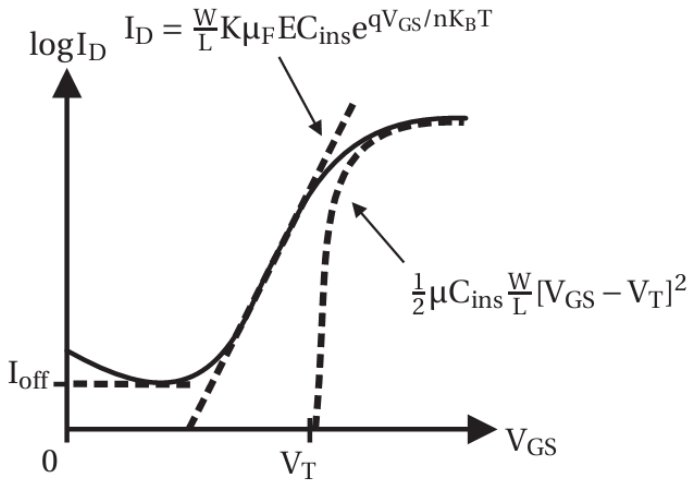


Figure B.2: Transfer characteristic of a MOSFET exhibiting an exponential dependence below V_T. As V_{GS} is later reduced, the exponential characteristic merges with the leakage current. Adapted from (WONG et al., 2009)

B.6 I_{on}/I_{off} Ratio

The I_{on}/I_{off} ratio is normally reported as the ratio between the maximum and the minimum drain current extracted from the transfer characteristic. Figure B.3 shows the extracted drain current from a semilog plot (log(I_D) versus V_{GS}).

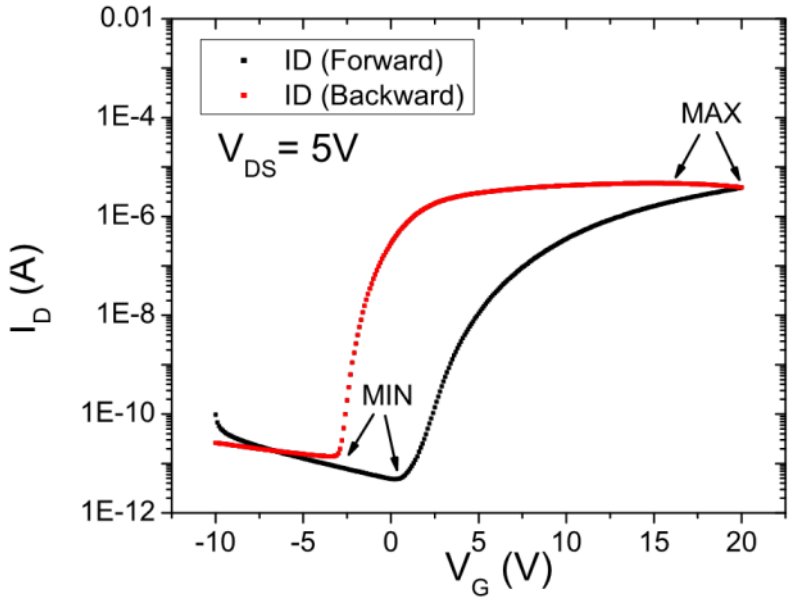


Figure B.3: The maximum and the minimum drain current of a ZnO nanoparticle TFT in a semi-log scale.

APPENDIX C GRAPHICS AND TABLES

This appendix presents some graphics and tables not shown in the text:

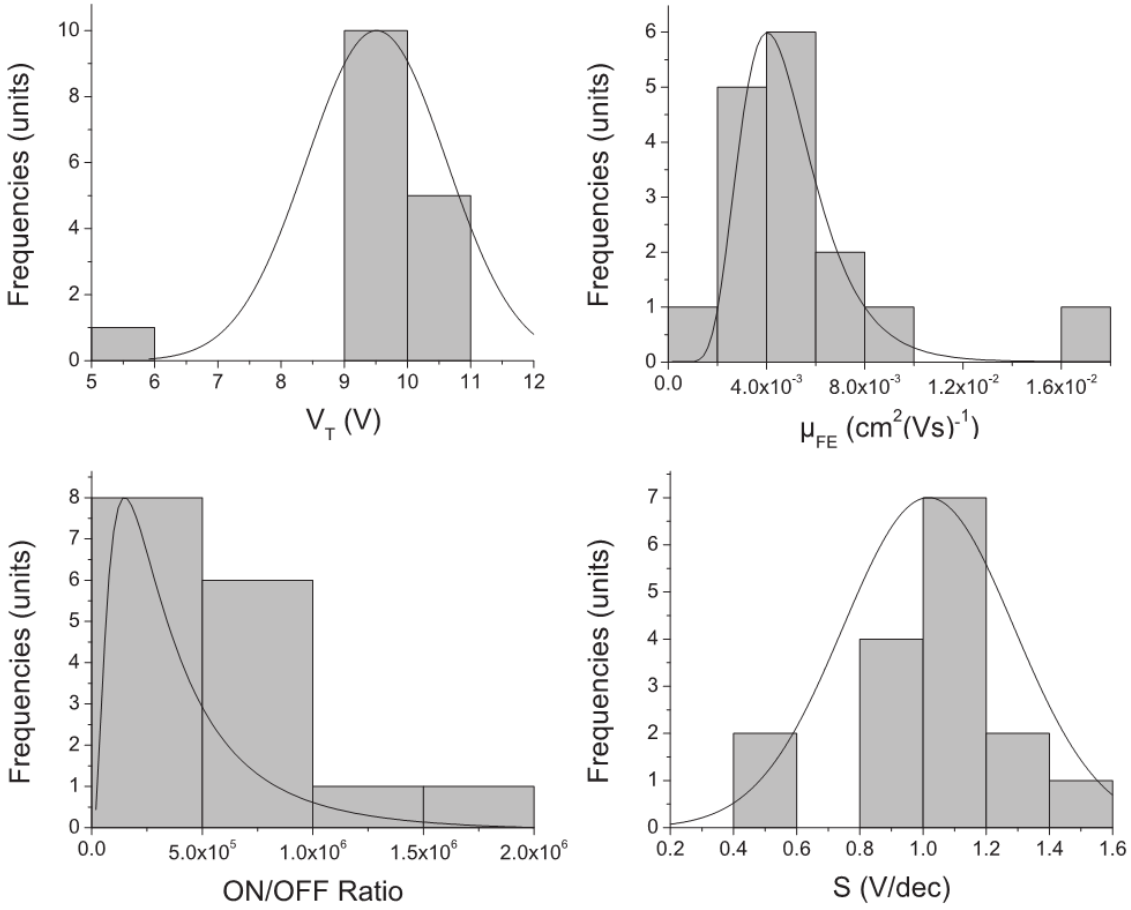


Figure C.1: Distribution of the 'forward' characteristics of ZnO nanoparticle TFT ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$).

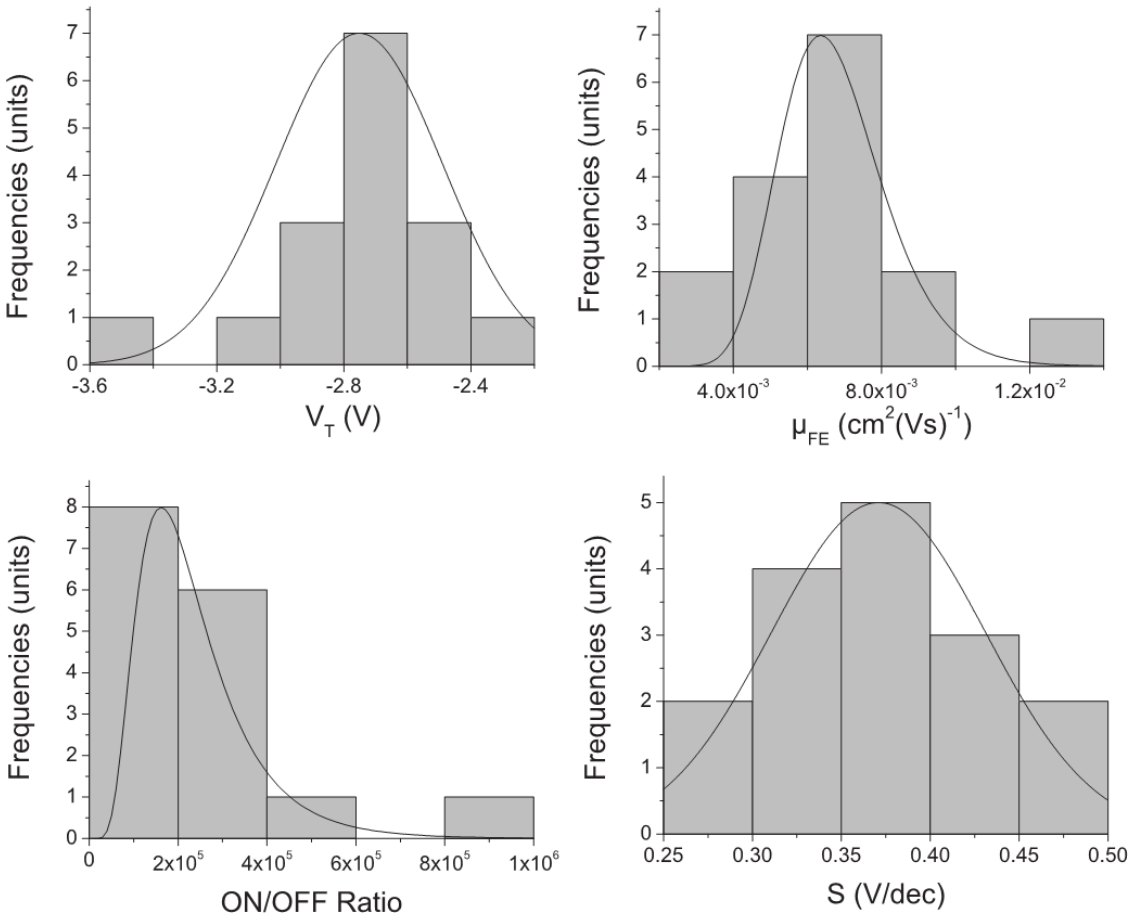


Figure C.2: Distribution of the 'backward' characteristics of ZnO nanoparticle TFT ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$).

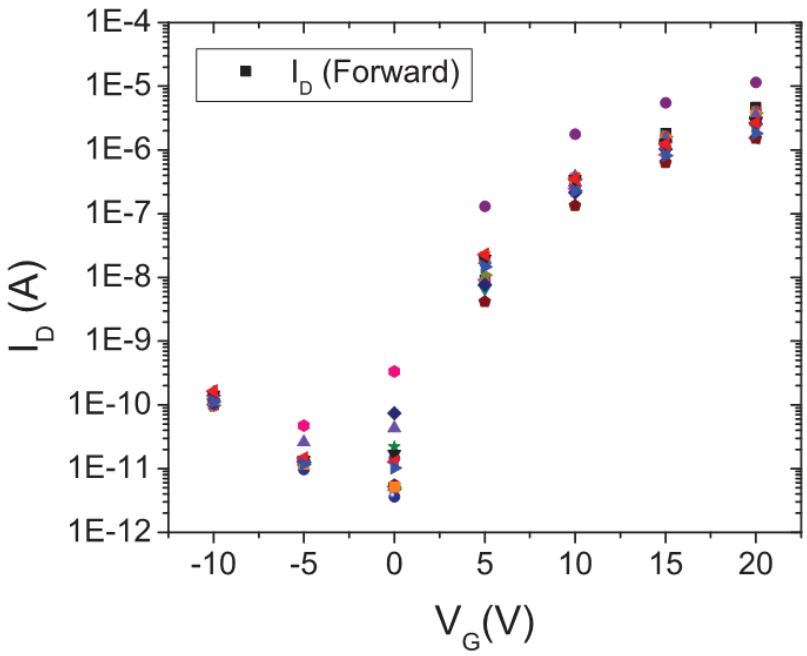


Figure C.3: Current level over samples of ZnO nanoparticle TFT ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$) while sweeping the gate voltage forwards.

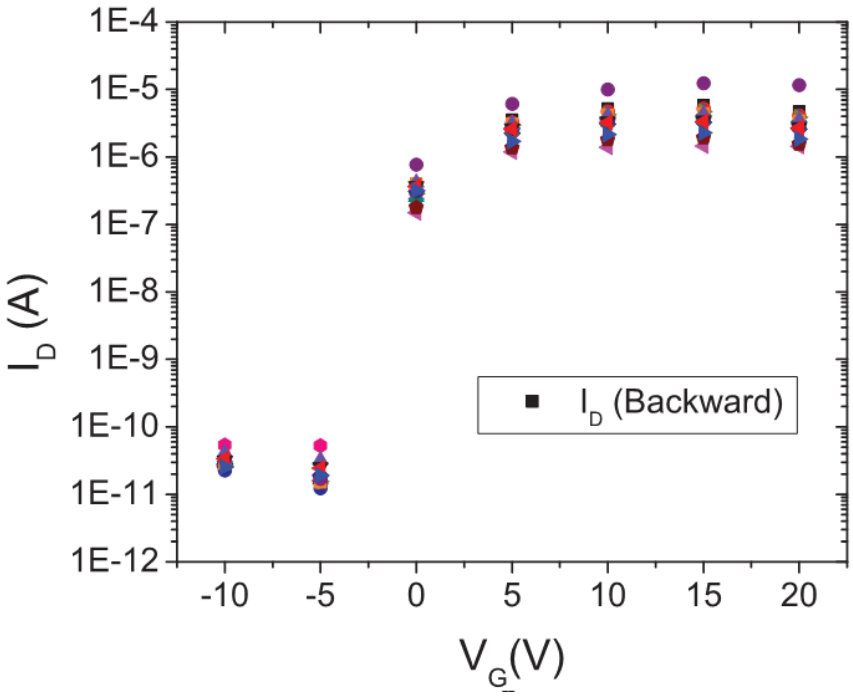


Figure C.4: Current level over samples of ZnO nanoparticle TFT ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$) while sweeping the gate voltage backwards.

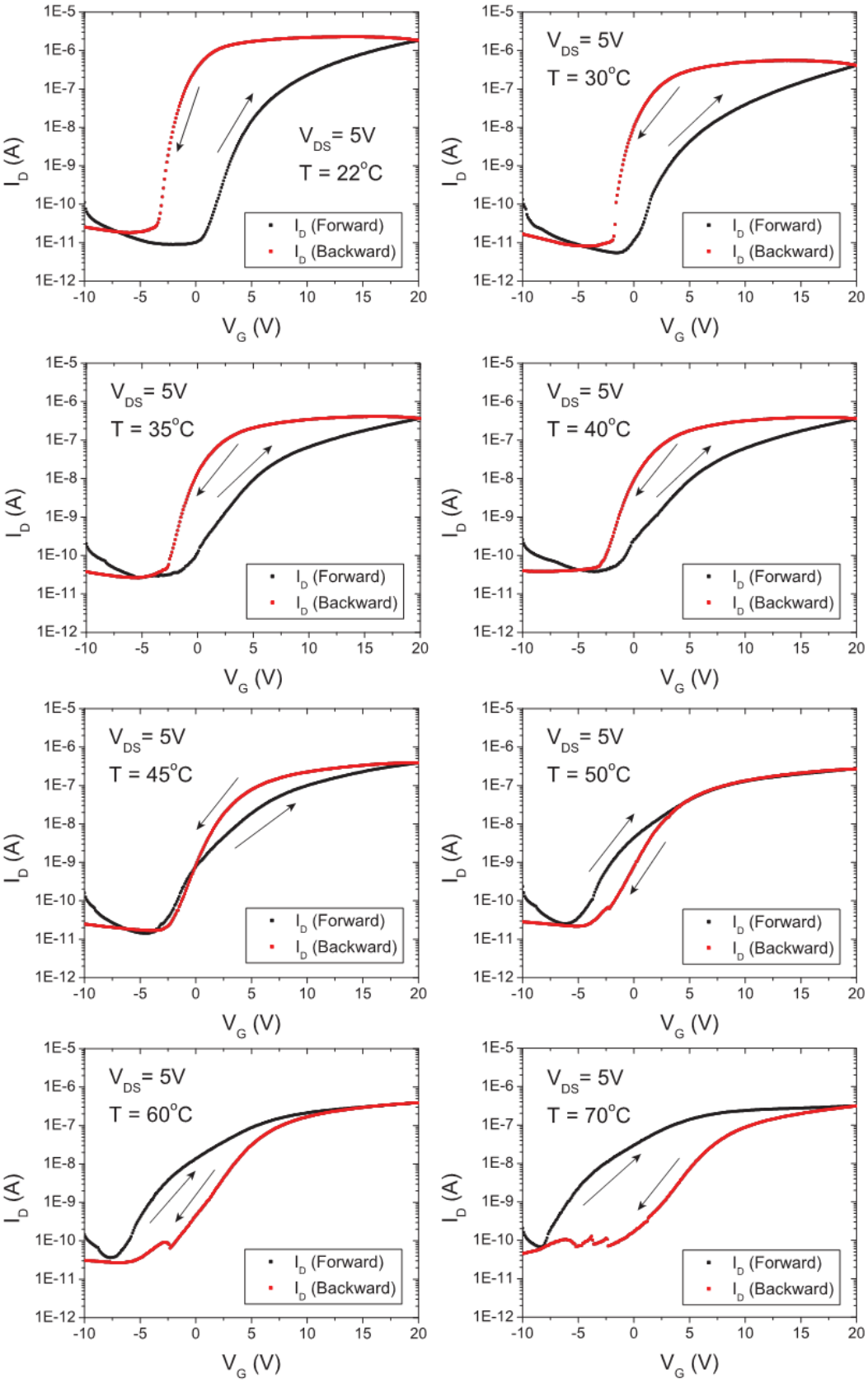


Figure C.5: Transfer characteristics of ZnO nanoparticle TFT ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$) with different temperatures.

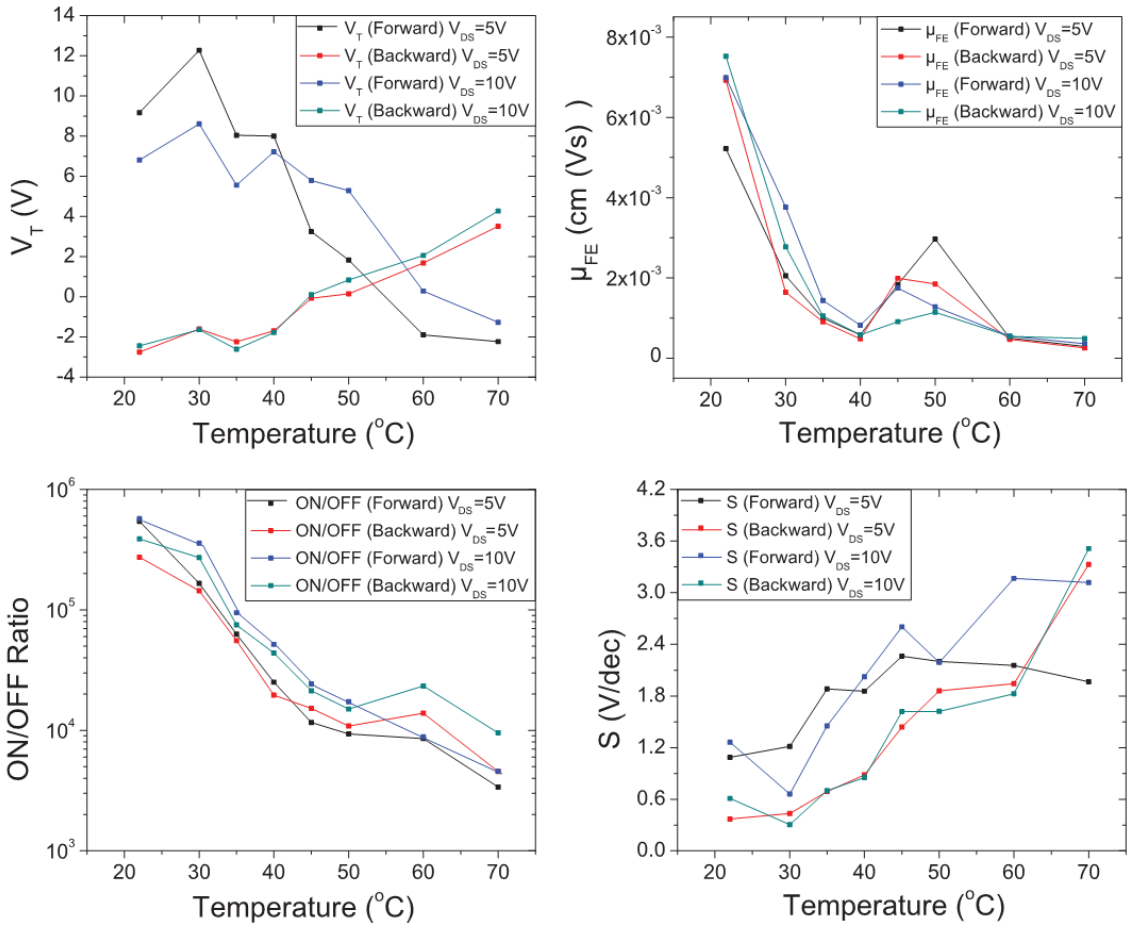


Figure C.6: Characteristics variation under different temperatures on ZnO nanoparticle TFT ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$).

Table C.1: Temperature dependency in the electrical characteristics of ZnO nanoparticle ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$) when sweeping forward V_G and $V_D = 5\ V$.

$T\ (°C)$	$V_T\ (V)$	$\mu_{FE}\ (cm^2/Vs)$	I_{on}/I_{off} ratio	S(V/dec)
22	9.17	$5.21 \cdot 10^{-3}$	$5.43 \cdot 10^{5}$	1.08
30	12.28	$2.05 \cdot 10^{-3}$	$1.66 \cdot 10^{5}$	1.21
35	8.05	$9.96 \cdot 10^{-4}$	$6.29 \cdot 10^{4}$	1.88
40	8.01	$5.78 \cdot 10^{-4}$	$2.50 \cdot 10^{4}$	1.85
45	3.23	$1.83 \cdot 10^{-3}$	$1.16 \cdot 10^{4}$	2.26
50	1.82	$2.96 \cdot 10^{-3}$	$9.31 \cdot 10^{3}$	2.20
60	-1.91	$5.04 \cdot 10^{-4}$	$8.53 \cdot 10^{3}$	2.15
70	-2.23	$2.92 \cdot 10^{-4}$	$3.38 \cdot 10^{3}$	1.96

Table C.2: Temperature dependency in the electrical characteristics of ZnO nanoparticle ($W = 1000\,\mu m$ and $L = 3/2\,\mu m$) when sweeping backward V_G and $V_D = 5\,V$.

$T\,(°C)$	$V_T\,(V)$	$\mu_{FE}\,(cm^2/Vs)$	I_{on}/I_{off} ratio	S(V/dec)
22	-2.75	$6.92 \cdot 10^{-3}$	$2.74 \cdot 10^{5}$	0.37
30	-1.61	$1.64 \cdot 10^{-3}$	$1.44 \cdot 10^{5}$	0.43
35	-2.24	$9.07 \cdot 10^{-4}$	$5.56 \cdot 10^{4}$	0.68
40	-1.69	$4.80 \cdot 10^{-4}$	$1.95 \cdot 10^{4}$	0.88
45	-0.07	$1.98 \cdot 10^{-3}$	$1.52 \cdot 10^{4}$	1.43
50	0.14	$1.85 \cdot 10^{-3}$	$1.08 \cdot 10^{4}$	1.85
60	1.68	$4.69 \cdot 10^{-4}$	$1.38 \cdot 10^{4}$	1.94
70	3.51	$2.58 \cdot 10^{-4}$	$4.55 \cdot 10^{3}$	3.33

Table C.3: Temperature dependency in the electrical characteristics of ZnO nanoparticle ($W = 1000\,\mu m$ and $L = 3/2\,\mu m$) when sweeping forward V_G and $V_D = 10\,V$.

$T\,(°C)$	$V_T\,(V)$	$\mu_{FE}\,(cm^2/Vs)$	I_{on}/I_{off} ratio	S(V/dec)
22	6.81	$6.99 \cdot 10^{-3}$	$5.73 \cdot 10^{5}$	1.26
30	8.61	$3.76 \cdot 10^{-3}$	$3.58 \cdot 10^{5}$	0.60
35	5.56	$1.43 \cdot 10^{-3}$	$9.48 \cdot 10^{4}$	1.45
40	7.22	$8.21 \cdot 10^{-4}$	$5.15 \cdot 10^{4}$	2.02
45	5.79	$1.74 \cdot 10^{-3}$	$2.43 \cdot 10^{4}$	2.60
50	5.29	$1.27 \cdot 10^{-3}$	$1.72 \cdot 10^{3}$	2.18
60	0.29	$5.51 \cdot 10^{-4}$	$8.80 \cdot 10^{3}$	3.16
70	-1.28	$3.63 \cdot 10^{-4}$	$4.57 \cdot 10^{3}$	3.11

Table C.4: Temperature dependency in the electrical characteristics of ZnO nanoparticle ($W = 1000\,\mu m$ and $L = 3/2\,\mu m$) when sweeping backward V_G and $V_D = 10\,V$.

$T\,(°C)$	$V_T\,(V)$	$\mu_{FE}\,(cm^2/Vs)$	I_{on}/I_{off} ratio	S(V/dec)
22	-2.45	$7.52 \cdot 10^{-3}$	$3.87 \cdot 10^{5}$	0.60
30	-1.64	$2.77 \cdot 10^{-3}$	$2.71 \cdot 10^{5}$	0.30
35	-2.61	$1.04 \cdot 10^{-3}$	$7.50 \cdot 10^{4}$	0.69
40	-1.79	$5.81 \cdot 10^{-4}$	$4.38 \cdot 10^{4}$	0.84
45	0.10	$9.09 \cdot 10^{-4}$	$2.12 \cdot 10^{4}$	1.61
50	0.84	$1.14 \cdot 10^{-3}$	$1.50 \cdot 10^{4}$	1.62
60	2.06	$5.45 \cdot 10^{-4}$	$2.33 \cdot 10^{4}$	1.82
70	4.28	$4.93 \cdot 10^{-4}$	$9.53 \cdot 10^{3}$	3.51

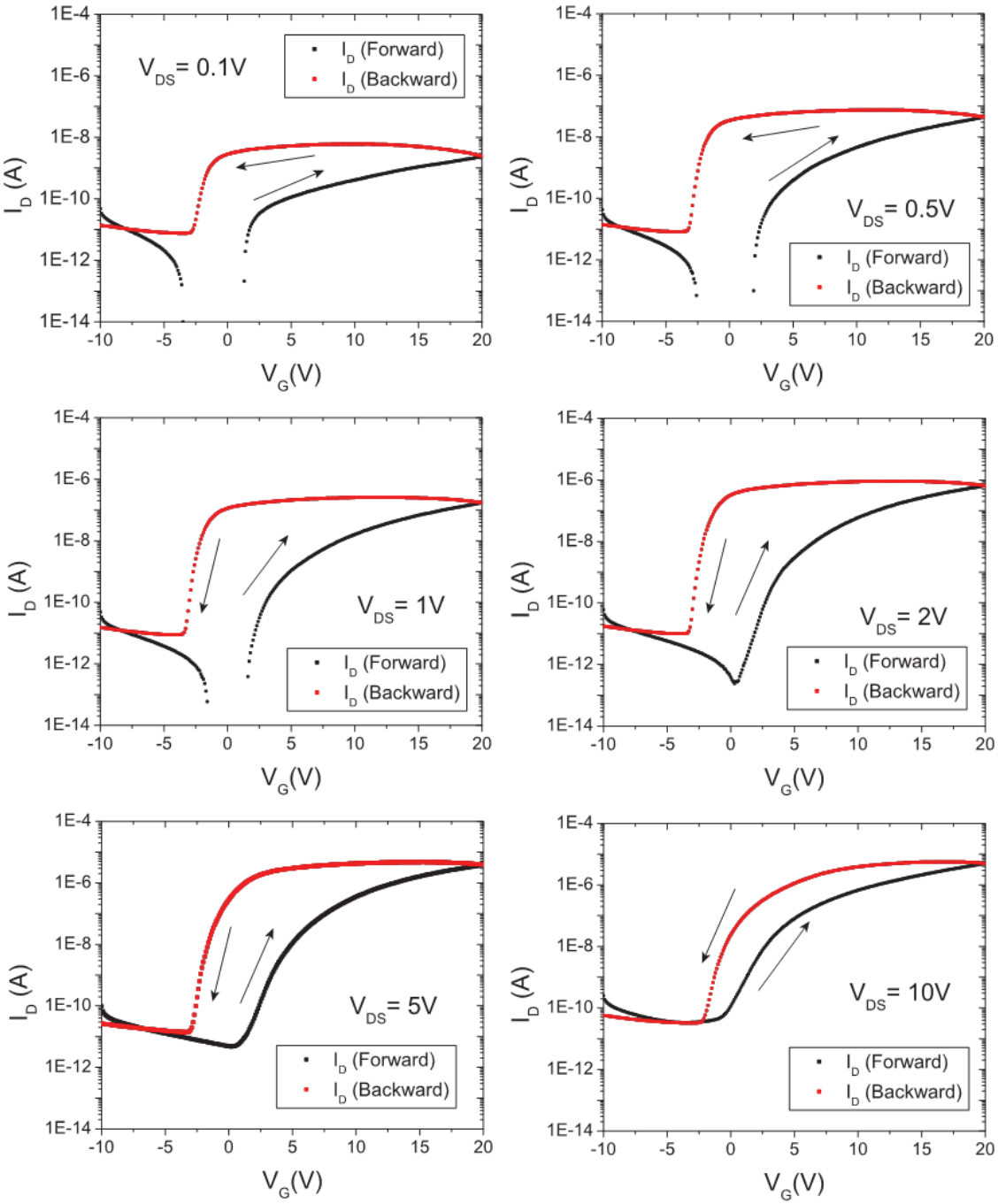


Figure C.7: Transfer characteristics of ZnO nanoparticle TFT ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$) applying different drain voltages.

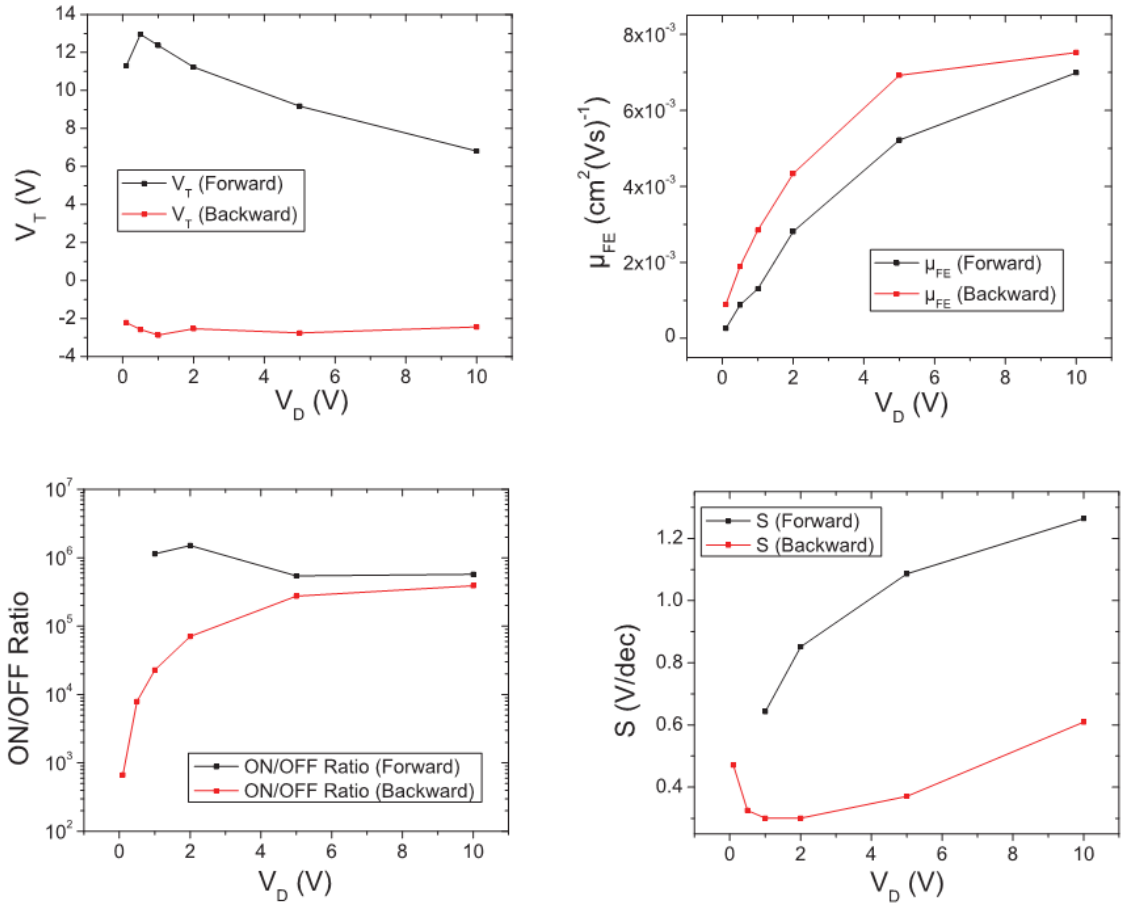


Figure C.8: Characteristics variation under different drain voltages on ZnO nanoparticle TFT ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$).

Table C.5: Voltage dependency in the electrical characteristics of ZnO nanoparticle ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$) when sweeping forward V_G.

$V_D\ (V)$	$V_T\ (V)$	$\mu_{FE}\ (cm^2/Vs)$	I_{on}/I_{off} ratio	S(V/dec)
0.1	11.30	$2.60 \cdot 10^{-4}$	–	–
0.5	12.95	$8.77 \cdot 10^{-4}$	–	–
1	12.37	$1.30 \cdot 10^{-3}$	$1.14 \cdot 10^{6}$	0.64
2	11.23	$2.81 \cdot 10^{-3}$	$1.50 \cdot 10^{6}$	0.85
5	9.17	$5.21 \cdot 10^{-3}$	$5.43 \cdot 10^{5}$	1.08
10	6.81	$6.99 \cdot 10^{-3}$	$5.73 \cdot 10^{5}$	1.26

Table C.6: Voltage dependency in the electrical characteristics of ZnO nanoparticle ($W = 1000\ \mu m$ and $L = 3/2\ \mu m$) when sweeping backward V_G.

$V_D\ (V)$	$V_T\ (V)$	$\mu_{FE}\ (cm^2/Vs)$	I_{on}/I_{off} ratio	S(V/dec)
0.1	-2.22	$8.96 \cdot 10^{-4}$	$6.70 \cdot 10^{2}$	0.47
0.5	-2.58	$1.89 \cdot 10^{-3}$	$7.93 \cdot 10^{3}$	0.32
1	-2.87	$2.84 \cdot 10^{-3}$	$2.28 \cdot 10^{4}$	0.30
2	-2.54	$4.33 \cdot 10^{-3}$	$7.05 \cdot 10^{4}$	0.30
5	-2.75	$6.92 \cdot 10^{-3}$	$2.74 \cdot 10^{5}$	0.37
10	-2.45	$7.52 \cdot 10^{-3}$	$3.87 \cdot 10^{5}$	0.60

APPENDIX D SUMMARY IN PORTUGUESE (RESUMO EM PORTUGUÊS DA DISSERTAÇÃO)

ESTUDO DA HISTERESE EM TRANSISTORES DE FILMES FINOS DE NANOPARTÍCULAS DE ÓXIDO DE ZINCO

1. INTRODUÇÃO

Milhares de organizações têm buscado eletrônica orgânica, flexível e impressa. Enquanto algumas dessas tecnologias já estão maduras, com o aumento substancial no mercado de películas fotovoltaicas, outras, como transistores de filmes finos, tornaram-se comercialmente disponíveis recentemente.

Os benefícios destes novos produtos eletrônicos são diversos, variando de menor custo, melhor desempenho, flexibilidade, transparência, confiabilidade e melhores credenciais ambientais. Produtos eletrônicos e elétricos existentes serão modificados e utilizados em uma grande variedade de novas aplicações, como sensores de pele eletrônica e telas transparentes.

Para transistores de filmes finos (TFT – *thin-film transistors*), o uso de silício policristalino, como material ativo, requer um processo de integração complexo e de alto custo. Esta é a razão principal para o crescente interesse em semicondutores processáveis, via solução, para processos de baixo custo e baixa temperatura. Transistores à base de materiais orgânicos, em particular o pentaceno, são alternativas para o silício policristalino. No entanto, semicondutores orgânicos apresentam limitada mobilidade de portadores no canal, instabilidade no ar e baixa confiabilidade elétrica, que geralmente são inaplicáveis para o processo de baixo custo.

Soluções baseadas em materiais inorgânicos têm ganhado foco entre os pesquisadores como uma possível alternativa. Entre estas, o óxido de zinco (ZnO) tem atraído a atenção como um material chave por causa de suas propriedades elétricas, sensoriais e ópticas.

Com o foco em aplicações de baixo custo, um processo com alta taxa de saída é necessário. Isto normalmente é alcançado ao se empregar técnicas simples de fabricação, como *spin-coating*, *inkjet-printing* ou processos *roll-to-roll*. Com o aperfeiçoamento da tecnologia de crescimento, novas nanoestruturas foram desenvolvidas e o óxido de Zinco nanoparticulado tem apresentado características condizentes com processos de baixo custo, uma vez que é possível processar as nanopartículas de ZnO diretamente via solução sem um processo custoso e de alta temperatura.

Porém, ao se integrar TFT com nanopartículas de óxido de zinco, alguns problemas foram observados, tais como: presença de histerese na curva I-V, baixa mobilidade de efeito de campo elétrico devido às interligações entre as nanopartículas, rugosidade das nanopartículas na interface do dielétrico de porta e o processo com altas temperaturas, que não é adequado para alguns substratos flexíveis.

Neste trabalho, nanopartículas de ZnO foram utilizadas para integrar transistores de filmes-finos, e PVP e PECVD-SiO_2 como dielétrico de porta. Uma investigação experimental foi feita a fim de observar o comportamento da histerese na curva de transferência, juntamente com essa investigação foi proposto um modelo qualitativo para o comportamento observado.

2. JUNÇÃO METAL-SEMICONDUTOR

Neste capítulo, as propriedades básicas da junção metal-semicondutor (Barreiras Schottky) foram expostas. Antes de serem discutidas as propriedades de tal junção, foram apresentadas as bandas de energia e a sua representação, tanto para o metal quanto para um semicondutor tipo-n, já que o ZnO é intrinsecamente um semicondutor deste tipo.

Após isto, foi discutido sobre o contato entre o metal e o semicondutor, onde foram também mostradas as bandas de energia no equilíbrio, e sobre a aplicação direta e reversa de potencial sobre a junção. Foram também apresentados brevemente o efeito Schottky, os mecanismos de transporte de corrente através de barreiras Schottky e o seu funcionamento nas condições encontradas nos transistores de nanopartículas de ZnO.

3. PROPRIEDAS DO ÓXIDO DE ZINCO E DO POLÍMERO USADO COMO DIELÉTRICO DE PORTA

O óxido de zinco nanoparticulado vem se mostrando como um material inorgânico promissor para a integração de transistores de filmes-finos do tipo-n, devido as sua compatibilidade com processos a base de soluções, baixa temperatura e processos com alta taxa de saída. Neste capítulo, as propriedades básicas do óxido de zinco foram discutidas com foco nas propriedades elétricas e ópticas.

Também foram apresentadas as nanopartículas (AdNano ZnO 20), fornecidas pela empresa Degussa AG, que foram utilizadas no processo de fabricação.

Poly(4-vinylphenol) ou PVP é um polímero ácido fraco que, devido a sua grande gama de aplicações, vem sendo pesquisado pela indústria de microeletrônica como um possível candidato a dielétrico de porta. A estrutura química do PVP, juntamente com o seu agente interconector (*cross-linker agent*), foi apresentada. Também foram avaliadas as propriedades elétricas do dielétrico em função do processo de integração utilizado e o efeito do grupo hidroxila presente na sua composição.

4. TRANSISTORES DE FILMES-FINOS DE ÓXIDO DE ZINCO

O capítulo 4 está dividido basicamente em três partes. Na primeira parte é apresentado o modelo básico da estrutura do transistor de filmes finos. O princípio de funcionamento é demonstrado de modo qualitativo, por meio de diagramas de bandas e por meio de equações. Modelos mais complexos também são brevemente analisados. No ponto de vista prático, os transistores podem assumir certas configurações, onde basicamente são avaliadas a posição do eletrodo de porta e a posição do canal em relação os eletrodos de dreno e fonte.

Na segunda parte deste capítulo foram apresentados transistores de filmes-finos que utilizam ZnO como semicondutor ativo. Primeiramente foi mostrada a evolução destes

transistores no grupo de pesquisa, uma cooperação entre a Universidade de Paderborn - Alemanha e a Universidade Federal do Rio Grande do Sul – Brasil. No início, utilizavam-se nanopartículas de silício porém, devido a grande resistência entre as nanopartículas e o baixo desempenho dos dispositivos integrados, optou-se por substituir nanopartículas de silício por nanopartículas de óxido de zinco. Os dispositivos baseados em ZnO apresentaram uma melhor performance e características potenciais para serem utilizados em eletrônica flexível e de baixo-custo. Nesta etapa também foi abordada a contribuição do autor no desenvolvimento dos transistores no grupo, além da observável histerese presente na curva I-V dos mesmos.

Juntamente com o trabalho do grupo, foram apresentados estudos de outros pesquisadores. Nesta revisão bibliográfica, foram demonstrados TFT baseados em ZnO que apresentavam algumas características importantes, tais como: transparência, flexibilidades, avaliação de desempenho, utilização de diferentes nanoestruturas e problemas, como por exemplo a histerese e a rugosidade na interface com o dielétrico de porta. Também se discutiu o mecanismo de transporte em filmes compostos de nanopartículas de ZnO.

A última parte deste capítulo tratou do processo de integração dos transistores caracterizados neste trabalho. Sendo apresentado o transistor integrado que utiliza PVP como dielétrico de porta e depois mostrado o transistor com dióxido de silício como dielétrico.

5. RESULTADOS E DISCUSSÃO

Neste capítulo são apresentados os resultados da caracterização dos transistores integrados. Previamente aos resultados, foram discutidas algumas razões para o surgimento da histerese na curva I-V de dispositivos baseados em ZnO. Para isto, também consideraram-se explicações provenientes de transistores baseados em materiais orgânicos que possuem o mesmo polímero utilizado neste trabalho (PVP).

As possíveis causas da histerese, quando utilizado o PVP como dielétrico, estão relacionadas ao grupo hidroxila (OH-). Este grupo químico está relacionado a deixar o polímero com uma propriedade polar, o que é relatado como a origem deste deslocamento da tensão de limiar de acordo com a direção da varredura da tensão de porta. O grupo hidroxila também é reportado na influência do aumento da corrente de fuga pelo dielétrico e ao aumento da concentração de armadilhas na interface com o semicondutor.

Contudo, armadilhas presentes na superfície das nanopartículas de óxido de zinco também têm um papel fundamental para a histerese. O oxigênio aprisionado na superfície funciona como um redutor de portadores (elétrons) livres nas nanopartículas. Ao ocorrer a desabsorção deste oxigênio pela tensão aplicada ou por exposição de luz ultravioleta, a concentração de elétrons no semicondutor é aumentada, diminuindo a resistência do canal e aumentando a corrente.

A apresentação dos resultados obtidos da caracterização elétrica dos TFT integrados começou pelo dispositivo que tem como dielétrico de porta o PVP. Após a exposição da curva de transferência, que apresentou uma histerese pronunciada no sentido anti-horário, as características básicas (tensão de limiar, mobilidade, razão I_{on}/I_{off} e

declividade da região sub-limiar) do transistor foram descritas. A partir do teste de estresse, foi observado um aumento da corrente de dreno, mesmo com tensões de porta e dreno constantes. Este aumento está de acordo com o esperado da polarização do PVP, que foi atribuído como a principal razão da histerese neste transistor, além que concorda com a direção da histerese apresentada na curva de transferência. Também foi observada no teste de estresse, a presença de uma flutuação discreta na corrente de dreno, que foi atribuída ao chaveamento de armadilhas em determinados pontos na rede de caminhos formados pelas nanopartículas.

Observou-se que a histerese é dependente da temperatura. Ao se aquecer o transistor, observa-se que a histerese desaparece por volta de 55ºC e ao elevar ainda mais a temperatura, a histerese troca o sentido, ficando no sentido horário. Foi realizado também um teste de estresse a temperaturas mais elevadas, onde notou-se que a corrente de dreno diminui apesar da tensão constante aplicada, o que está de acordo com a direção da histerese na curva I-V. Esta variação do comportamento da histerese em função da temperatura foi atribuída a uma compensação da polarização do PVP pelo aumento das armadilhas na interface entre o semicondutor e o dielétrico.

A influência do oxigênio na superfície das nanopartículas pode ser observada no transistor com SiO_2 como dielétrico de porta. A direção anti-horária da histerese está de acordo com a explicação de que ao ser liberado o oxigênio, aumenta a condutividade do canal, aumentando a corrente de dreno. Também foi realizado um teste de estresse neste transistor, onde foi mostrado que o efeito da liberação do oxigênio (aumento da corrente de dreno) satura após um certo período e, a partir deste ponto, o efeito de captura de elétrons na interface com o óxido de silício é o efeito dominante.

Ao final deste capítulo são discutidos possíveis testes a serem feitos a fim de solidificar a explicação apresentada pela caracterização dos transistores.

6. CONCLUSÃO

Em resumo, o presente trabalho apresentou o processo de integração de dois tipos de transistores, um utilizando PVP como dielétrico de porta e o outro utilizando SiO_2 como dielétrico. A histerese na curva I-V observada quando a tensão de porta é incrementada e posteriormente reduzida foi o foco do estudo deste trabalho.

Foram apontadas, como as principais causas para a histerese, a polarização do polímero utilizado como dielétrico de porta, armadilhas na interface entre o semicondutor e o dielétrico e as armadilhas na superfície das nanopartículas na forma de moléculas de oxigênio. Para suportar esta explicação foram feitos teste de estresse e caracterizações elétricas em variadas temperaturas.

Também foi observada a influência de armadilhas localizadas em determinados caminhos de percolação por meio de uma flutuação discreta na corrente no teste de estresse. O que solidifica o conceito que o transporte de corrente em filmes constituídos de nanopartículas de ZnO é feitos por uma rede de caminhos criados pelas interligações das mesmas.