**Abstract**

The Izhikevich Simple Model (ISM) for neural activity presents a good compromise between waveform quality and computational cost. FPGAs (Field-Programmable Gate Array) are powerful, flexible, and inexpensive digital hardware that can implement such a model. We present an implementation on FPGA of the ISM whose latency is up to 56 times smaller than the ones in the literature.

**Comparison with the Literature**

<table>
<thead>
<tr>
<th>✔</th>
<th>Good waveform</th>
<th>✔</th>
<th>Up to 56x lower latency</th>
<th>☇</th>
<th>High clock speed</th>
<th>☒</th>
<th>No pipeline</th>
<th>☒</th>
<th>No logic reuse</th>
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</thead>
</table>

**Conclusions**

Our implementation is best suited for hybrid networks systems and presents a fair performance for artificial-only networks. The low latency of the circuit will allow us to reuse the same neuron multiple times.

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**References**


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Modified Equations of ISM \[1,2,3\]

\[ \begin{align*}
\frac{dv}{dt} &= \frac{1}{32} \left( v^2 + 4v + 109.375 - u^* + I^* \right) \\
\frac{du^*}{dt} &= a^*(b^*v - u^*) \\
\end{align*} \]

\[ \begin{array}{c}
v \geq 30mV \\
\Rightarrow \begin{cases}
v \leftarrow c \\
u^* \leftarrow u^* + d
\end{cases}
\end{array} \]

Implemented Neuron

Used FPGA: Altera’s DE4

Results

This data was obtained from the FPGA running our implementation through the SignalTap II tool in Quartus II® Software.