Exploration of Approximate Memory Architectures in HEVC
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Introduction

HEVC (High Efficiency Video Coding)
• Requires 40%-70% higher computation effort and >2x more memory accesses when compared to H.264
• Strongly relies on the memory hierarchy to enhance overall performance

Approximate Computing Techniques
• Explore the energy and performance benefits that can be achieved through hardware level approximations
• Usually in the context of error-tolerant applications

Problem Context
• HEVC runs in platforms with complex memory hierarchies
• Great impact both in execution time and energy consumption associated to memory accesses
• Previous study done mapping the memory accesses of the HEVC Encoder’s modules

• Inter-Prediction - 72.9% and Residual Coding – 15.1% are the most demanding modules in terms of memory

Analysis

• The encoding process is very resilient to faults
  • Faulty bits will probably be masked if the data differs too much from the average in a given Coding Tree Unit (CTU)
  • Higher resolution videos are more resilient because the CTUs have less variation in the pixel values
    • Compromised bits are more likely to be dismissed
  • 5000 Fault injections in memory for 144p video have shown a Silent Data Corruption (SDC) rate of 0.45% while 99.5% were masked (didn’t affect the resulting video)
  • Testing higher video resolutions resulted in no SDCs

Next steps
• Simulate approximate memory for the more demanding modules of the encoder
• Compare different approaches to approximations currently available in the literature

References