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Exploiting EDA Tools for the Analysis and Protection of Integrated Circuits against Radiation-Induced Single Event Transients

Graduation Project

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CONTENTS

LIST OF ABBREVIATIONS AND ACRONYMS

BLIF	Berkeley Logic Interchange Format
CED	Concurrent Error Detection
CMOS	Complementary Metal-Oxide-Semiconductor
DCS	Detailed Circuit Simulation
EDA	Electronic Design Automation
EMF	Electrical Masking Factor
FR	Failure Rate
GND	Ground
IC	Integrated Circuit
ISCAS	IEEE International Symposium on Circuits and Systems
MTTF	Mean Time To Failure
PTM	Predictive Technology Model
SER	Soft Error Rate
SET	Single Event Transient
SEU	Single Event Upset
SOI	Silicon On Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
TMR	Triple Modular Redundancy
VDD	Voltage Drain-Drain

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ABSTRACT

This work presents a study of the analysis and protection of integrated circuits against *single event transients* using EDA tools. Single event transient (SET) arises from the strikes of high-energy particles in combinational logic blocks and may lead the system to undesired results. Dependability of nanometer digital circuits to SET becomes a major concern with aggressive technology scaling, reduced voltage levels and increased clock frequencies.

EDA tools play an important role in robust circuits design. Even though device simulation requires advanced computational methods and considerable computing time, it has great contribution to the understanding of the physical mechanisms leading to radiation-induced errors. Moreover, EDA tools represent a cost-effective analysis and protection solution in earlier design-cycle steps when compared to process-related and physical testing approaches.

In a first moment, literature is reviewed introducing gate-level and transistor-level analysis and protection methodologies. Secondly, an existing academic EDA tool to improve circuits' dependability is studied. After, an implemented detailed circuit simulation technique is introduced. Finally, sensitivity reduction results provided by the academic tool are analyzed with the detailed circuit simulation technique.

Keywords: Single event transients, reliability of digital circuits, EDA tools.

Explorando Ferramentas de EDA para a Análise e Proteção de Circuitos Integrados Contra Eventos Singulares Transitórios Induzidos por Radiação

RESUMO

Este trabalho apresenta um estudo da análise e proteção de circuitos integrados contra *eventos singulares transitórios* usando ferramentas de EDA. Eventos singulares transitórios (SETs) surgem a partir da colisão de partículas de alta energia em circuitos combinacionais podendo levar o sistema a resultados indesejados. A confiabilidade de circuitos digitais nanométricos em relação a SETs torna-se uma grande preocupação devido à redução agressiva das dimensões de transistores, dos níveis de voltagem bem como ao aumento da frequências de relógio.

Ferramentas de EDA desempenham um papel importante na concepção de circuitos robustos. Mesmo que a simulação de circuitos requeira métodos computacionais avançados e um tempo de execução considerável, ela tem grande contribuição na compreensão dos mecanismos físicos que provocam erros induzidos por radiação. Além disso, ferramentas de EDA representam uma solução custo-eficaz para análise e proteção em etapas anteriores do ciclo de concepção quando comparada aos métodos de teste físico e às técnicas relacionadas ao processo de fabricação.

Em um primeiro momento, a literatura é revisada, introduzindo metodologias de análise e proteção no nível portas e no nível transistor. Em segundo lugar, uma ferramenta acadêmica de EDA existente para aumentar a confiabilidade de circuitos é estudada. Depois, uma técnica implementada de simulação detalhada de circuitos é introduzida. Finalmente, os resultados de redução de sensibilidade fornecidos pela ferramenta acadêmica são analisados usando a técnica de simulação detalhada.

Palavras-chave: Eventos singulares transitórios, confiabilidade de circuitos digitais, ferramentas de EDA.

1 INTRODUCTION

1.1 Context

The electrical behavior of digital integrated circuits (ICs) may suffer the influence of the environment they are inserted. In spaceborne applications, high energy heavy ions and high energy protons may result in either direct or indirect interaction with ICs and may be induced by cosmic rays and solar radiation, for instance. Also, in terrestrial and high-altitude applications, alpha particles as well as high and low energy neutrons may interact with the electrical behavior of ICs. In these applications, the phenomena are usually induced by radioactive decay, cosmic ray byproduct or thermal energy. The effect of these interactions is related to the manner in which the undesired particles disturb the original arrangement of charge carriers (electrons and holes) in sensitive nodes of the circuits. Figure 1.1 illustrates the effect of junction charge collection induced by heavy ion on a sensitive semiconductor region.

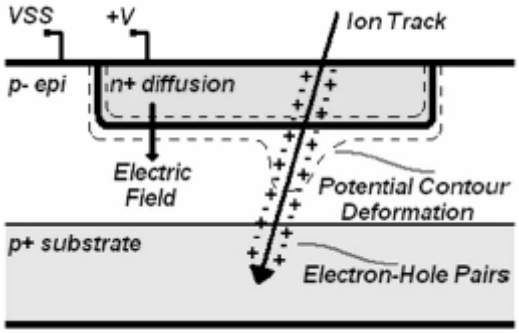


Figure 1.1: Charge carriers disturbance on a sensitive semiconductor region

There are two main radiation sources that may produce soft errors in ICs operating at sea level (BAUMANN, 2001). One of them is represented by the alpha particles emitted by radioactive impurities existing in the ICs itself and in its package. The other source is represented by cosmic neutrons resulting from the interaction of high-energy cosmic rays with atoms in the earth's atmosphere.

Undesired current disturbances may reflect on a logical state change in the harmed circuit node. If a logical state change occurs in a memory element (e.g. static latches and SRAMs), the effect is known as *single event upset* (SEU). If a temporary current disturbance occurs in a combinational logic circuit, the effect is known as *single event transient* (SET). This logical state change may lead a system to unexpected results, manifesting itself as a glitch propagating to the primary outputs or the next level of flip-flops. This wrong signal or datum is known as a *soft error*. The rate at which a circuit suffers or is predicted to suffer a soft error is known as *soft error rate* (SER). The

minimum charge produced by a particle strike to cause an error is known as the *critical charge* (Q_c).

SER may vary for different technology nodes or operating frequencies. This rate tends to increase as the square of the technology feature size and voltage levels decrease. SER regarding single event transients depends on clock frequency. SER regarding single event upsets is independent of clock frequency (MAVIS, 2002).

1.2 Motivation

In deep-submicron CMOS technologies, soft errors due to radiation represent a challenge for the reliability of integrated circuits. Applications like high-end servers may contain large memory caches and, if no protection is applied, soft errors may cause a system crash more than once a month. These errors are also an important issue in applications such as automotive and medical, which require high product reliability (HEIJMEN; NIEUWLAND, 2006).

The impact of a single event transient in the chip SER grows with technology scaling and it is more complicated to simulate and to mitigate than a single event upset. The contribution of combinational logic SER to the *mean-time-to-failure* (MTTF) rate is increasing not only with the decrease in the logic gate dimensions, but also with the increase in the amount of combinational logic per chip and with the increase in frequency of operation. Dedicated approaches in testing, simulation and design modification are necessary to make logic more SER robust.

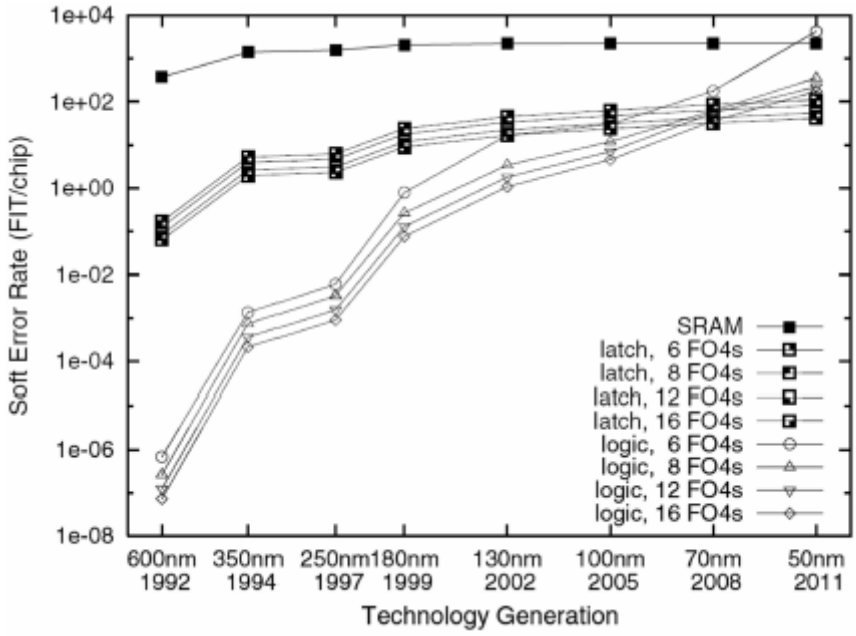


Figure 1.2: SER/chip for SRAM, latches and logic (SHIVAKUMAR et al, 2002)

Whereas efficient memory protection solutions have been concerned (ROCKETT, 1988; WHITAKER et al, 1991; CALIN et al, 1996), error rates in combinational logic circuits are increasing for nanometric technologies. The reduction of voltage levels and the reduction of the square of technology feature size, allied to increasing clock frequency reduce the transition time of the logic gates. SERs in combinational logic circuits are predicted to reach levels comparable to SERs in memory elements by 2011

as shown in Figure 1.2. It is necessary to find efficient combinational logic circuits protection to improve the dependability of circuits under energetic particles influence.

SERs in combinational logic circuits can be reduced, for instance, by resizing the transistors (LAZZARI et al, 2008). Such approach intends to find the minimum transistor widths that attenuate SETs. Efficient techniques must be applied to reach high soft errors coverage with the lowest penalties on area, consumption and performance. Electronic Design Automation (EDA) tools play an important role in the design of SET-hardened combinational logic blocks.

Device simulation requires advanced computational methods and considerable computing time. However, it has great contribution to the understanding of the physical mechanisms leading to soft errors. Simulation also provides accurate estimations of parameters that are applied in SER prediction methods.

1.3 Project description

The scope of this project is to exploit EDA tools and techniques to analyze and protect combinational parts of integrated circuits at the gate-level and at the transistor-level. In a first moment, literature is reviewed introducing gate-level and transistor-level analysis and protection methodologies. Secondly, an existing academic EDA tool to improve circuits' dependability is studied. After, an implemented detailed circuit simulation technique is introduced. Finally, sensitivity reduction results provided by the academic tool are analyzed with the detailed circuit simulation technique.

Figure 1.3 illustrates the project overall flow. A set of benchmark circuits is selected for the SET hardening optimizations. The academic tool mentioned above (which is called SET-Factor) is responsible for these optimizations. A detailed circuit simulation framework is implemented to analyze the results presented by SET-Factor.

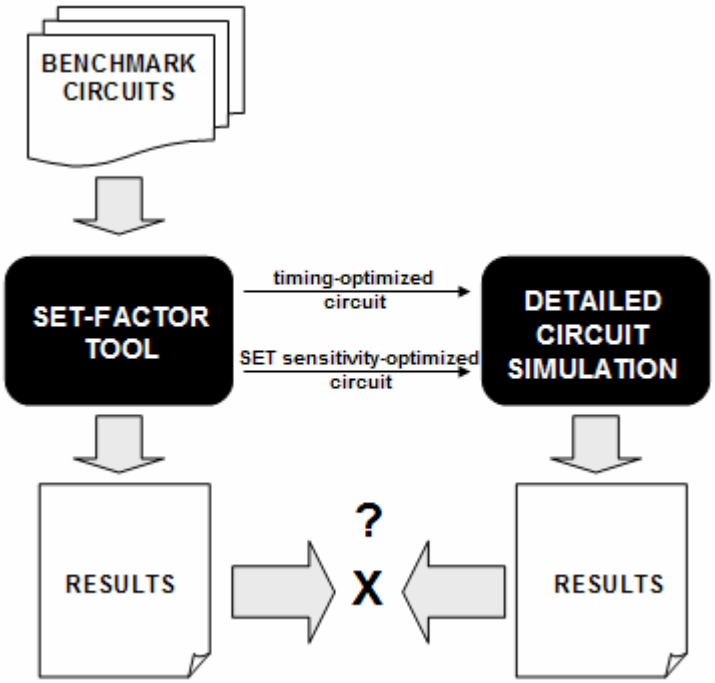


Figure 1.3: Project overall flow

2 RELATED WORKS

2.1 SER analysis

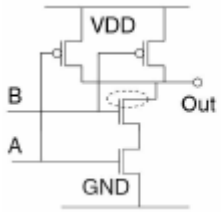
Soft error rates analysis in combinational logic circuits is discussed in (HEIJMEN; NIEUWLAND, 2006) and (NIEUWLAND et al, 2006). The first work presents techniques to evaluate SER in physical ICs under real conditions as well as simulation approaches to understand and predict errors. The contribution of both SEU and SET is considered, but a special attention is given to SET. The second work presents methods for soft error analysis and protection focusing only on combinational logic circuits. Both works represent a very important contribution regarding single event transient analysis in deep-submicron technologies.

(HEIJMEN; NIEUWLAND, 2006) presents methods that are applied to measure SER of physical devices under nominal conditions and under accelerated conditions. Under nominal conditions, the neutron flux and consequently the neutron-induced component of the SER increase 10× with every 3km of increase in altitude, saturating at about 15km. At high altitudes the neutron-component dominates over the alpha-induced SER. To accurately measure the alpha-induced contribution to the SER, experiments must be performed at underground locations that are shielded from cosmic neutrons. Under accelerated conditions, the presence of a strong extra radiation source can induce neutron flux with an intensity eight orders of magnitude higher than the neutron flux at the sea level in nominal conditions. It means that one hour under these accelerated conditions is equivalent to about 15,000 years of exposure under nominal conditions at the sea level. Different conditions of exposure, such as in high altitudes and under extra radiation source, can be extrapolated to obtain the SER levels at sea level.

Measuring SER in combinational logic is not a trivial task. The transients have a short duration and a SET has to be latched to a memory element to be observable. The vulnerability of a combinational logic cell depends on the circuit topology as well as on the sizes of the transistors. The small gate capacitance and weak current drive of small transistors represent potential sensitivity to SET. Simulation is usually preferred over measurement to characterize SER in combinational logic.

(NIEUWLAND et al, 2006) explains that standard cells are not all equally sensitive and neither the transistors within a standard cell have an equal contribution to the logic SER of that gate. For instance, in the NAND gate of the Figure 2.1, the N-transistor connected to the output is the most sensitive to induce a transient. The main reason is the location of this transistor in the NAND gate: near the output. The second reason is that N-transistors are more vulnerable to transients than P-transistors because of the

high mobility of their charge carriers. The probability of inducing a transient is smaller in P-transistors due to the lower mobility of the holes.



Inputs A	Inputs B	Failure rate (A.U.)
0	0	10
0	1	120
1	0	90
1	1	50

Figure 2.1: Transient probability of a NAND gate (NIEUWLAND et al, 2006)

The transient probability is strongly dependent on the input combination. When the NAND gate receives a '00' input combination, both P-transistors in parallel drive the output node to VDD. Only the drain of the upper N-transistor is sensitive to a transient current to GND (dashed region in Figure 2.1). This combination has small contribution in SER. However, the failure rate for the '01' input combination is high. In this case, the drain, channel and source regions of the upper N-transistor as well as the drain-source region of the lower N-transistor are sensitive to transient currents to ground. Also, only one P-transistor is responsible for driving the output node, representing less drive strength than when both P-transistors are driving in parallel.

According to the work mentioned above, the failure rate values in the table of Figure 2.1 are based on simulations using models that were calibrated with data from SER measurements on memory elements. This table shows that even if '01' and '10' combinations are logically equivalent, they result in a different failure rate. This difference is expected, since for the '10' combination only the upper N-transistor is sensitive to a transient current to the ground.

The analysis of the SER of combinational logic can be performed starting from three estimations (NIEUWLAND et al, 2006):

Gate-SER: it is necessary to know the probability (*P*) that each possible input combination is applied to a gate and also the failure rate of each combination. Gate-SER is obtained by multiplying *P*s for all possible input vectors with the corresponding failure rates and adding them.

Glitch-observability: in some gates, a certain value in one input can force the output to a specific value, despite the value on the other inputs. For example, a '0' in one input of a NAND gate is a controlling value which will necessarily force the output to '1'. If a gate receives a controlling value, a transient error (glitch) will not propagate to the output (as illustrated by Figure 2.2). The transient blocking is also called *logical masking*. The glitch-observability is the probability that a glitch originating from a certain gate in a circuit will propagate to the circuit's output without being logically masked by other gates in the path to the output. The glitch-observability of a gate is calculated regarding the glitch-observabilities of subsequent gates in the same path to the circuit's output.

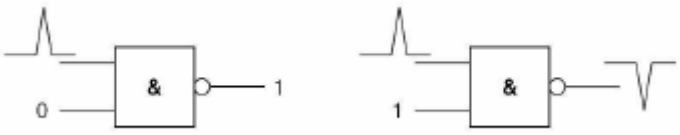


Figure 2.2: Control values for a NAND gate (NIEUWLAND et al, 2006)

Electrical Masking Factor (EMF): a glitch can be attenuated (electrically masked) in the path to the circuit's output whether its amplitude and duration are not large enough (OMAÑA et al, 2003). An electrically masked glitch does not produce a failure at the circuit's output. The attenuation depends on the path length (the longer the path, the higher the probability of attenuation) and on the gate types in the path (due to dissimilar parasitic capacitances and propagation delays).

Each gate contribution to the SER of a logic circuit can be defined as the Failure Rate of the gate (FR_{gate}) and depends on the input vector probabilities to the gate, the type of the gate and the structure of the circuit. FR_{gate} can be expressed using the parameters defined above as:

$$FR_{gate} = Gate_{SER} \cdot Glitch_{observability} \cdot EMF$$

FR_{gate} can be used to identify gates with higher sensitivity to transients. Based on the contribution of each gate, the soft error rate of a circuit ($SER_{circuit}$) can be calculated by:

$$SER_{circuit} = \sum_{i=1}^{n} FR_{gate(i)}$$

$SER_{circuit}$ can be used to compare different combinational logic implementations for soft error reduction.

2.2 SER reduction

Soft error rate reduction can be performed in technology, system or circuit levels. At technology level for example, the Silicon on Insulator (SOI) technology can result in a SER reduction of approximately 5×, but this solution is not always feasible or not worth its price. At system level, it is possible to use error detection methods and recalculate the wrong datum. This solution requires great hardware complexity and re-synchronization of the circuit for recalculation. A solution at circuit level is usually more suitable (NIEUWLAND et al, 2006).

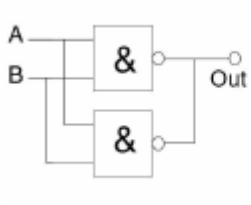
Two well-known approaches for soft error mitigation are Triple Modular Redundancy (TMR) and dual modular redundancy. (NIEUWLAND et al, 2006) explains that these approaches are not recommended due to reasons like large area overhead, additional gate delay or the efficacy on errors reduction. (MOHANRAM; TOUBA, 2003) presents the partial duplication. As not all nodes contribute equally to SER of the system, the method proposes only the duplication of the most sensitive parts and the use of two-rail code checkers. By adding these structures, an area overhead, an additional circuitry and a considerable complexity of design are introduced. Two-rail checker, for instance, will require restarting structures such as pipelines when an error is detected.

2.2.1 Gate multiplication

The gate multiplication approach is based on the idea that transients can be better compensated by increasing the drive strength of the transistors driving the output node. (NIEUWLAND et al, 2006) presents two techniques to increase the drive strength of sensitive nodes of the circuit: transistor folding (parallel transistors properly spread in the circuit) and gate multiplication. A special attention is given to gate multiplication method because it is easier to apply on circuit level by multiplicating standard cells.

This method requires neither redesign nor re-characterization of existing standard cell libraries, not affecting current flows and libraries.

The work mentioned above explains that error rate due to transients can decrease in more than 10× on average with the proposed gate multiplication method. Critical charge simulations were performed for a duplicated version of the NAND gate of the Figure 2.1. The results are shown in Figure 2.3.



Inputs A	Inputs B	Failure rate (A.U.)
0	0	0.5
0	1	15
1	0	10
1	1	2

Figure 2.3: Transient probability of a duplicated NAND gate (NIEUWLAND et al, 2006)

The algorithm implemented by (NIEUWLAND et al, 2006) handles an input netlist (Verilog file) of the circuit. A list of gates is generated and ordered by the gate's contribution to the SER. Those gates with major contribution are duplicated until the target area overhead or SER reduction level is achieved. Maximum area overhead and SER reduction level are user inputs.

Figure 2.4 shows a specific example in which the critical gates identified are a NAND2, a NOR4 and a NAND4. The SER of this circuit was reduced by 50% at an area overhead of 30%. Simulations using a number of ISCAS'85 logic benchmarks shows that larger circuits (e.g. c7552 with 7552 gates) tends to have a better ratio between SER improvement and area overhead due to logical and electrical masking. For larger circuits, more than 60% SER reduction was achieved at 20% area cost.

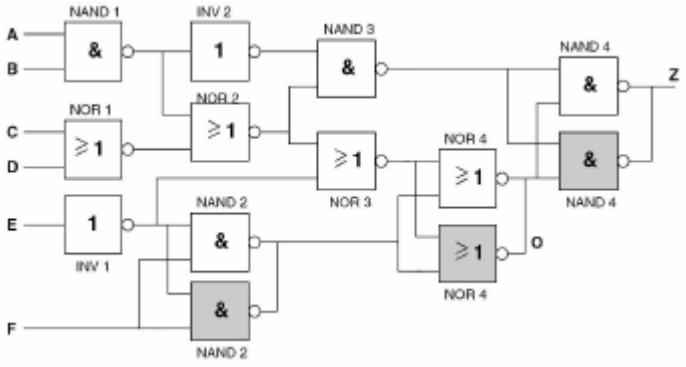


Figure 2.4: Example circuit with 50% SER reduction by duplicating only three gates (NIEUWLAND et al, 2006)

2.2.2 Partial duplication

Based on the asymmetric error susceptibility of nodes in a logic circuit (mainly due masking factors and distance from primary outputs), (MOHANRAM; TOUBA, 2003) introduces a partial duplication approach to reduce error rates in logic circuits with concurrent error detection (CED). The main idea is to target the CED towards to nodes with highest contribution to increase the SER. Results show this technique has a significant tradeoff between the SER reduction and the overheads when compared to full duplication methods, especially considering losses in terms of area, once partial duplication does not cover all nodes.

The proposed method involves selecting a set of nodes (called “cutset”) near the primary outputs. Logic is partially duplicated as shown in Figure 2.5. The circuit is traversed from the primary outputs to the primary inputs adding nodes with highest soft error susceptibility to the cutset. The area overhead is updated whenever a new node is added to the cutset. The process terminates when the size of the cutset equals or exceeds the specified area overhead.

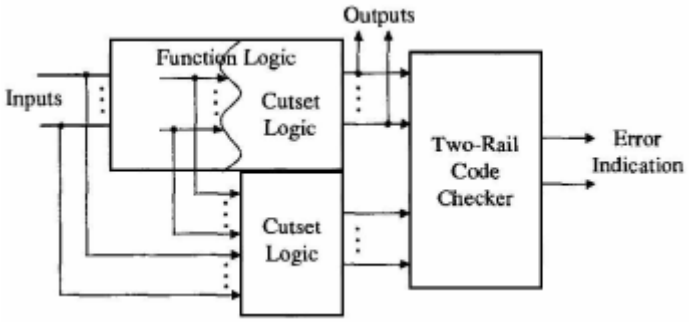


Figure 2.5: CED with partial duplication (MOHANRAM; TOUBA, 2003)

The results achieved by (MOHANRAM; TOUBA, 2003) show a 50% area overhead for an average reduction of 90% in soft error failure rate.

2.2.3 Gate sizing

The gate sizing method consists in replacing the most sensitive cells of a circuit by more robust ones. A library of cells usually contains more than one version of each cell, with different transistor sizing. Therefore, a sensitive cell may be replaced by another one with bigger transistors and same logic function to reduce SER.

Gate sizing techniques for SER reduction are presented in (DHILLON et al, 2005), (CAZEAUX et al, 2005) and (ZHOU; MOHANRAM, 2006). In (ZHOU; MOHANRAM, 2006), candidates are selected according to their sensitivity level which is determined by the logical masking of each node in the circuit. The results of this methodology are positive if compared to the results of the gate multiplication methodology (Subsection 2.2.1) due to area overhead reduction. In this work, the average area overhead is of 33% for a 90% of SER coverage. Also this method does not compromise the circuit test due to the absence of redundancy.

2.2.4 Transistor sizing

Pull-up and pull-down transistors can be dependently or independently sized to reduce SER. In the first case, the approach is also called symmetric transistor sizing, whereas in the second case it is called asymmetric transistor sizing. (LAZZARI et al, 2008) introduces a transistor sizing methodology which aims to reduce SER by sizing pull-up and pull-down blocks of the gates separately. Most sensitive nodes are identified considering logical and electrical masking factors. The smallest transistor widths of each circuit gate for SET attenuation are found by traversing and analyzing the circuit from the primary outputs to the primary inputs. The degradation of a SET depends on the delay of each gate in the path.

The sensitivity model used in the work cited above was proposed in (WIRTH et al, 2007). In this model, the behavior of a SET in a circuit node is a function of the driving gate resistances and the capacitances involved with the faulting node. Figure 2.6 shows

an example of a transient propagation after a particle strikes the output of a NAND gate (in the first stage of the circuit). The transient pulse duration at the hit node is function of the resistance R, the capacitance C, the charge Q and some technology process constants. In the example of Figure 2.6, R is $r_1 + r_2$ because this value is defined as the effective resistance of the pull-up path (if PMOS transistors are active) or the effective resistance of the pull-down path (if NMOS transistors are active). C is defined as the effective load capacitance driven by the output node. The critical charge Q_c is the minimum charge of a particle needed to induce a SET in a node. It depends on several process-related factors and also on R and C.

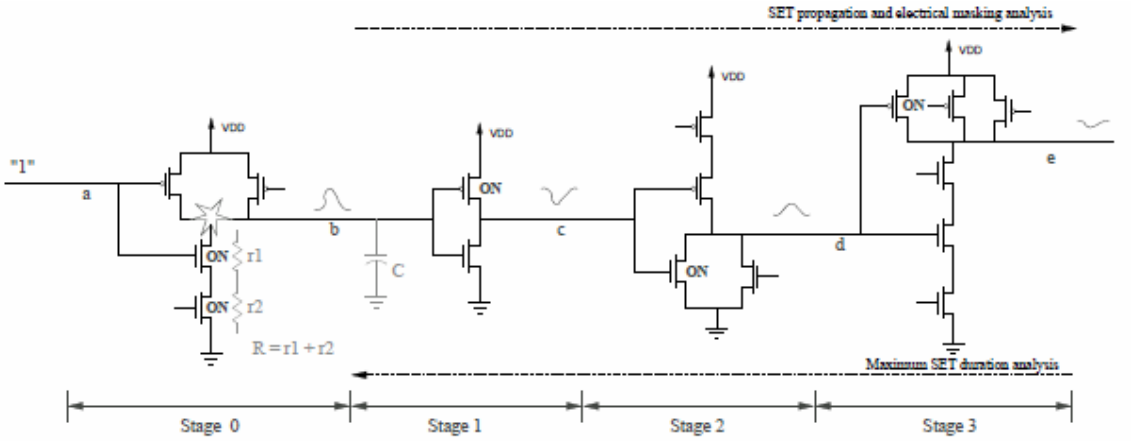


Figure 2.6: A transient pulse propagation example (LAZZARI et al, 2008)

In the example shown in Figure 2.6, the NMOS transistors of the gate in the first stage are the main responsibles for the SET duration, as they are active (thus, they represent the effective R of the node). Therefore, the transistor sizing algorithm proposed by (LAZZARI et al, 2008) sizes only these transistors aiming to reduce the resistances r_1 and r_2 and consequently increase their capacitances.

Results show that the transistor sizing strategy introduces small area overhead and timing penalties. Table 2.1 shows some data extracted from (LAZZARI et al, 2008), regarding average area, timing and power overheads to reduce the circuit sensitivity to 50% and to 0%. Four combinational circuits were used, ranging from 227 to 423 gates each.

Table 2.1: Average area, power and timing overheads for symmetric and asymmetric sizing techniques

Sizing	**Symmetric**		**Asymmetric**	
Sensitivity $S_{circuit}$	**50%**	**0%**	**50%**	**0%**
Area (%)	61.2	83.5	48.0	61.1
Power (%)	52.7	69.0	40.2	43.3
Timing (%)	7.0	12.8	6.6	10.1

These results are quite interesting. The asymmetrical transistor sizing algorithm and allied to computer-efficient models had a significant tradeoff between SER reduction and penalties in area, power and timing. This methodology for SER reduction was implemented in SET–Factor tool, which was selected to be analyzed in Section 3.

3 EXPLOITING AN EDA TOOL

3.1 SET-Factor tool description

The key insight behind the SET-Factor tool is the improvement of the dependability of circuits under energetic particles by resizing transistors in the most critical paths of the combinational blocks. The tool analyzes the vulnerability of a circuit to single event transients by identifying the most sensitive nodes. These nodes are identified concerning logical and electrical masking factors. The transistor resizing algorithm separately resizes the pull-up and the pull-down transistor networks of CMOS circuits, allowing either a symmetrical or an asymmetrical resizing.

The sensitivity of combinational parts of digital circuits can be defined by logical and electrical masking analysis (LAZZARI, 2007). SET-Factor calculates the sensitivity of a circuit according to the following equation:

$$S_{circuit} = \sum_{n=1}^{N} (1 - L_n) \cdot (1 - E_n)$$

where L_n is the probability of logical masking of a SET in a node n (glitch-observability), whereas E_n corresponds to its electrical attenuation. E_n is "1" if the transient pulse is totally attenuated or "0" if it can affect a primary output. It means that for total pulse electrical attenuation E_n = 1 and the sensitivity of the node n is zero. Logical masking is calculated by SET-Factor using controllability and observability techniques, taking into account the logical function of each gate of the circuit.

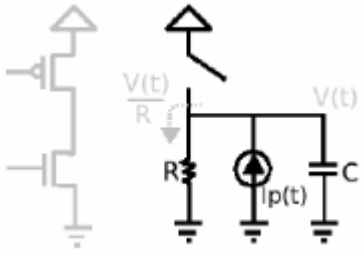


Figure 3.1: Equivalent circuit to calculate SET effect in a node (LAZZARI, 2007)

SETs are modeled using a double exponential equation (better described in Section 4.1) describing the behavior of a current source applied in the affected node. Figure 3.1 illustrates the equivalent circuit SET-Factor uses to calculate the critical charge Q_c needed to induce a SET in a node as well as the transient pulse duration. C is the effective loading capacitance lumped onto the output node of the gate and R is the effective resistance of the "ON" transistors of the gate. Pulse characteristics like voltage

peak value and peak time value are obtained using derivations of mentioned double exponential equation as presented in (WIRTH et al, 2007). Complete attenuation of a transient pulse is considered when the voltage peak does not reach ½VDD.

3.2 Transistor resizing algorithm

The key idea behind SET-Factor transistor resizing algorithm is to find the smallest transistor width of each logic gate of the circuit for SET attenuation. Basically, the transistor resizing algorithm can be divided into two major steps: first, the circuit sensitivity $S_{circuit}$ is determined using equation presented in Section 3.1; after, every node n of the circuit is visited to find the minimum transistor widths for each gate g connected to this node.

Let G be the set of gates in the circuit, N be the set of nets, O be the set of primary outputs, M be the maximum sensitivity allowed and Q_c be the maximum critical charge. In the first step, for each net n belonging to set of nets N, SET-Factor calculates the logical masking L_n and the electrical masking E_n as explained in Section 3.1 and so the sensitivity $S_{circuit}$ is determined.

In the second step, circuit is traversed from the outputs to the inputs analyzing each node and resizing the transistors in the path. For each net n, if the sensitivity S_n of the node is higher than M, the maximum pulse duration that is suppressed before the primary outputs is determined. The algorithm continuously increases the transistors width until the SET in the node is smaller than this pulse duration. When this situation is reached, the transistors are sized as expected to the charge Q_c.

The reason for the circuit traversal from the primary outputs to the primary inputs is that the propagation delay of the gates is changed after resizing. For example, if the propagation delay of a gate becomes smaller, the SET propagates with smaller degradation to the primary outputs. The algorithm ensures that during the evaluation of node n, every gate between this node and the POs have been already resized.

As the sensitivity of a node n is analyzed taking into account the effective resistance of the "ON" transistors of the gate connected to this node (Figure 3.1), pull-up and pull-down networks contribution can be separately evaluated. This is what allows SET-Factor to perform a symmetrical or an asymmetrical transistor resizing. When symmetrical resizing is selected, transistors of both pull-up and pull-down networks are proportionally resized. On the other hand, asymmetrical resizing independently resizes pull-up and pull-down networks, keeping all the transistors with the minimum width possible for SET attenuation. As in the last case, no transistor has an unnecessary width increase; area and power overhead are reduced in comparison to symmetrical approach. However, it is important to keep in mind that asymmetrical resizing may have a great impact in the original balance of rise and fall delays of the gates.

3.3 Tool usage

First of all, SET-Factor does not contain a graphical user interface. It must be launched by the UNIX command line and it uses ASCII file types as inputs. Figure 3.2 illustrates the most common inputs as well as its output.

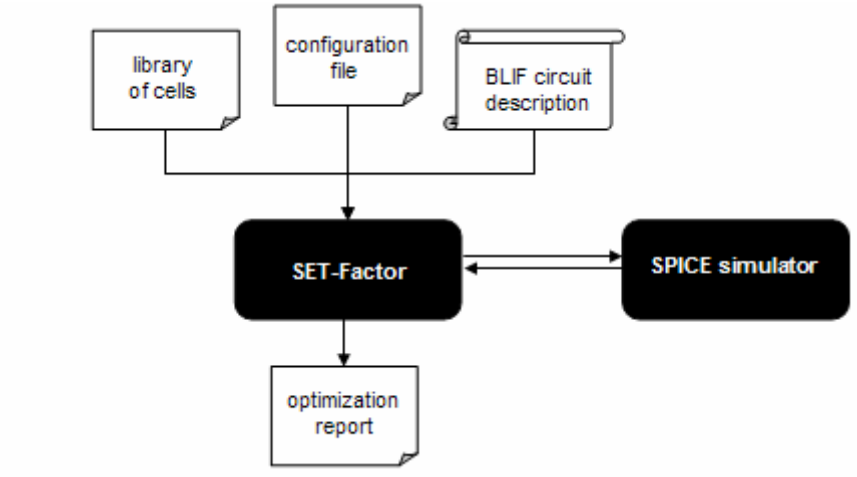


Figure 3.2: SET-Factor inputs and outputs

Input circuit is a BLIF description. All circuit gates are mapped to gates with the minimum drive strength of the library (usually referred to X1 drive strength). This circuit is then mapped by the tool to a timing-target sizing and the sensitivity to single event transients is determined. Later, depending on the user's choice (passed as an argument), the tool tries to harden this circuit using symmetrical or asymmetrical transistor resizing techniques.

The configuration file contains information regarding the work directory, the chosen SPICE simulator, maximum transistor sizes for hardening optimization, critical charge value, technology file to be used, the number of input patterns for observability detection and process related information of the transistors (as the threshold voltages, for instance).

The library of cells contains different drive strengths versions of different gates. It is used by the tool to generate the timing-optimized circuit version for further sensitivity analysis and protection against single event transients. In this project, the default library of SET-Factor is used; however other libraries may be used if desired.

The tool basically reads the given configuration file and the library of cells to create a timing lookup table. After, it reads the input circuit BLIF file and apply capacitances to nets. All gates are simulated using the SPICE simulator specified in the configuration file, running transistor sizing algorithm, detecting controllability and observability by vector simulation and calculating electrical masking to create the timing-optimized circuit. Then, static timing analysis is performed to this circuit. The next step is the application of the asymmetrical or symmetrical resizing algorithm (depending on a user parameter entry) to generate the SET-hardened circuit. Again, the static timing analysis is performed to determine the frequency of the resized circuit. Also, the electrical masking is recalculated to determine the sensitivity of the SET-hardened circuit. As the logical masking (already calculated by the controllability and observability techniques for the timing-optimized circuit) does not need to be recalculated (it remains the same), results are then reported.

The output of the tool is only an optimization report containing sensitivity, area and frequency results for both timing-optimized and SET-hardened circuits.

3.4 Tool modification

By default, SET-Factor output is an optimization report. However, to perform the detailed analysis of the results proposed in this work, it was necessary to obtain both the timing-optimized and the SET-hardened circuit descriptions. Tool source code had to be inspected to gather these circuit descriptions from the internal data structures.

Figure 3.3 illustrates the exact point in SET-Factor source code where the tool had to be modified to gather desired circuits: the *cktgraph* data structure. Actually, both the pointed header (*cktgraph.h*) and its corresponding source (*cktgraph.cpp*) files were modified.

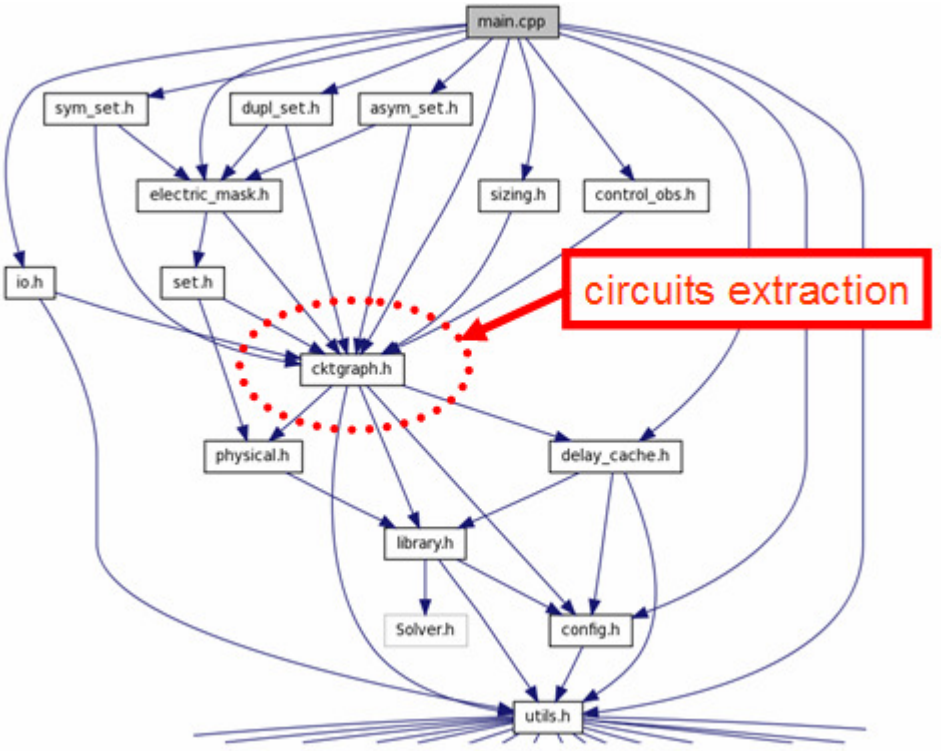


Figure 3.3: Dependency graph for main.cpp of SET-Factor

After the source code modification, both the timing-optimized and the SET-hardened circuit descriptions became default outputs of the tool. Figure 3.4 illustrates the inputs and outputs diagram after this work.

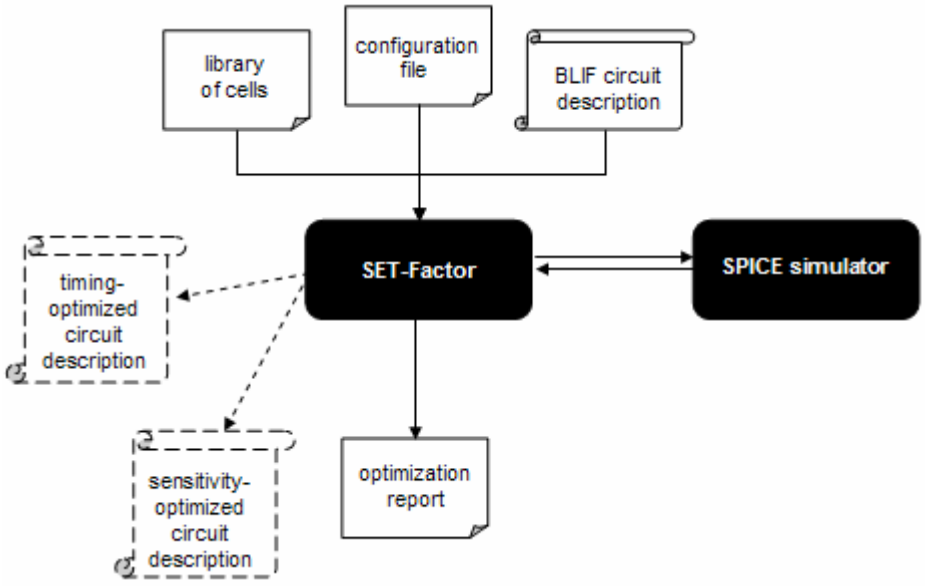


Figure 3.4: SET-Factor inputs and outputs after source code modification

4 DETAILED CIRCUIT SIMULATION ANALYSIS

The detailed circuit simulation (DCS) technique using transistor-level SPICE simulations was selected in this work. Besides being a straightforward algorithm, detailed circuit simulation using SPICE is highly accepted both in the industry and in the academy as a trustful tool to analyze different implementations of an integrated circuit and even the accuracy of results in methodologies validation. The main drawback of this technique is the time consumption which may be unacceptable by the industry, usually dealing with tight time-to-market constraints. However, in this project time-to-market is not a constraint.

4.1 SET injection

The adopted model for SET injection in the detailed circuit simulation is a transient current source addition to the harmed node (illustrated in Figure 4.1).

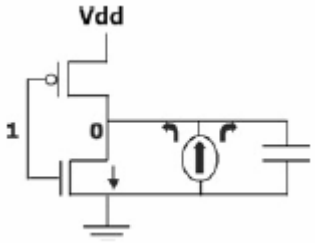


Figure 4.1: SET model for SPICE simulation (WIRTH et al, 2007)

The transient current is modeled by a double exponential equation (MESSENGER, 1982):

$$I(t) = I_0(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta})$$

Where I_0 is defined as $Q/(\tau_\alpha - \tau_\beta)$. Q represents the particle charge whereas τ_α and τ_β are constants which are very dependent on several process-related factors. In this work, τ_α was defined as 0.164×10^{-9} and τ_β was defined as 0.05×10^{-9} (DHARCHOUDHURY et al, 1994).

The SPICE current source adopted to represent this equation was the "EXP" source described below:

```
Iset 'net+' 'net-' EXP('initial_value' 'pulsed_value'
                       'rise_delay' 'tau_beta' 'fall_delay'
                       'tau_alfa')
```

Where `Iset` is the SPICE name of the source component; `net+` and `net-` are the positive and the negative nodes to connect the current source (if node is initially in logic "0", current is applied as in Figure 4.1 to produce a positive pulse in resulting voltage; however, if node is initially in logic "1" current source nodes must be inverted to produce a negative pulse in resulting voltage); `initial_value` is the starting value of the pulse (in this work, defined as "0"); `pulsed_value` is I_0 value (which is determined as $Q/(\tau_\alpha - \tau_\beta)$ for a desired charge); `tau_alfa` and `tau_beta` are the pre-defined constants τ_α and τ_β; `rise_delay` and `fall_delay` are the exponential rise and fall delays which were set as 0.5ns and 0.51ns in this work, meaning that the pulse will start to rise in 0.5ns and start to fall in 0.51ns of the SPICE simulation.

Figure 4.2 illustrates a SET propagation example. All the inputs of the NAND gates are set to "1" in order to have a sensitized path from the error site (gate with output net *G9*) to the output (net *G17*). If at least one of the inputs of the NAND gates of the SET propagation path were set to "0", the transient would be masked (as better illustrated in Section 4.2).

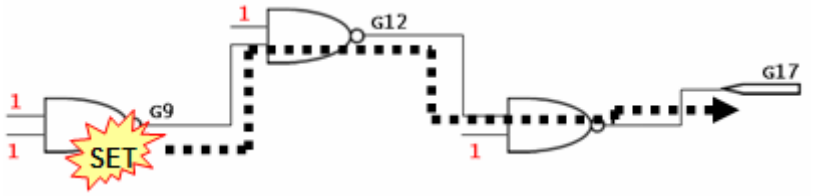


Figure 4.2: SET propagation in a sensitized path

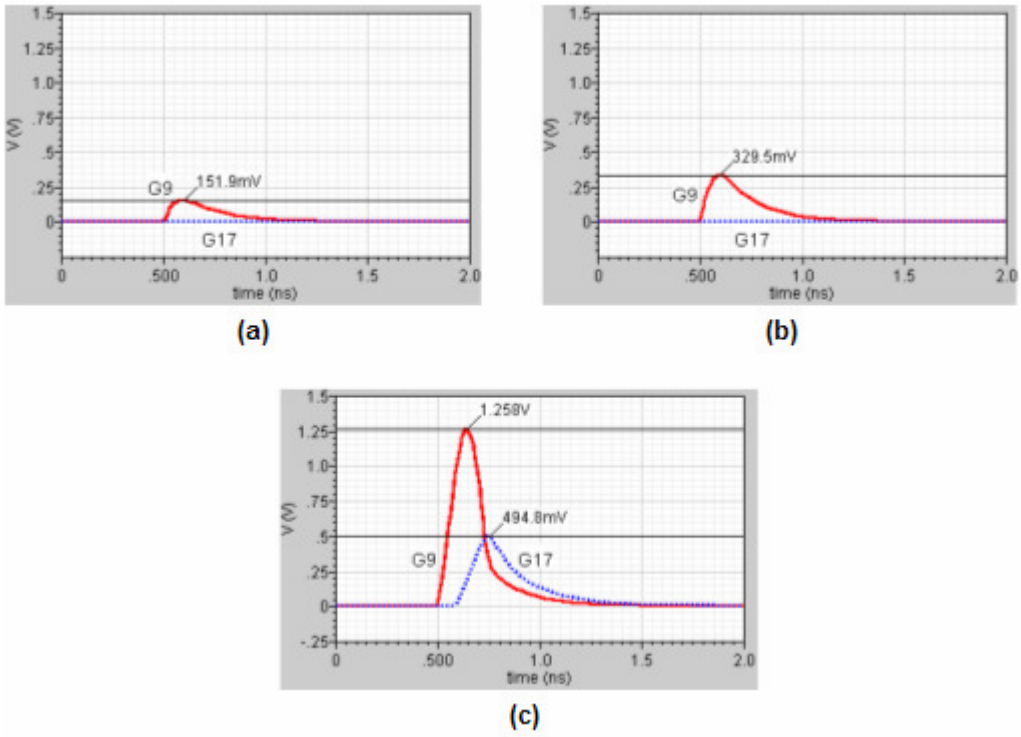


Figure 4.3: Simulation of SET effects for different charge injections: (a) Q = 0.3pC, (b) Q = 0.6pC and (c) Q = 1.0pC.

The effects of a transient in CMOS circuits are strongly dependent on its electrical charge. Injections for different charges were analyzed using *Cadence*® Virtuoso® *UltraSim* Full-Chip Simulator. All the waveforms were plotted using *Cadence*® *WaveScan* viewer. Figure 4.3 illustrates the effects of SET injection of Figure 4.2 for different charges. A charge of 0.3pC (a) and a charge of 0.6pC (b), both injected on net *G9*, had no effect in the output net *G17*. Resulting disturbance in voltage signals was not enough to reach V_{th} of the PMOS transistors of the NAND gate connected to the circuit output *G17*. In other words, PMOS transistors were not activated and a path between the output *G17* and the VDD was not created. On the other hand, a charge of 1.0pC in net *G9* led the output voltage signal to reach about 0.5V.

4.2 Logical masking analysis

Depending on the input vector that is applied to a logic gate, a single event transient may not propagate to a primary output, being "blocked" by the logical gate. When it happens, it is said the SET is logically masked. This section aims to illustrate the logical masking factor using the framework described in Section 4.1.

Figure 4.4 illustrates an example of logical masking effect on the circuit c17 of ISCAS'85 (ISCAS'85, 2010) benchmarks. A transient pulse is injected in node *G9* simulating a particle strike in the pointed gate. The input vector of the circuit was chosen in such a way to produce a NAND controlling value (logical "0") in the gates inside dashed ellipses. These controlling values should produce a logical masking effect in these gates avoiding the propagation of the transient pulse.

Figure 4.5 shows the results using the *Cadence*® *WaveScan* viewer. As expected, nodes *G15* and *G16* remained stable and pulse did not propagate through the NAND gates with controlling values. On the other hand, pulse normally propagated through the NAND gates with the other input forced to logical "1".

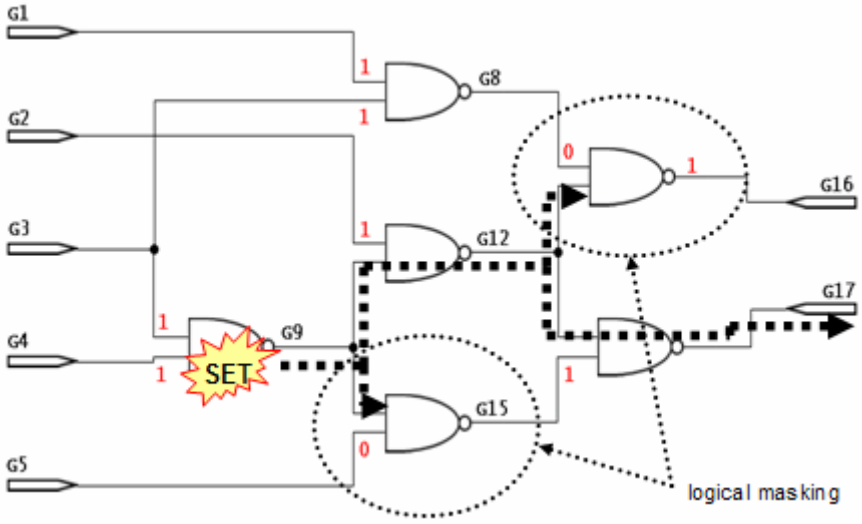


Figure 4.4: Logical masking example on c17 benchmark circuit

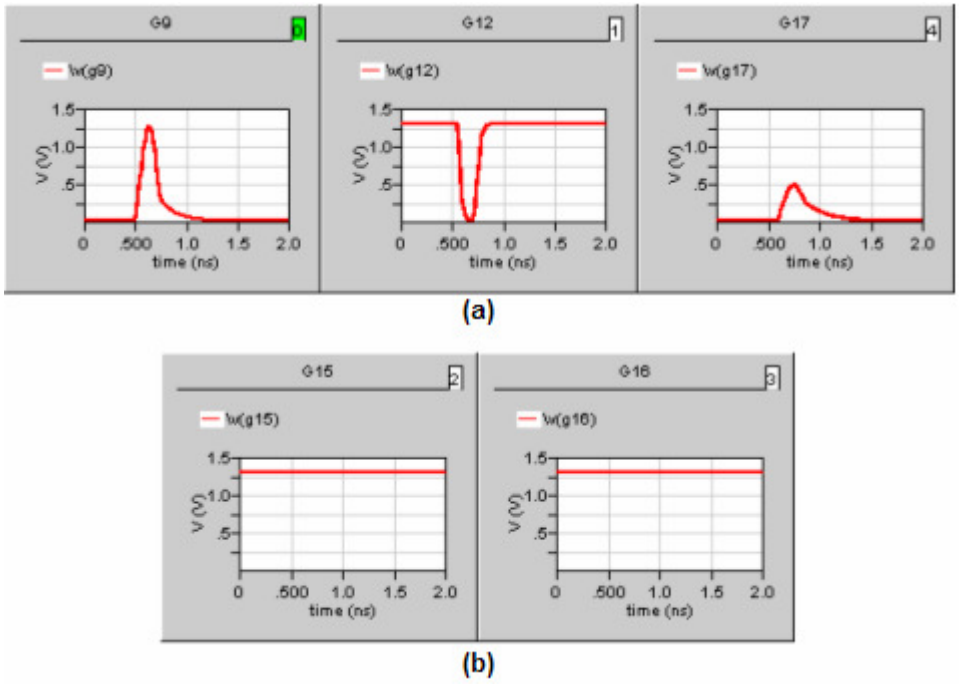


Figure 4.5: Simulation result for a SET that propagates through nodes *G12* and *G17* (a), being logically masked before nodes *G15* and *G15* (b) of c17 benchmark circuit

4.3 Electrical masking analysis

A single event transient can be seen as nothing more than an electrical signal "glitch" propagating through a circuit. Physical properties of the electrical path may attenuate this signal pulse. When this attenuation is such that the SET does not affect a primary output, it is said the transient is electrically masked. This section aims to illustrate the electrical masking factor using the framework described in Section 4.1.

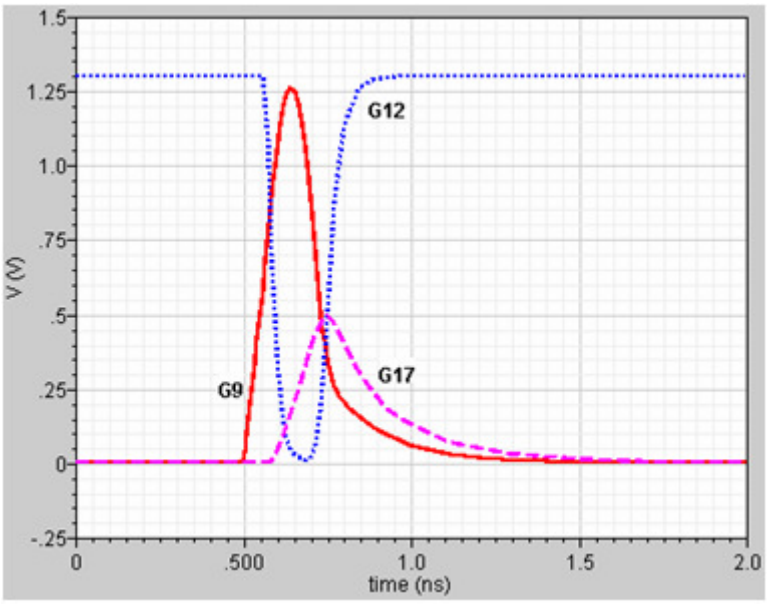


Figure 4.6: Electrical attenuation of a SET which propagates from node *G9* to *G17*

Figure 4.6 illustrates an example of electrical masking effect on the circuit c17 of ISCAS'85 benchmarks. The injected transient pulse almost reaches the VDD voltage at

the node it is injected (*G9*). As can be seen in the Figure, after short time duration, a logical state change is reflected in the next stage (*G12*) and the pulse is inverted by a NAND gate in the path. Again, after short time duration, the pulse affects the output node (*G17*). Though, when the output is reached, the initial pulse with amplitude close to VDD (1.3V, in this case) is attenuated to about 0.5V.

4.4 Methodology automation

The DCS flow automation is described here. As illustrated in Figure 4.7, a SPICE circuit description is converted to a template file for the simulator controller. Basically, the simulator template contains desired configurations to be used by the SPICE simulator, circuit inputs described as parameters to be changed by the SPICE simulator controller, transient pulse characteristics modeled as a current source (with nodes also described as parameters for the simulator controller), capacitances to stabilize the POs, SPICE statements for error monitoring in the POs and parameters for transient simulation. A simulator input template for c17 of ISCAS'85 benchmarks is presented at the end of this document (as an annex).

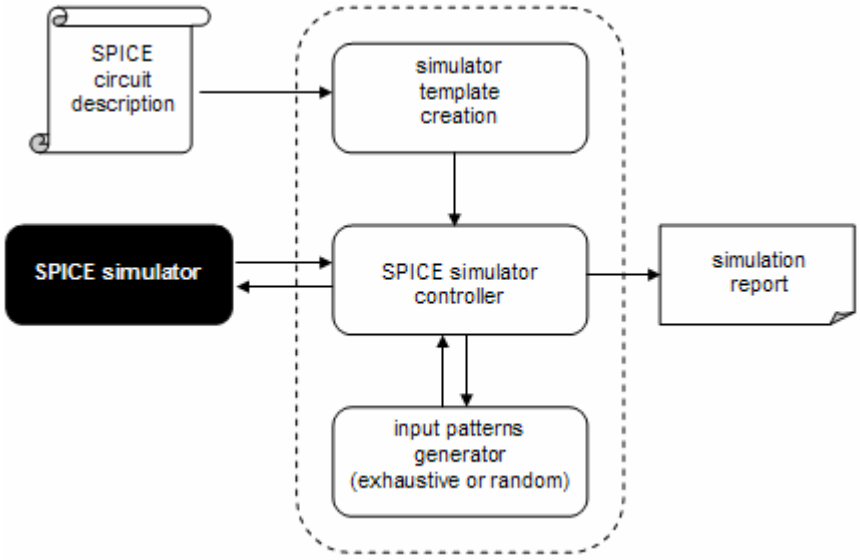


Figure 4.7: Detailed circuit simulation (DCS) overall flow

The SPICE simulator controller is responsible for modifying the parameters of the template described above. It applies all the input patterns possible (produced by the input patterns generator) if exhaustive simulation is selected or applies a desired number of input patterns if random simulation is selected. For each input pattern, each internal net of the template receives a transient pulse (by connecting the parameterized current source) and runs the SPICE simulator. If the outputs are affected, the SPICE measure statements will be triggered and the results are collected.

The input patterns generator behavior is quite simple. It returns all the input patterns combinations possible if the number of inputs only is passed as an argument. If, besides the inputs number, the desired number of input patters is also passed as argument, vectors are returned with random values.

The number of charge injections of the detailed circuit simulation implemented is given by the considered number of input patterns multiplied by the number of nets to inject pulses. In other word, the complexity of the algorithm (thus, the runtime)

exponentially increases with the number of inputs (2^n different combinations for n inputs) and linearly increases with the number of gates in the circuits (once pulses are injected only in the output nets of the circuit gates).

The framework presented here was implemented using Perl language, aiming UNIX environments. No graphical user interface was developed. Flow execution must be performed in command line.

Pulse duration in POs discussion

The pulse duration in a PO is relevant if there is latch connected to it. Latches need a specific time to store information (which is called *latching window*). As no information is given regarding the latching window of eventual sequential elements that could be connected to the outputs, errors are here characterized by the pulse amplitude rather than its duration. It seems to be a reasonable decision once the amplitude is the responsible for a logical state change, while pulse duration only determines if the erroneous value would be masked or not by a latching window. In other words, the worst case scenario is considered here: a latching window which tends to zero and thus which does not mask any error.

Adopted error situation

An error is characterized when the excursion of the voltage signal of a PO reaches a transistor threshold. In other words, a logical state change is characterized if the PO signal was 0V and it rises to V_{th} value of the NMOS transistor or if the PO signal was VDD voltage and it falls to V_{th} value of the PMOS transistor. This error situation is based on the assumption that gates of same CMOS technology would be connected to these POs.

Errors counting

It is assumed that if a pulse injection affects more than one PO, one single error is characterized. From this assumption, it is inferred that no matter if one, several or all POs are affected by a single SET injection; the fact is that the circuit response is erroneous.

5 SIMULATION RESULTS

5.1 Simulation flow description

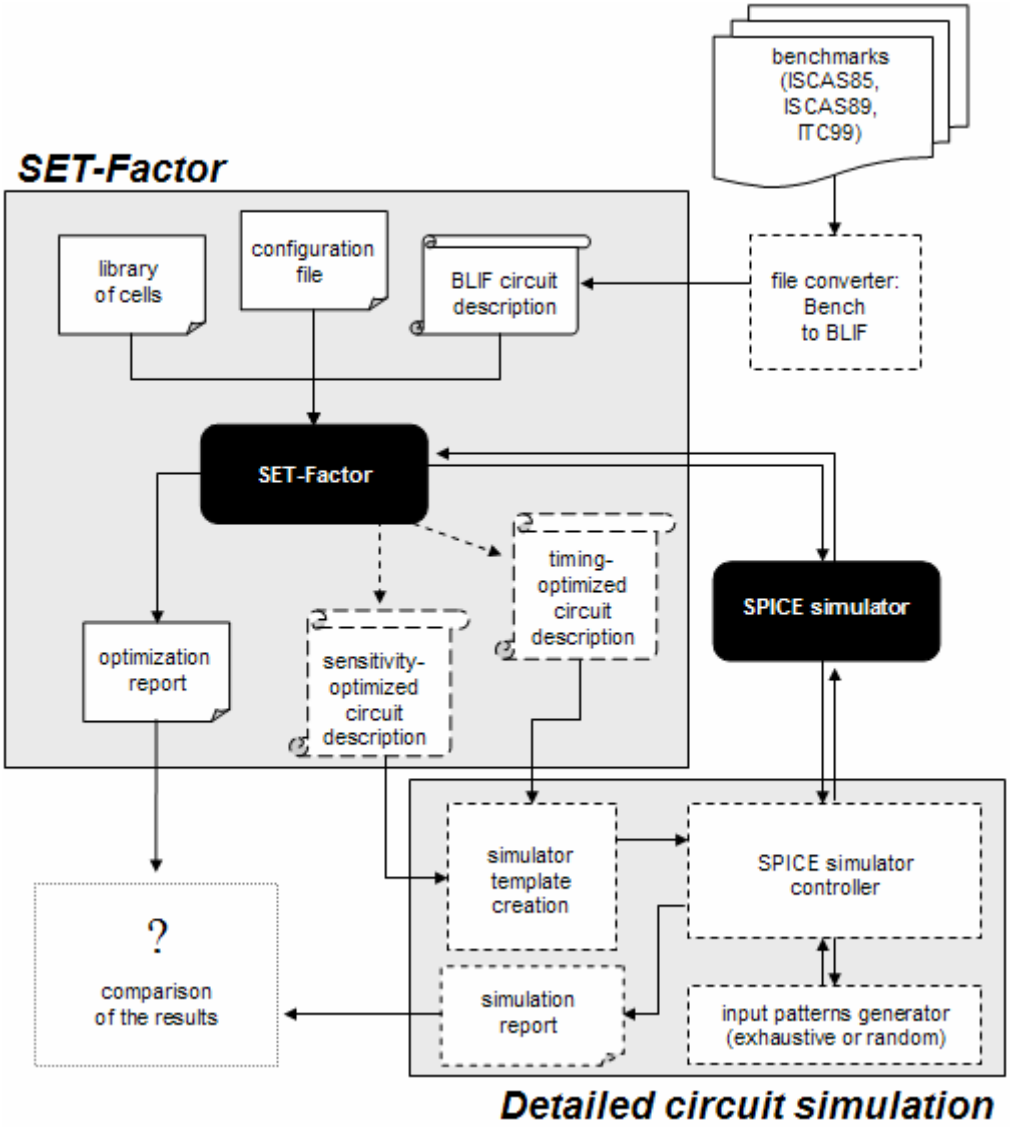


Figure 5.1: Simulation flow for the analysis of sensitivity optimization results reported by SET-Factor tool

The simulation flow for circuits hardening using SET-Factor tool as well as its results analysis using the detailed circuit simulation approach is described in Figure 5.1. All parts represented in dashed lines in the diagram were implemented for this work.

First, a set of benchmarks were selected. A file converter was created to generate SET-Factor inputs from BLIF files. Figure 5.2 shows an example of file conversion from benchmark to BLIF file for the c17 circuit. This is a simple case for file conversion that indeed could be done by hand. However, for larger circuits (with several gates) this task becomes too much time consuming and the converter becomes very useful.

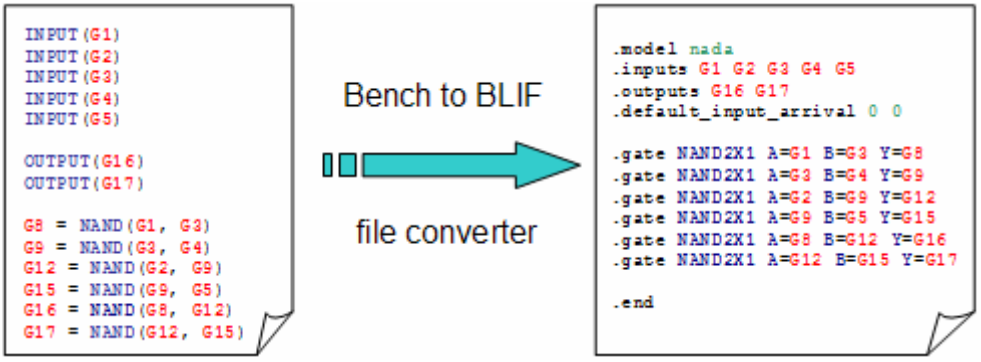


Figure 5.2: File converter applied to c17 benchmark circuit

The BLIF files are handled by SET-Factor to generate circuits with timing-optimized sizing according to a library of cells. The library of cells used in this project was a default library that comes with SET-Factor. The relevant configurations of the tool were the maximum transistor size for the sensitivity optimization (16μm), the number of input patterns to detect observability of SETs (1024) and the critical charge (1pC). In a second moment, SET-Factor analyzes the sensitivity of the timing-optimized circuits and generates SET sensitivity-optimized circuits, using either asymmetrical or symmetrical resizing. Both techniques are used and analyzed here.

Once the timing-optimized and the sensitivity-optimized circuits are generated, both are analyzed using the detailed circuit simulation. Transient pulses described in Section 4.1 are injected with a charge of 1pC to be coherent with SET-Factor optimization criteria. A better description of the benchmarks is given in Section 5.2 and results are evaluated in Section 5.3.

Injected charges discussion

Despite the fact the very few particles charge is higher than 0.3pC at the ground level (ZHOU; MOHANRAM, 2006), this charge value does not have great impact on the circuits studied in this work as seen in Section 4.1. The reason for this small impact is closely related to the transistor sizes and the technology node (130nm) used here. Therefore, a charge of higher impact was selected: 1.0pC. In this sense, the simulations performed in this work are more related to charges found in altitudes higher than ground level.

Another important remark is that in this work, no charges were injected in internal nodes of a gate. The motivation for this decision is that a particle hit at an internal node

of a gate will necessarily cause a smaller SET at the output node when compared to a direct charge injection at the output of the logical gate (WIRTH et al, 2007).

Due to the fast complexity increase of the DCS (better explained in Section 4.4), multiple gate failures were not simulated in this work, as it would result in unacceptable runtimes by the number of possible failing gates combinations. However, it is important to notice that multiple gate failures (multiple SET injections) are relevant only in random simulations, not in exhaustive simulations (mostly used here).

General simulation environment settings

SET-Factor:

- Number of input patterns to observability detection: 1024
- Maximum transistor size (w): 16µm
- Critical charge (Q_c): 1pC
- Technology: PTM 130nm (PTM, 2010)

Detailed circuit simulation:

- Injected charge (Q): 1pC
- Technology: PTM 130nm (PTM, 2010)

SPICE simulator:

- *Cadence*® Virtuoso® *UltraSim* Full-Chip Simulator

Hardware:

- CPUs: 2 x 1600MHz - Sun Blade 2500 (Silver) Server
- Microprocessors architecture: UltraSPARC-IIIi (sparcv9)
- Memory size: 2GB
- Operating system: SunOS 5.10

5.2 Benchmarks description

Table 5.1: Benchmarks statistics

Circuit	Origin	PIs	POs	Gates	Internal nets
c17	ISCAS'85	5	2	6	4
b02_opt_C	ITC'99	4	4	25	21
b06_opt_C	ITC'99	5	8	48	40
b01_opt_C	ITC'99	5	5	46	41
s27scan	ISCAS'89	7	4	16	12
s386scan	ISCAS'89	13	13	277	264
s298scan	ISCAS'89	17	20	166	146
s208scan	ISCAS'89	19	10	117	107

A set of 8 benchmark circuits was selected to be studied using both SET-Factor and the detailed circuit simulation approach. The benchmarks belong to ISCAS'85 (ISCAS'85, 2010), ISCAS'89 (ISCAS'89, 2010) and ITC'99 (ITC'99, 2010). All circuits used in this work are strictly combinational versions. Table 5.1 presents important benchmarks data for the results evaluation. All net which is neither a primary input (PI) nor a primary output (PO) is considered as an *internal net*.

5.3 Results

Benchmark circuits described in Section 5.2 were used to perform the analysis of the sensitivity reduction results reported by SET-Factor tool. First, benchmarks files were converted to BLIF files. The BLIF files were used by SET-Factor to generate a timing-optimized circuit which was also optimized by the tool using both asymmetrical and symmetrical resizing techniques. This latest step generated a here-called sensitivity-optimized circuit for each benchmark. In a second moment, both the timing-optimized and the sensitivity-optimized circuits were analyzed using detailed circuit simulation to check the effectiveness of SET-Factor hardening techniques. Protection and analyzes runtime as well as the accuracy of the results are discussed.

Table 5.2 shows the results of SET-Factor for the asymmetrical resizing hardening technique. Despite the penalties in area and frequency, the sensitivity reduction report presents optimistic results, especially for the three last benchmarks of the Table. In these cases, the initial sensitivity was quite high (more than 60%), being reduced to less than 25%. Runtimes range from about 9min to 1h10min.

Table 5.2: SET-Factor results after asymmetrical resizing

Circuit	Runtime (hh:mm:ss)	Timing optimized circuit (initial)	SET sensitivity optimized circuit (final)			
		Sensitivity	Sensitivity	Sensitivity reduction	Area overhead	Frequency overhead
c17	00:13:19	4.0 %	0.0 %	100.0 %	-32.0 %	-4.7 %
b02_opt_C	00:11:08	10.9 %	3.6 %	67.1 %	47.2 %	9.2 %
b06_opt_C	00:15:39	26.4 %	9.0 %	66.1 %	159.2 %	19.2 %
b01_opt_C	00:17:38	19.4 %	4.5 %	76.6 %	87.0 %	15.5 %
s27scan	00:09:14	5.5 %	3.5 %	36.5 %	15.9 %	17.4 %
s386scan	00:49:13	78.3 %	17.6 %	77.5 %	109.0 %	33.4 %
s298scan	01:10:30	65.7 %	23.8 %	63.8 %	240.0 %	29.5 %
s208scan	00:38:10	63.9 %	17.2 %	73.1 %	100.4 %	14.5 %

After SET-Factor optimization, the both the timing-optimized and the sensitivity-optimized circuits were simulated using detailed circuit simulation. Results are presented in Table 5.3. First five benchmarks (i.e. from c17 to s27scan) of the Table were exhaustively simulated, i.e. all input patterns possible were considered and all internal nets received SET injections. These five benchmark results represent the most accurate results of the simulations. Inspecting this table, it is possible to notice that the error rate reduction (comparing the initial circuit and the sensitivity-optimized version)

presents some negative values, which is not a good news as these negative values represent an increase in the error rates after SET-Factor optimization. As better analyzed later, the DCS starts to show good indicatives that asymmetrical resizing hardening technique of SET-Factor is not 100% reliable. Another remark from this Table is the reported runtime: the worst case took more than 68 hours to simulate using DCS.

Table 5.3: DCS results for asymmetrical resizing

Circuit	Injected SETs	Timing optimized circuit (initial)			SET sensitivity optimized circuit (final)			Error rate reduction
		Runtime (hh:mm:ss)	Errors in POs	Error rate (%)	Runtime (hh:mm:ss)	Errors in POs	Error rate (%)	
c17	128	00:31:44	20	15.6	00:32:06	6	4.7	70.0 %
b02_opt_C	336	01:57:45	21	6.3	02:36:25	23	6.3	-0.6 %
b06_opt_C	1280	08:32:17	230	18.0	16:01:41	217	17.0	5.7 %
b01_opt_C	1312	10:14:29	173	13.2	18:49:28	204	15.6	-17.9 %
s27scan	1536	07:32:14	28	1.8	07:01:48	12	0.8	57.1 %
s386scan	2216	20:48:34	57	2.6	68:06:20	84	3.8	-47.4 %
s298scan	1280	10:52:26	88	6.9	31:58:54	117	9.1	-33.0 %
s208scan	1824	16:00:32	321	17.6	44:25:52	322	17.6	-0.3 %

The same procedure of evaluation was also performed for the symmetrical resizing technique. Table 5.4 shows the results of SET-Factor. Again, sensitivity reduction report presents quite optimistic results despite the significant penalties in area and frequency. Runtime results show that, in general, the symmetrical hardening is a little bit faster than the asymmetrical technique.

Table 5.4: SET-Factor results after symmetrical resizing

Circuit	Runtime (hh:mm:ss)	Timing optimized circuit (initial)	SET sensitivity optimized circuit (final)			
		Sensitivity	Sensitivity	Sensitivity reduction	Area overhead	Frequency overhead
c17	00:09:22	4.0 %	0.0 %	100.0 %	-9.9 %	-0.3 %
b02_opt_C	00:11:31	10.9 %	2.8 %	74.1 %	102.3 %	16.7 %
b06_opt_C	00:14:49	26.3 %	7.8 %	70.3 %	310.2 %	13.4 %
b01_opt_C	00:17:16	19.4 %	5.3 %	72.9 %	185.0 %	11.0 %
s27scan	00:09:19	5.5 %	3.0 %	45.3 %	36.5 %	12.9 %
s386scan	00:32:39	78.6 %	18.1 %	77.0 %	206.8 %	17.5 %
s298scan	00:48:55	65.1 %	27.3 %	58.1 %	467.2 %	22.0 %
s208scan	00:38:41	64.2 %	18.1 %	71.9 %	217.1 %	0.9 %

SET-Factor results for the symmetrical resizing technique were also analyzed with DCS. However, as shown in Table 5.5, the error rate reduction after the sensitivity-optimization was confirmed by the DCS, for almost all benchmarks, indicating more reliability in symmetrical resizing than in asymmetrical resizing results. Also, runtimes for the sensitivity-optimized circuits using symmetrical resizing were, in general, shorter than those reported in Table 5.3.

Table 5.5: DCS results for symmetrical resizing

Circuit	Injected SETs	Timing optimized circuit (initial)			SET sensitivity optimized circuit (final)			Error rate reduction
		Runtime (hh:mm:ss)	Errors in POs	Error rate (%)	Runtime (hh:mm:ss)	Errors in POs	Error rate (%)	
c17	128	00:31:44	20	15.6	00:23:06	0	0.0	100.0 %
b02_opt_C	336	01:57:45	21	6.3	01:35:04	3	0.1	85.7 %
b06_opt_C	1280	08:32:17	230	18.0	09:14:04	16	1.3	93.0 %
b01_opt_C	1312	10:14:29	173	13.2	08:50:34	56	4.3	67.6 %
s27scan	1536	07:32:14	28	1.8	07:12:24	0	0.0	100.0 %
s386scan	2216	20:48:34	57	2.6	21:09:28	57	2.6	0.0 %
s298scan	1280	10:52:26	88	6.9	15:32:06	17	1.3	80.7 %
s208scan	1824	16:00:32	321	17.6	18:58:12	74	4.1	77.0 %

Last three benchmarks (i.e. s386scan, s298scan and s208scan) of Tables 5.3 and 5.5 were simulated using random input patterns (i.e. 8, 8 and 16 input vectors, respectively) as the simulation time for exhaustive approach is unfeasible.

Runtime analysis

Both the runtime of SET-Factor optimization and the DCS results are analyzed here. All runtime considered in this work includes the runtime of the SPICE simulator (*UltraSim*) as both SET-Factor and DCS depends on it.

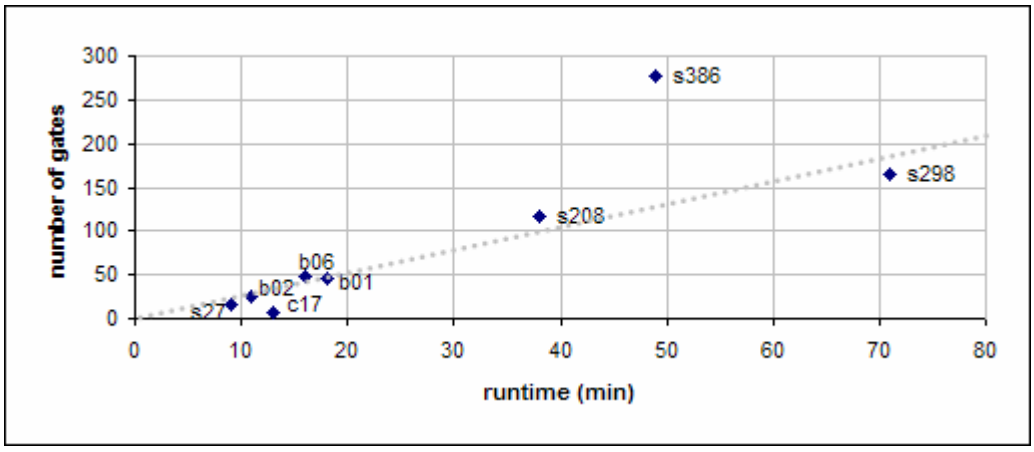


Figure 5.3: SET-Factor runtime for sensitivity optimization using asymmetrical resizing

Figure 5.3 illustrates a linear increase on the runtime of SET-Factor according to the number of gates in the circuit. This is expected, once, as explained in Section 3.2, the

tool evaluates the sensitivity and performs the resizing visiting each node. This number of "visits" linearly increases with the number of gates. The s386 benchmark represents an exception in the results. Theoretically, the runtime for the s298 should be shorter than for the s386 as it has a smaller number of gates. An explanation would be that s298 has significantly more POs and PIs than s386, and as SET-Factor traverses the circuit from each PO to each PI, this would introduce more complexity (runtime) for the tool execution.

The runtime of SET-Factor for the symmetrical resizing optimization is illustrated in Figure 5.4. Again, s386 benchmark is an exception for a linear increase according to number of gates in the circuit.

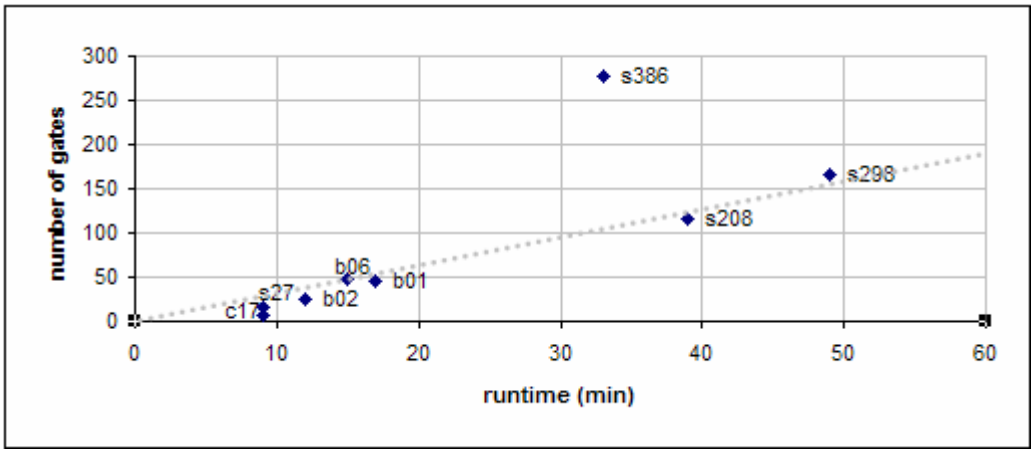


Figure 5.4: SET-Factor runtime for sensitivity optimization using symmetrical resizing

Figure 5.5 illustrates the effort of DCS, comparing the runtime between timing-optimized (before asymmetrical resizing) and the sensitivity-optimized (after asymmetrical resizing) circuits for the same number of SET injections (represented by the triangles) in both circuit versions. Even with the same number of gates and pulse injections, the difference in the runtime becomes higher for larger circuits like s298, s208 and s386.

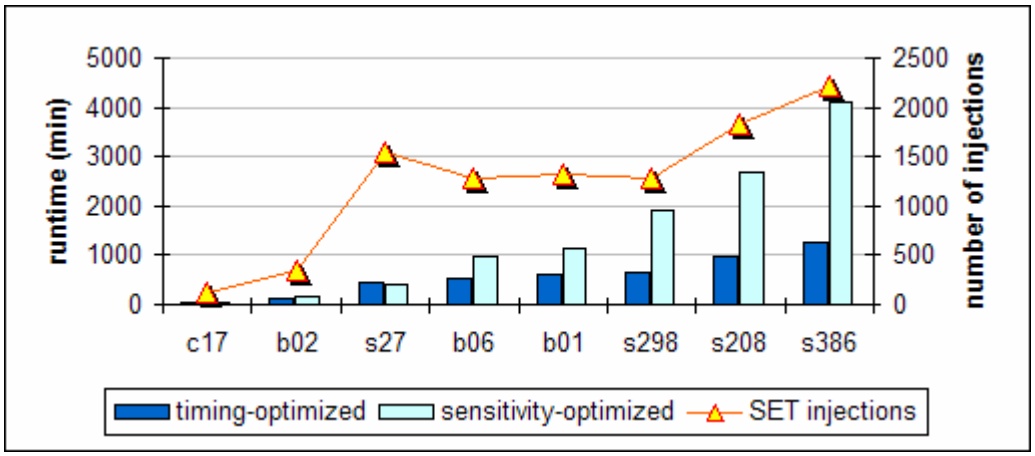


Figure 5.5: Comparison of DCS runtime for the benchmarks before and after asymmetrical resizing

Maybe a reason for this significant increase in runtime is that the asymmetrical resizing requires more effort from the SPICE simulator used in this work (*UltraSim*). A step called "building models" is the most time consuming part of the simulations and its

execution time increases with the number of gates in the circuit. As the only difference between the timing-optimized and the sensitivity-optimized circuits simulation was the transistors sizing, maybe it is possible to infer that the execution time of the "building models" step also increases with the number of different gate sizing introduced by the asymmetrical resizing.

On the other hand, the sensitivity-optimized circuits using the symmetrical resizing presented almost the same execution time of the timing-optimized ones. Figure 5.6 illustrates the DCS effort for both sizing versions using the same number of SET injections on each benchmark.

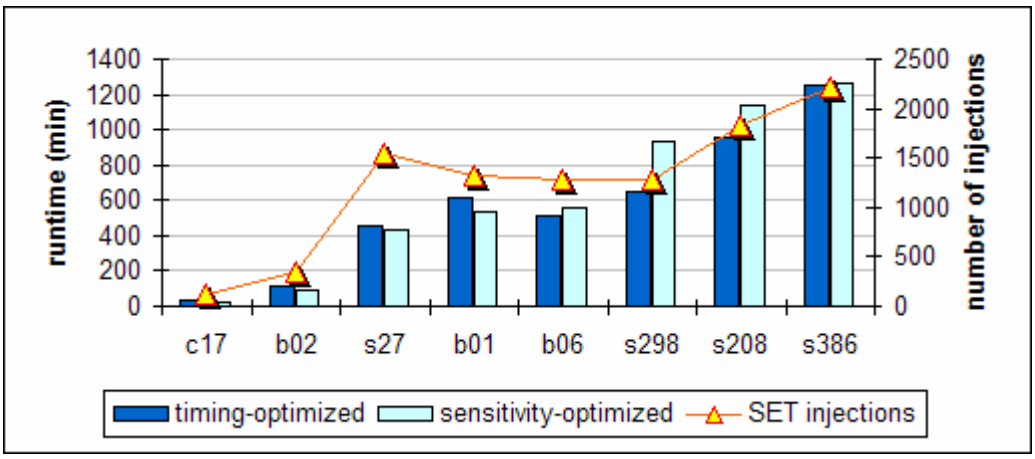


Figure 5.6: Comparison of DCS runtime for the benchmarks before and after symmetrical resizing

Accuracy analysis

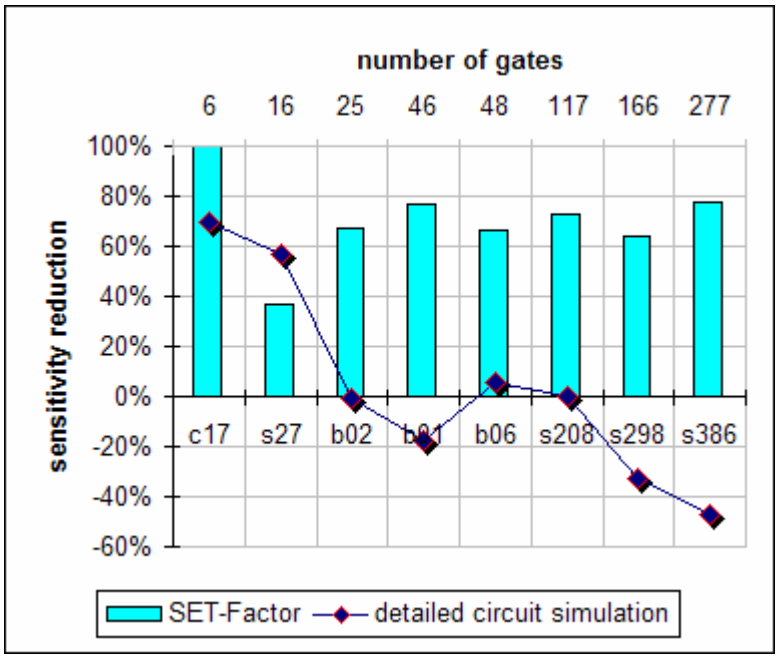


Figure 5.7: Comparison between SET-Factor results using asymmetrical resizing technique and DCS sensitivity analysis

Figure 5.7 illustrates an analysis of SET-Factor sensitivity results for the asymmetrical resizing optimization using the detailed circuit simulation. The sensitivity reduction reported by SET-Factor (represented by the vertical bars) after the benchmarks optimization is not coherent with the error rates reported by the DCS (represented by the diamonds). In five cases (b02, b01, s208, s298 and s386) the negative error rates reduction reported by DCS means that circuits became even more sensitive to SETs after SET-Factor optimization. Despite the fact that the last three benchmarks were simulated using significantly few random input patterns to have a feasible simulation runtime, they represent a good indicative (along with the first five exhaustive simulations) that the results reported for asymmetrical resizing of SET-Factor are not trustful.

In the case of the symmetrical resizing optimization, the sensitivity reduction results are more reliable. Figure 5.8 illustrate that, in five cases, the error rate reduction reported by the DCS was even higher than the sensitivity reduction reported by SET-Factor. In the case of the s27 benchmark, SET-Factor reported a sensitivity reduction of 45.3% after the optimization. Though, none of the injected pulses affected the outputs of the optimized circuit and a reduction of 100% was reported by the DCS. The s386 benchmark represents an exception: the same amount of errors was triggered by the DCS for the timing-optimized and for the sensitivity-optimized circuits, i.e. no error rate reduction. As this last benchmark is included in the set of those three circuits analyzed with significantly small random input patterns, it is not an accurate indicative of a bad result. Anyway, the first five circuits were exhaustive simulated, being a accurate indicative of the symmetrical resizing effectiveness for the SET sensitivity reduction.

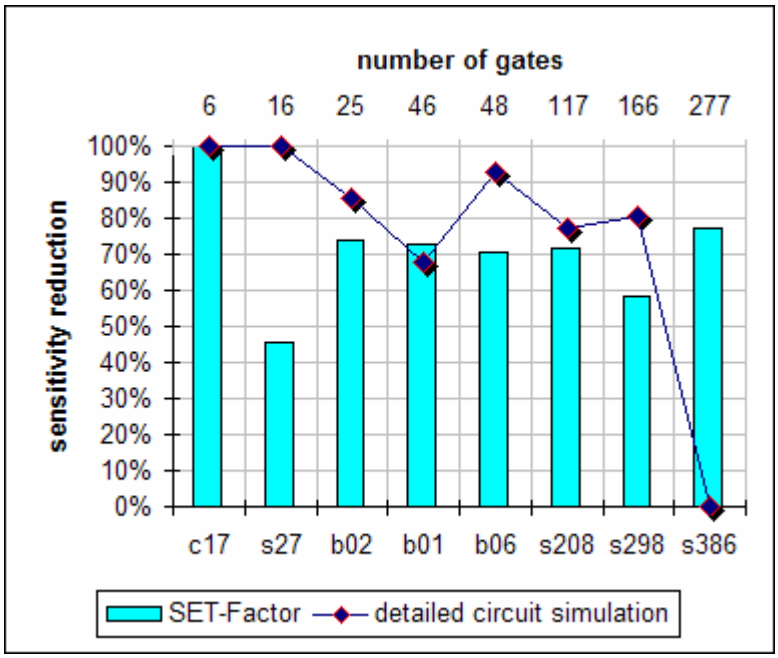


Figure 5.8: Comparison between SET-Factor results using symmetrical resizing technique and DCS sensitivity analysis

Discrepancy of results discussion

SET-Factor considers an error when the excursion of the voltage signal of a PO reaches VDD/2, whereas in detailed circuit simulation implemented in this work considers an error when the excursion of the voltage signal of a PO reaches a transistor

threshold (as explained in Section 4.4). Maybe, this difference in POs error measurements introduces some discrepancies of results because some of the attenuated voltage pulses that can be observed in SET-Factor measurements are not observed in detailed circuit simulation. Maybe not.

6 CONCLUSION

One of the main difficulties found during the tool analysis and evaluation was the lack of documentation of SET-Factor. An article published by the tool developer and also his PhD thesis were very useful documents to understand the tool goals as well as its proposed transistor resizing methodology. However, these documents do not reach the necessary level of details to understand how the resizing methodology is implemented and how SET-Factor works as a software.

As the straightforward technique of detailed circuit simulation implemented in this work runs UltraSim for each injected transient pulse, the runtime becomes critical for exhaustive simulations. The most time consuming part of SPICE simulation using UltraSim is a step called “building models”. Also, the execution time of “building models” step increases with the number of gates in the circuit. In future works, one possibility to improve the runtime of the technique implemented is to run UltraSim only once, varying SET injection nets and input patterns during a single run of the simulator. In this case, primary outputs monitoring would be performed for a given clock frequency, i.e., considering a maximum propagation delay for a SET to produce a logical state change in these outputs.

This work presented good indicatives of the reliability of both asymmetrical and symmetrical resizing techniques for SET sensitivity optimization of combinational logic blocks. Both techniques are performed by SET-Factor tool with improved runtime. However, results indicated low reliability for asymmetrical resizing results. On the other hand, symmetrical resizing results are quite reliable (at least in comparison to detailed circuit simulation technique applied in this work).

Presented results are not conclusive to invalidate the asymmetrical resizing of SET-Factor because of the few sample of benchmarks used here. However, this study may motivate further works in this sense, at least representing good indicatives of SET-Factor results accuracy.

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ANNEX – SIMULATOR INPUT TEMPLATE (C17)

```
.include /home/work/setfactor_modif/techs/130nm_bulk.pm
VVDD vcc 0 1.3
VGND gnd 0 0

* PIs: G3 G4 G1 G2 G5
* POs: G16 G17

*******************************************************************************
* MY FAULT INJECTION ENVIRONMENT DECLARATIONS (TEMPLATE)
*

.usim_opt sim_mode=df speed=7 analog=0

* INPUT STIMULI
.param
+ inp0001 = input_param000x
+ inp0002 = input_param000x
+ inp0003 = input_param000x
+ inp0004 = input_param000x
+ inp0005 = input_param000x

Vi0001 G3 gnd inp0001
Vi0002 G4 gnd inp0002
Vi0003 G1 gnd inp0003
Vi0004 G2 gnd inp0004
Vi0005 G5 gnd inp0005

* TRANSIENT INJECTION
* SET double exponential model
* Qc = 1.0pC (aprox. highest excursion of V < 1.3V)
.param
+cur_Io     = 8.77E-03
+tau_alfa   = 0.164E-09
+tau_beta   = 0.05E-09
+rise_delay = 0.5E-09
+fall_delay = 0.51E-09

Iset input_param1001 input_param1002 EXP(0 'cur_Io' 'rise_delay' 'tau_beta' 'fall_delay' 'tau_alfa')

*
*******************************************************************************

.subckt NAND2X1I0 G1 G3 G8 vcc gnd
MN0 G8 G1 n0 gnd NMOS L=1.3e-07 W=6.2e-07 AD=1.554e-12 PD=3.62e-06 AS=1.554e-12 PS=3.62e-06
MN1 n0 G3 gnd gnd NMOS L=1.3e-07 W=6.2e-07 AD=1.554e-12 PD=3.62e-06 AS=1.554e-12 PS=3.62e-06
MP0 G8 G1 vcc vcc PMOS L=1.3e-07 W=1.3e-06 AD=2.03e-12 PD=4.3e-06 AS=2.03e-12 PS=4.3e-06
MP1 G8 G3 vcc vcc PMOS L=1.3e-07 W=1.3e-06 AD=2.03e-12 PD=4.3e-06 AS=2.03e-12 PS=4.3e-06
.ends NAND2X1I0

.subckt NAND2X1I1 G3 G4 G9 vcc gnd
MN0 G9 G3 n0 gnd NMOS L=1.3e-07 W=1.502e-05 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MN1 n0 G4 gnd gnd NMOS L=1.3e-07 W=1.502e-05 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MP0 G9 G3 vcc vcc PMOS L=1.3e-07 W=1.57e-05 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
MP1 G9 G4 vcc vcc PMOS L=1.3e-07 W=1.57e-05 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
.ends NAND2X1I1

.subckt NAND2X1I2 G2 G9 G12 vcc gnd
MN0 G12 G2 n0 gnd NMOS L=1.3e-07 W=5.42e-06 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MN1 n0 G9 gnd gnd NMOS L=1.3e-07 W=5.42e-06 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MP0 G12 G2 vcc vcc PMOS L=1.3e-07 W=6.1e-06 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
MP1 G12 G9 vcc vcc PMOS L=1.3e-07 W=6.1e-06 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
.ends NAND2X1I2

.subckt NAND2X1I3 G9 G5 G15 vcc gnd
MN0 G15 G9 n0 gnd NMOS L=1.3e-07 W=7.02e-06 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MN1 n0 G5 gnd gnd NMOS L=1.3e-07 W=7.02e-06 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MP0 G15 G9 vcc vcc PMOS L=1.3e-07 W=7.7e-06 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
MP1 G15 G5 vcc vcc PMOS L=1.3e-07 W=7.7e-06 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
.ends NAND2X1I3

.subckt NAND2X1I4 G8 G12 G16 vcc gnd
MN0 G16 G8 n0 gnd NMOS L=1.3e-07 W=2.22e-06 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MN1 n0 G12 gnd gnd NMOS L=1.3e-07 W=2.22e-06 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MP0 G16 G8 vcc vcc PMOS L=1.3e-07 W=2.9e-06 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
MP1 G16 G12 vcc vcc PMOS L=1.3e-07 W=2.9e-06 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
.ends NAND2X1I4

.subckt NAND2X1I5 G12 G15 G17 vcc gnd
MN0 G17 G12 n0 gnd NMOS L=1.3e-07 W=2.22e-06 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
```

```
MN1 n0 G15 gnd gnd NMOS L=1.3e-07 W=2.22e-06 AD=1.0514e-11 PD=1.642e-05 AS=1.0514e-11 PS=1.642e-05
MP0 G17 G12 vcc vcc PMOS L=1.3e-07 W=2.9e-06 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
MP1 G17 G15 vcc vcc PMOS L=1.3e-07 W=2.9e-06 AD=1.099e-11 PD=1.71e-05 AS=1.099e-11 PS=1.71e-05
.ends NAND2X1I5

XI0 G1 G3 G8 vcc gnd NAND2X1I0
XI1 G3 G4 G9 vcc gnd NAND2X1I1
XI2 G2 G9 G12 vcc gnd NAND2X1I2
XI3 G9 G5 G15 vcc gnd NAND2X1I3
XI4 G8 G12 G16 vcc gnd NAND2X1I4
XI5 G12 G15 G17 vcc gnd NAND2X1I5

*********************************************************************************
* MY FAULT INJECTION ENVIRONMENT DECLARATIONS (TEMPLATE)
*

* OUTPUT LOAD CAPACITANCES
C1 G16 gnd 220E-15
C2 G17 gnd 220E-15

* OUTPUTS MONITORING
.measure tran SET_rises_G16
+     trig v(G16) val=0.96 cross=1
+     targ v(G16) val=0.97 cross=1
.measure tran SET_falls_G16
+     trig v(G16) val=0.37 cross=1
+     targ v(G16) val=0.36 cross=1

.measure tran SET_rises_G17
+     trig v(G17) val=0.96 cross=1
+     targ v(G17) val=0.97 cross=1
.measure tran SET_falls_G17
+     trig v(G17) val=0.37 cross=1
+     targ v(G17) val=0.36 cross=1

* TRANSIENT SIMULATION PARAMETERS
.tran 0.01n 6n

*
*********************************************************************************

.end
```